

**General Information Silicon Timed Circuits Multiport Memory** Nonvolatile RAM **Intelligent Sockets Timekeeping User-Insertable Memory User-Insertable Memory (Secured) Battery Backup and Battery Chargers System Extension** Sip Stik Prefabs **Automatic Identification** Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 



1992-1993 PRODUCT DATA BOOK



1992-1993 PRODUCTDATA **800**K

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## **General Information**

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

Intelligent Sockets

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 

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ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
Posses	11 of 010 = xxxx	10180 384	0) 01-	16-Pin 30IC
DS0065	SOFTWARE	N/A	DS0065	910 n/9-81
DS1000	14-Pin DIP	-40 to +85	DS1000-xxx	xxx = 025  to  500  ns xxx = 025  to  500  ns
	14-Pin DIP Sheared NC	-40 to +85	DS1000K-xxx	
	8-Pin DIP	-40 to +85		xxx = 025  to  500  ns xxx = 025  to  500  ns
	14-Pin GULLWING	-40 to +85		010001 - 10010
	8-Pin GULLWING	-40 to +85	DS1000H-xxx	xxx = 025 to 500ns
	16-Pin SOIC	-40 to +85	DS1000S-xxx	xxx = 025 to 500ns
DC1000	8-Pin SOIC	-40 to +85	DS1000Z-xxx	xxx = 025  to  500  ns
DS1003	8-Pin DIP	-40 to +85	DS1003M-16	
	8-Pin DIP	-40 to +85	DS1003M-20	
	8-Pin DIP	-40 to +85	DS1003M-25	
	a mi mim	-40 to +85	DS1003M-33	
		-40 to +85	DS1003M-40	
	8-Pin GULLWING	-40 to +85	DS1003H-16	
	8-Pin GULLWING	-40 to +85	DS1003H-20	
	a Di CIII I MINIO	-40 to +85	DS1003H-25	
		-40 to +85	DS1003H-33	
	8-Pin GULLWING	-40 to +85	DS1003H-40	
	14-Pin DIP	-40 to +85	DS1003-16	
		-40 to +85	DS1003-20	
		-40 to +85	DS1003-25	
	14-Pin DIP	-40 to +85	DS1003-33	
		-40 to +85	DS1003-40	
	14-Pin GULLWING	-40 ot +85	DS1003G-16	
		-40 to +85	DS1003G-20	
	14-Pin GULLWING	-40 to +85	DS1003G-25	
	14-Pin GULLWING	-40 to +85	DS1003G-33	
DOLLARS OF	14-Pin GULLWING	-40 to +85	DS1003G-40	FMILIUD ni9+8
DS1005	14-Pin DIP	-40 to +85	DS1005-xxx	xxx = 060 to 250ns
	14-Pin DIP Sheared NC	-40 to +85	DS1005K-xxx	xxx = 060 to 250ns
	8-Pin DIP	-40 to +85	DS1005M-xxx	xxx = 060 to 250ns
	14-Pin GULLWING	-40 to +85	DS1005G-xxx	xxx = 060 to 250ns
	8-Pin GULLWING	-40 to +85	DS1005H-xxx	xxx = 060 to 250ns
DS1007	16-Pin SOIC	-40 to +85	DS1005S-xxx	xxx = 060 to 250ns
DS 1007	16-Pin DIP	-40 to +85	DS1007-xxx	xxx = 001 to 999ns
DC1010	16-Pin SOIC	-40 to +85	DS1007S-xxx	xxx = 001 to 999ns
DS1010	14-Pin DIP 14-Pin GULLWING	-40 to +85	DS1010-xxx	xxx = 050 to 500ns
		-40 to +85	DS1010G-xxx	xxx = 050 to 500ns
DC1012		-40 to +85	DS1010S-xxx	xxx = 050 to 500ns
DS1012		-40 to +85	DS1012M-xxx	xxx = 001 to 999ns
		-40 to +85	DS1012H-xxx	xxx = 001 to 999ns
DS1013		-40 to +85	DS1012Z-xxx	xxx = 001 to 999ns
	a Di Dib	-40 to +85	DS1013-xxx	xxx = 010 to 150ns
		-40 to +85	DS1013M-xxx	xxx = 010 to 150ns
	14-Pin GULLWING	-40 to +85	DS1013G-xxx	xxx = 010 to 150ns
		-40 to +85	DS1013H-xxx	xxx = 010 to 150ns
	14-Pin Sheared	-40 to +85	DS1013K-xxx	xxx = 010 to 150ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	16-Pin SOIC	-40 to +85	DS1013S-xxx	xxx = 010 to 150ns
DS1020	16-Pin DIP	0 to +85	DS1020-25	0.25ns Steps
	16-Pin DIP	0 to +85	DS1020-500	.50ns Steps
	16-Pin DIP	0 to +85	DS1020-100	1.00ns Steps
	16-Pin DIP	0 to +85	DS1020-200	2.00ns Steps
	16-Pin SOIC	0 to +85	DS1020S-250	.25ns Steps
	16-Pin SOIC	0 to +85	DS1020S-500	.50ns Steps
	16-Pin SOIC	0 to +85	DS1020S-100	1.00ns Steps
	16-Pin SOIC	0 to +85	D\$1020S-200	2.00ns Steps
DS1040	8-Pin DIP	-40 to +85	DS1040M-75	75ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-100	100ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-150	150ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-200	200ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-250	250ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-500	500ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-B50	50ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-D60	60ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-A15	15nx max pulse width
	8-Pin DIP	-40 to +85	DS1040M-A20	20ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-A32	32.5ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-B40	40ns max pulse width
	8-Pin DIP	-40 to +85	DS1040M-D70	70ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-75	75ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-100	100ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-150	150ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-200	200ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-250	250ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-500	500ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-B50	50ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-D60	60ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-A15	15ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-A20	20ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-A32	32.5ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-B40	40ns max pulse width
	8-Pin GULLWING	-40 to +85	DS1040H-D70	70ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-75	75ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-100	100ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-150	150ns max pulse width
		-40 to +85	DS1040Z-200	200ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-250	250ns max pulse width
		-40 to +85	DS1040Z-500	500ns max pulse width
		-40 to +85	DS1040Z-B50	50ns max pulse width
		-40 to +85	DS1040Z-D60	60ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-A15	15ns max pulse width
	the state of the s	-40 to +85	DS1040Z-A20	20ns max pulse width
		-40 to +85	DS1040Z-A32	32.5ns max pulse width
	0 1 111 0 0 10	-40 to +85	DS1040Z-B40	40ns max pulse width
	8-Pin SOIC	-40 to +85	DS1040Z-d70	70ns max pulse width

	THE BUSINESS OF		C	RDERING INFORMATION
DEVICE	PACKAGE	OPERATING	ORDERING	SPEED
	TYPE	TEMP.	NUMBER	OR
		RANGE		VERSION
		(CELSIUS)	(cerre	
DS1200	10Pin DIP	0 to + 70	DS1200	
	10-Pin DIP	-40 to +85	DS1200N	
	16-Pin SOIC	0 to +70	DS1200S	
	16-Pin SOIC	-40 to +85	DS1200SN	
DS1201	Electronic Key/Tag	0 to +70	DS1201	
DS1202	8-Pin DIP	0 to +70	DS1202	24 x 8 RAM
	8-Pin DIP	-40 to +85	DS1202N	24 x 8 RAM
	16-Pin SOIC	0 to +70	DS1202S	24 x 8 RAM
	16-Pin SOIC	-40 to +85	DS1202SN	24 x 8 RAM
DS1203S-B1	8-Pin SOIC	0 to +70	DS1203S-B1	
	8-Pin SOIC	-40 to +85	DS1203SN-B1	
DS1204U	Electronic Key/Tag	0 to +70	DS1204U-G01	Generic Code #1
		0 to +70	DS1204U-G02	Generic Code #2
		0 to +70	DS1204U-G03	Generic Code #3
		0 to +70	DS1204U-G04	Generic Code #4
		0 to +70	DS1204U-G05	Generic Code #5
		0 to +70	DS1204U-xxx	xxx = 011 to 999
		0 to +70	DS1204U-G1C	Generic Code #1 w/cap
		0 to +70	DS1204U-G2C	Generic Code #2 w/cap
		0 to +70	DS1204U-G3C	Generic Code #3 w/cap
		0 to +70	DS1204U-G4C	Generic Code #4 w/cap
		0 to +70	DS1204U-G5C	Generic Code #5 w/cap
DS1205S	16-Pin SOIC	0 to +70	DS1205S	
	16-Pin SOIC	-40 to +85	DS1205SN	
DS1205U	Electronic Key/Tag	0 to +70	DS1205U	
DS1206	14–Pin DIP	0 to +70	DS1206	
	14-Pin DIP	-40 to +85	DS1206N	
	16-Pin SOIC	0 to +70	DS1206S	
	16-Pin SOIC	-40 to +85	DS1206SN	
DS1207	Electronic Key/Tag	0 to +70	DS1207-G01	Generic Code #1
		0 to +70	DS1207-G02	Generic Code #2
			DS1207-G03	Generic Code #3
			DS1207-G04	Generic Code #4
			DS1207-G05	Generic Code #5
			DS1207-xxx	xxx = 001  to  999
		0 to +70	DS1207-G1C	Generic Code #1 w/cap
		0 to +70	DS1207-G2C	Generic Code #2 w/cap
		0 to +70	DS1207-G3C	Generic Code #3 w/cap
		0 to +70	DS1207-G4C	Generic Code #4 w/cap
DOLOGOO DA	10001 00	0 to +70	DS1207-G5C	Generic Code #5 w/cap
DS1209S-B1	16-Pin SOIC	0 to +70	DS1209S-B1	
D04040	16-Pin SOIC	-40 to +85	DS1209SN-B1	
DS1210	8—Pin DIP	0 to +70	DS1210	
	8—Pin DIP	-40 to +85	DS1210N	
	16-Pin SOIC	0 to +70	DS1210S	
D04044	16-Pin SOIC	-40 to +85	DS1210SN	
DS1211	20-Pin DIP	0 to +70	DS1211	
	20-Pin DIP	-40 to +85	DS1211N	

DEVICE	PACKAGE TYPE 10	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20-Pin SOIC	0 to +70	DS1211S	10 K(9 4 9 12)
	20-Pin SOIC	-40 to +85	DS1211SN	
DS1212	28-Pin DIP	00 0 to +70	DS1212	
	28-Pin DIP	-40 to +85	DS1212N	
	28-Pin PLCC	0 to +70	DS1212Q	
	28-Pin PLCC	-40 to +85	DS1212QN	
DS1213B	Socket	0 to +70	DS1213B	
DS1213C	Socket	0 to +70	DS1213C	
DS1213D	Socket	0 to +70	DS1213D	
DS1215	16-Pin DIP	0 to +70	DS1215	
. 1%	16-Pin DIP	-40 to +85	DS1215N	
	16-Pin SOIC	0 to +70	DS1215S	
DS1216B	Socket		DS1216B	16/64K RAM Socket
DS1216C	Socket		DS1216C	64/256K RAM Socket
DS1216D	Socket	0 to +70	DS1216D	256K/1M RAM Socket
DS1216E	Socket	0 to +70	DS1216E	64/256K ROM Socket
DS1216F	Socket	0 to +70	DS1216F	64/256K/1M ROM Socket
DS1217A	20 Generic Code	0 to +70	DS1217A 16K-25	16K Bit Density
			DS1217A 64K-25	64K Bit Density
		0 to +70	DS1217A 128K-25	128K Bit Density
			DS1217A 192K-25	192K Bit Density
		0 to +70	DS1217A 256K-25	256K Bit Density
DS1217M		0 to +70	DS1217M 1/2-25	1/2 Megabit Density
		0 to +70	DS1217M 1-15	1 Megabit Density
		0 to +70	DS1217M 2-25	2 Megabit Density
		0 to +70	DS1217M 3-25	3 Megabit Density
		0 to +70	DS1217M 4-25	4 Megabit Density
DS1218	8-Pin DIP	0 to +70	DS1218	AOR AMELIA
	16-Pin SOIC	0 to +70	DS1218S	
DS1220AB/A	Canario Coo	0 to +70	DS1220AB	200ns
		0 to +70	DS1220AB-150	150ns
		0 to +70	DS1220AB-120	120ns
		0 to +70	DS1220AB-100	100ns
		-40 to +85	DS1220AB-IND	200ns
		-40 to +85	DS1220AB-100-IND	100ns
		0 to +70	DS1220AD	200ns
		0 to +70	DS1220AD-150	150ns
		0 to +70	DS1220AD-120	120ns
		0 to +70	DS1220AD-100	100ns
		-40 to +85	DS1220AD-IND	200ns
		-40 to +85	DS1220AD-100-IND	100ns
DS1220Y		0 to +70	DS1220Y	200ns
		0 to +70	DS1220Y-150	150ns
		0 to +70	DS1220Y-120	120ns
		0 to +70	DS1220Y-100	100ns
		-40 to +85	DS1220Y-IND	200ns
		-40 to +85	DS1220Y-100-IND	100ns

				ORI	DERING INF	ORMATION
DEVICE	PACKAGE TYPE	PRING	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION	DEVICE
DS1221	16-Pin DIP		0 to +70	DS1221		
	16-Pin DIP		-40 to +85	DS1221N		
	16-Pin SOIC		0 to +70	DS1221S		
	16-Pin SOIC		-40 to +85	DS1221SN		
DS1222	14-Pin DIP		0 to +70	DS1222		
	14-Pin DIP		-40 to +85	DS1222N		
	16-Pin SOIC		0 to +70	DS1222S		
	16-Pin SOIC		-40 to +85	DS1222SN		
DS1225AB/AD	100ns		0 to +70	DS1225AB	200ns	
			0 to +70	DS1225AB-170	170ns	
			0 to +70	DS1225AB-150	150ns	
			-40 to +85	DS1225AB-IND	200ns	
			-40 to +85	DS1225AB-150-IND	150ns	
			0 to +70	DS1225AD	200ns	
			0 to +70	DS1225AD-170	170ns	
			0 to +70	DS1225AD-150	150ns	
			-40 to +85	DS1225AD-IND	200ns	
			-40 to +85	DS1225AD-150-IND	150ns	
DS1225D/E			0 to +70	DS1225D-120	120ns	
			0 to +70	DS1225D-100	100ns	
			0 to +70	DS1225D-85	85ns	
			0 to +70	DS1225D-70	70ns	
			-40 to +85	DS1225D-120-IND	120ns	
			-40 to +85	DS1225D-70-IND	70ns	
			0 to +70	DS1225E-120	120ns	
			0 to +70	DS1225E-100	100ns	
			0 to +70	DS1225E-85	85ns	
			0 to +70	DS1225E-70	70ns	
			-40 to +85	DS1225E-120-IND	120ns	
			-40 to +85	DS1225E-70-IND	70ns	
DS1225Y			0 to +70	DS1225Y	200ns	
			0 to +70	DS1225Y-150	150ns	
			0 ot +70	DS1225Y-170	170ns	
			-40 to +85	DS1225Y-IND	200ns	
			-40 to +85	DS1225Y-150-IND	150ns	
DS1227	20-Pin DIP		0 to +70	DS1227		
	20-Pin DIP		-40 to +85	DS1227N		
	20-Pin SOIC		0 to +70	DS1227S		
	20-Pin SOIC		-40 to +85	DS1227SN		
DS1228	16-Pin DIP		0 to +70	DS1228		
	16-Pin SOIC		0 to +70	DS1228S		
DS1229	20-Pin DIP					
	20-Pin SOIC		0 to +70			
DS1230Y/AB				DS1230AB	200ns	
				DS1230AB-150	150ns	
			0 to +70			

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DS1230AB-100 DS1230AB-85 100ns 85ns

ACTIMOM SOFT 0 to +70 ACTIMOM SOFT 0 to +70

DEVICE	PACKAGE TYPE 10	TEMP.	NUMBER	SPEED OR VERSION	1000000
		0 to +70	DS1230AB-70	70ns	1021
		-40 to +85	DS1230AB-IND	200ns	
		-40 to +85			
		-40 to +85		85ns	
		-40 to +85		70ns	
		0 to +70	DS1230Y	200ns	
		0 to +70		150ns	
			DS1230Y-120	120ns	
			DS1230Y-100	100ns	
			DS1230Y-85	85ns	
		0 to +70		70ns	
			DS1230Y-IND	200ns	
				120ns	
			DS1230Y-85-IND	85ns	
			DS1230Y-70-IND	70ns	
DS1231			DS1231-20	20	
501201		0 to +70		35	
	8-Pin DIP			50	
	8-Pin DIP			20	
			DS1231N-35	35	
	8-Pin DIP		DS1231N-50	50	
	8-Pin GULLWING			20	
	8-Pin GULLWING			35	
	8-Pin GULLWING			50	
	8-Pin GULLWING		DS1231GN-20	20	
	8-Pin GULLWING	-40 to +85		35	
	8-Pin GULLWING		DS1231GN-50	50	
	16-Pin SOIC		DS1231S-20	20	
	16-Pin SOIC	0 to +70		35	
	16-Pin SOIC			50	
	10 DI 0010		DS1231SN-20	20	
	16-Pin SOIC		DS1231SN-35	35	
		-40 to +85		50	
DS1232	8-Pin DIP		DS1232		
	8-Pin DIP				
	8-Pin GULLWING	0 to +70			
			DS1232GN		
DS1232LP					
			DS1232LPSN		
DS1233 5V			DS1233-10	10% MONIT	OR
			DS1233-15	15% MONIT	
			DS1233-10N	10% MONIT	
			DS1233-15N	15% MONIT	

DEVICE	PACKAGE	OPERATING	ORDERING	DERING INFOR	agivan
DEVICE	TYPE	TEMP.	NUMBER	OR	
	иогеязу	RANGE	MAR	VERSION	
	SOT-223	0 to +70	DS1233Z-10	10% MONITOR	
	SOT-223	0 to +70	DS1233Z-15	15% MONITOR	
	SOT-223	-40 to +85	DS1233Z-10N	10% MONITOR	
	SOT-223	-40 to +85	DS1233Z-15N	15% MONITOR	
DS1233A 3.3	V TO-92	0 to +70	DS1233B-10	10% MONITOR	
	TO-92	0 to +70	DS1233B-15	15% MONITOR	
	TO-92	-40 to +85	DS1233B-10N	10% MONITOR	
	TO-92	-40 to +85	DS1233B-15N	15% MONITOR	
	SOT-223	0 to +70	DS1233BZ-10	10% MONITOR	
	SOT-223	0 to +70	DS1233BZ-15	15% MONITOR	
	SOT-223	-40 to +85	DS1233BZ-10N	10% MONITOR	
	SOT-223		DS1233BZ-15N	15% MONITOR	
DS1234	14-Pin DIP		DS1234		
	16-Pin SOIC		DS1234S		
DS1236	16-Pin DIP	0 to +70	DS1236	10% MONITOR	
	16-Pin DIP	0 to +70	DS1236-5	5% MONITOR	
	16-Pin DIP	-40 to +85		10% MONITOR	
	16-Pin DIP		DS1236N-5	5% MONITOR	
	16-Pin SOIC		DS1236S	10% MONITOR	
	16-Pin SOIC		DS1236S-5	5% MONITOR	
	16-Pin SOIC		DS1236SN	10% MONITOR	
	16-Pin SOIC		DS1236SN-5	5% MONITOR	
DS1237			DS1237-x	x = 1 TO 8	
			DS1237S-x	x = 1 TO 8	
DS1238			DS1238	10% MONITOR	
		0 to +70		5% MONITOR	
		0 to +70		10% MONITOR	
	16-Pin SOIC			5% MONITOR	
DS1239	16-Pin DIP			10% MONITOR	
		0 to +70		5% MONITOR	
	16-Pin DIP			10% MONITOR	
	16-Pin DIP		DS1239N-5	5% MONITOR	
	16-Pin SOIC			10% MONITOR	
	16-Pin SOIC		DS1239S-5	5% MONITOR	
	16-Pin SOIC		DS1239SN	10% MONITOR	
	16-Pin SOIC	-40 to +85	DS1239SN-5	5% MONITOR	
DS1243Y	28-Pin Encap. DIP	0 to +70	DS1243Y	8K x 8 RAM; 200	ne
DS1244Y		0 to +70		8K x 8 RAM; 150	
	28-Pin Encap. DIP		DS1244Y-120	8K x 8 RAM; 120	
DS1245Y/AB			DS1245AB-120	120ns	115
012101710			DS1245AB-100	100ns	
			DS1245AB-100		
				85ns 70ns	
		-40 to +85	DS1245AB_70		
			DS1245AB-120-IND	120ns 85ns	
			DS1245AB-85-IND		
			DS1245AB-70-IND	70ns	
			DS1245Y-120	120ns	
		0 to +70	DS1245Y-100	100ns	

DEVICE	PACKAGE TYPE		OPERATIN TEMP. RANGE (CELSIUS)		ORDERING NUMBER	SPEED OR VERSION	
	ROTHON AND C	11-586	0 to +70	07	DS1245Y-85	85ns	
			0 to +70			70ns	
						120ns	
						85ns	
					DS1245Y-70-IND	70ns	
DS1245FF	_					120ns	
						100ns	
DS1248Y	32-Pin Encap. DIP					128K x 8 RAM; 1	150ns
5012101	32-Pin Encap. DIP					128K x 8 RAM; 1	
DS1250	яотном жаг аз		0 to +70			TZOIC X O TIAIVI,	20113
DS1255U							
DS1258K						For CyberCard	
2012001	Kit		N/A		DS1258K-002	For CyberCard	
DS1259	16-Pin DIP		0 to +70			roi Oybeilley	
001203	16–Pin DIP						
	16-Pin SOIC						
	16-Pin SOIC						
DS1260						250 mAHr	
001200							
			0 to +70 0 to +70			500 mAHr	
DC1060	ACTIMOM AS					1000 mAHr	
DS1262	28-Pin DIP				DC4000C		
DC4007						101/	
DS1267	14-Pin DIP					10K ohms	
	14-Pin DIP					50K ohms	
	14-Pin DIP					100K ohms	
	14-Pin DIP		-40 to +85			10K ohms	
	14-Pin DIP		-40 to +85			50K ohms	
	14-Pin DIP		-40 to +85			100K ohms	
	14-Pin SOIC		0 to +70			10K ohms	
	14-Pin SOIC		0 to +70		1-1-1-1-1	50K ohms	
	14-Pin SOIC					100K ohms	
	14-Pin SOIC					10K ohms	
	14-Pin SOIC		-40 to +85			50K ohms	
			-40 to +85			100K ohms	
DS1275	8-Pin DIP				DS1275		
					DS1275S		
			-40 to +85		DS1275SN		
DS1277			0 to +70				
004000	24-Pin DIP				DS1277N		
DS1280	44-Pin Flat Pack				DS1280FP-44		
	44-Pin Flat Pack				DS1280FPN-44		
	80-Pin Flat Pack				DS1280FP-80		
	80-Pin Flat Pack						
DS1283	28-Pin DIP				DS1283	50 X 8 RAM	
	28-Pin SOIC				DS1283S	50 X 8 RAM	
DS1284			0 to +70		DS1284	50 X 8 RAM	
	28-Pin PLCC		0 to +70		DS1284Q	50 X 8 RAM	

	RDERING INFOF	Ol			
	SPEED	ORDERING	OPERATING	PACKAGE	DEVICE
	OR	NUMBER	TEMP.	TYPE	
	VERSION		RANGE		
		130)	(CELSIUS)		
	50 X 8 RAM	DS1284QN	-40 to +85	28-Pin PLCC	
	50 X 8 RAM	DS1285	0 to +70	24-Pin DIP	DS1285
	50 X 8 RAM	DS1285Q	0 to +70	28-Pin PLCC	
	50 X 8 RAM	DS1285S	0 to +70	28-Pin SOIC	
	50 X 8 RAM	DS1286	0 to +70	28-Pin Encap. DIP	DS1286
	50 X 8 RAM	DS1287	0 to +70	24-Pin Encap. DIP	DS1287
	50 X 8 RAM	DS1287A	0 to +70	24-Pin Encap. DIP	DS1287A
		DS1290	0 to +70	16-Pin Encap. DIP	DS129X
		DS1291	0 to +70	16-Pin DIP	
		DS1291N	-40 to +85	16-Pin DIP	
		DS1292	0 to +70	24-Pin Encap. DIP	
		DS1293	0 to +70	24-Pin DIP	
		DS1293N	-40 to +85	24-Pin DIP	
	512 x 8 RAM	DS1310	0 to +70	40-Pin Socket	DS1310
RTC	512 x 8 RAM +	DS1311	0 to +70	40-Pin Socket	DS1311
		DS1336	0 to +70	16-Pin DIP	DS1336
		DS1336N	-40 to +85	16-Pin DIP	
		DS1336S	0 to +70	16-Pin SOIC	
	90 49-81	DS1336SN	-40 to +85	16-Pin SOIC	
		DS1360	0 to +70	20-Pin DIP	DS1360
		DS1360N	-40 to +85	20-Pin DIP	
		DS1360S	0 to +70	20-Pin SOIC	
		DS1360SN	-40 to +85	20-Pin SOIC	
		DS1380	0 to +70	24-Pin DIP	DS1380
		DS1380N	-40 to +85	24-Pin DIP	
		DS1380S	0 to +70	24-Pin SOIC	
		DS1380SN	-40 to +85	24-Pin SOIC	
		DS1381	0 to +70		DS1381
	4K x 8 RAM	DS1385	0 to +70	24-Pin DIP	DS1385
	4K x 8 RAM	DS1385S	0 to +70	28-Pin SOIC	
0ns	8K x 8 RAM; 15	DS1386 8-150	0 to +70	32-Pin Encap. DIP	DS1386
0ns	8K x 8 RAM; 12	DS1386 8-120	0 to +70	32-Pin Encap. DIP	
50ns	32K x 8 RAM; 1	DS1386 32-150	0 to +70	32-Pin Encap, DIP	
20ns	32K x 8 RAM; 1	DS1386 32-120	0 to +70	32-Pin Encap. DIP	
	4K x 8 RAM	DS1387	0 to +70	32-Pin Encap. DIP	DS1387
8 RAM	COMPAQ; 4K x	DS1395	0 to +70	24-Pin DIP	DS1395
8 RAM	COMPAQ; 4K x	DS1395S	0 to +70	28-Pin SOIC	
8 RAM	COMPAQ; 4K x	DS1397	0 to +70		DS1397
	8K x 8 RAM	DS1485	0 to +70	24-Pin DIP	DS1485
	8K x 8 RAM	DS1485S	0 to +70	28-Pin SOIC	
150ns	128K x 8 RAM;	DS1486-150	0 to +70	00 D: F DID	DS1486
	128K x 8 RAM;	DS1486-120	0 to +70	32-Pin Encap. DIP	
	8K x 8 RAM	DS1488	0 to +70	24-Pin Encap. DIP	DS1488
	10 Yrs.		-20 to +70	Consumer Gr	DS1494
8 RAM	COMPAQ; 8K x		0 to +70	24-Pin DIP	DS1495
	COMPAQ; 8K x		0 to +70	28-Pin SOIC	
	COMPAQ; 8K x		0 to +70	24-Pin Encap. DIP	DS1497

ORDERIN	G INFORMATION		* * * * * * * * * * * * * * * * * * * *		
DEVICE	PACKAGE TYPE	RANGE	ORDERING NUMBER	SPEED OR VERSION	Partino
DS1585	28-Pin DIP	0 to +70	DS1585	8K x 8 RAM	
	28-Pin SOIC	0 to +70	DS1585S	8K x 8 RAM	
DS1587	28-Pin Encap. DIP	0 to +70	DS1587	8K x 8 RAM	
DS1602	8-Pin DIP	0 to +70	DS1602		
	8-Pin DIP	-40 to +85	DS1602N		
	8-Pin SOIC	0 to +70	DS1602S		
	8-Pin SOIC	-40 to +85	DS1602SN		
DS1603	7-Pin Module	0 to +70	DS1603		
	7-Pin Module	-40 to +85	DS1603N		
DS1609	24-Pin DIP	0 to +70	DS1609-35	35ns	
	24-Pin DIP	0 to +70	DS1609-50	50ns	
	24-Pin DIP	-40 to +85	DS1609N-35	35ns	
	24-Pin DIP	-40 to +85	DS1609N-50	50ns	
	24-Pin SOIC	0 to +70	DS1609S-35	35ns	
	24-Pin SOIC	0 to +70	DS1609S-50	50ns	
	24-Pin SOIC	-40 to +85	DS1609SN-35	35ns	
	24-Pin SOIC	-40 to +85	DS1609SN-50	50ns	
DS1610	16-Pin DIP	0 to +70		11 June 1—	
	16-Pin DIP	-40 to +85	DS1610N		
	16-Pin SOIC	0 to +70	DS1610S		
	16-Pin SOIC	-40 to +85	DS1610SN		
DS1613			DS1613C		
		0 to +70			
DS1630Y/A	В		DS1630AB-120	120ns	
		0 to 70	DS1630AB-100	100ns	
			DS1630AB-85	85ns	
		0 to 70	DS1630AB-70	70ns	
		-40 to +85	DS1630AB-70-IND	70ns	
		0 to 70	DS1630Y-120	120ns	
		0 to 70	DS1630Y-100	100ns	
endê		0 to 70	DS1630Y-85	85ns	
		0 to 70	DS1630Y-70	70ns	
		-40 to +85	DS1630Y-70-IND	70ns	
DS1632	16-Pin DIP	0 to 70	DS1632		
	16-Pin DIP	-40 to +85	DS1632N		
	16-Pin SOIC	0 to +70	DS1632S		
	16-Pin SOIC	-40 to +85	DS1632SN		
DS1633	3–Pin TO–220		DS1633XX	See factory for co	omplete
DS1640	16-Pin DIP	0 to 70	DS1640		
	16-Pin DIP	-40 to +85	DS1640N		
	16-Pin SOIC	0 to +70	DS1640S		
	16-Pin SOIC	-40 to +85	DS1640SN		
	16-Pin DIP	0 to +70		Consumer Grade	18 1 M
	16-Pin SOIC	0 to +70		Consumer Grade	
DS1642	28-Pin Encap. DIP	0 to +70		2K x 8 RAM; 120	
	28-Pin Encap. DIP		DS1642-150	2K x 8 RAM; 150	
DS1643	28-Pin Encap. DIP	0 to +70	DS1643-120	8K x 8 RAM; 120	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28-Pin Encap. DIP	0 to 70	DS1643-150	8K x 8 RAM; 150 ns
DS1645Y/AB		0 to 70	DS1645AB-120	120ns
		0 to 70	DS1645AB-100	100ns
		0 to 70	DS1645AB-85	85ns
		0 to 70	DS1645AB-70	70ns
		-40 to +85	DS1645AB-70-IND	70ns
		0 to 70	DS1645Y-120	120ns
		0 to 70	DS1645Y-100	100ns
		0 to 70	DS1645Y-85	85ns
		0 to 70	DS1645Y-70	70ns
		-40 to +85	DS1645Y-70-IND	70ns
DS1645EE		0 to 70	DS1645EE-100	100ns
		0 to 70	DS1645EE-85	85ns
		0 to 70	DS1645EE-70	70ns
		-40 to +85	DS1645EE-70-IND	70ns
DS1650Y/AB		0 to 70	DS1650AB-100	100ns
		0 to 70	DS1650AB-85	85ns
		0 to 70	DS1650AB-70	70ns
		-40 to +85	DS1650AB-70-IND	70ns
		0 to 70	DS1650Y-100	100ns
		0 to 70	DS1650Y-85	85ns
		0 to 70	DS1650Y-70	70ns
		-40 to +85	DS1650Y-70-IND	70ns
DS1651	8–Pin DIP	-25 to +85	DS1651	
	8-Pin SOIC	-25 to +85	DS1651S	
DS1652	8–Pin DIP	-25 to +85	DS1652	
	8-Pin SOIC	-25 to +85		
DS1653	8–Pin DIP	-25 to +85	DS1653	
	8-Pin SOIC	-25 to +85		
DS1666		0 to 70		
	14–Pin DIP		DS1666N	
	16-Pin SOIC		DS1666S	
D04007	16-Pin SOIC		DS1666SN	
DS1667	20-Pin DIP	0 to 70	DS1667	
	20-Pin DIP	-40 to +8	5DS1667N	
	20-Pin SOIC	0 to 70	DS1667S	
DC1000	20-Pin SOIC	-40 to +85	DS1667SN	
DS1668		0 to 70		
DS1669		0 to 70	DS1669 DS1669N	
		-40 to +85		
		0 to 70 -40 to +85	DS1669S DS1669SN	
DS199X-4		-40 to +85		
D3133/-4		COLORAGO HA		
		-20 to +70 -20 to +70	DOLLOON FF	
		-20 to +70		
		-20 to +70	DS1993L-F5	10 Yrs
		-20 to +70	DS1994L-F5	10 Yrs

DEVICE		OPERATING TEMP. RANGE	ORDERING NUMBER	SPEED OR VERSION	
		(CELSIUS)	2.H0)		
DS2009	28-Pin DIP (300 MIL)		DS2009-35	35ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2009-50	50ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2009-65	65ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2009-80	80ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2009	120ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009N-35	35ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009N-50	50ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009N-65	65ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009N-80	80ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009N	120ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2009D-35	35ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2009D-50	50ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2009D-65	65ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2009D-80	80ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2009D	120ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009DN-35	35ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009DN-50	50ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009DN-65	65ns	
	28-Pin DIP (300 MIL)		DS2009DN-80	80ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2009DN	120ns	
	32-Pin PLCC	0 to 70	DS2009R-35	35ns	
	32-Pin PLCC	0 to 70	DS2009R-50	50ns	
	32-Pin PLCC	0 to 70	DS2009R-65	65ns	
	32-Pin PLCC	0 to 70	DS2009R-80	80ns	
	32-Pin PLCC	0 to 70	DS2009R	120ns	
	32-Pin PLCC	-40 to +85	DS2009RN-35	35ns	
	32-Pin PLCC	-40 to +85	DS2009RN-50	50ns	
	32-Pin PLCC	-40 to +85		65ns	
	32-Pin PLCC	-40 to +85	DS2009RN-80	80ns	
	32-Pin PLCC	-40 to +85	DS2009RN	120ns	
DS2010	28-Pin DIP (600 MIL)	0 to 70	DS2010-50	50ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2010-65	65ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2010-80	80ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2010	120ns	
	28-Pin DIP (600 MIL)		DS2010N-50	50ns	
	28-Pin DIP (600 MIL)		DS2010N-65	65ns	
		-40 to +85	Doccioni co	80ns	
		-40 to +85	DS2010N	120ns	
			DS2010D-50	50ns	
	28-Pin DIP (300 MIL)		DS2010D-65	65ns	
	28-Pin DIP (300 MIL)		DS2010D-80	80ns	
	28-Pin DIP (300 MIL)			120ns	
	28-Pin DIP (300 MIL)		DS2010DN-50	50ns	
	28-Pin DIP (300 MIL)		DS2010DN-65	65ns	
	28-Pin DIP (300 MIL)		DS2010DN-80	80ns	
	28-Pin DIP (300 MIL)		DS2010DN	120ns	
		0 to 70	DS2010R-50	50ns	
	32-Pin PLCC	0 to 70	DS2010R-65	65ns	

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DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION	BOIVE
	32-Pin PLCC	0 to 70	DS2010R-80	80ns	
	32-Pin PLCC	0 to 70	DS2010R	120ns	
	32-Pin PLCC	-40 to +85	DS2010RN-50	50ns	
	32-Pin PLCC	-40 to +85	DS2010RN-65	65ns	
	32-Pin PLCC	-40 to +85	DS2010RN-80	80ns	
	32-Pin PLCC	-40 to +85	DS2010RN	120ns	
S2011	28-Pin DIP (600 MIL)	0 to 70	DS2011-50	50ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2011-65	65ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2011-80	80ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2011	120ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2011N-50	50ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2011N-65	65ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2011N-80	80ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2011N	120ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2011D-50	50ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2011D-65	65ns	
			DS2011D-80	80ns	
	28-Pin DIP (300 MIL)	0 to 70	DS2011D	120ns	
		-40 to +85	DS2011DN-50	50ns	
	28-Pin DIP (300 MIL)	-40 to +85	DS2011DN-65	65ns	
	28-Pin DIP (300 MIL)		DS2011DN-80	80ns	
			DS2011DN	120ns	
		0 to 70		50ns	
			DS2011R-65	65ns	
		0 to 70	DS2011R-80	80ns	
		0 to 70	DS2011R	120ns	
	32-Pin PLCC	-40 to +85	DS2011RN-50	50ns	
		-40 to +85	DS2011RN-65	65ns	
		-40 to +85		80ns	
	32-Pin PLCC	-40 to +85	DS2011RN	120ns	
S2012	28-Pin DIP (600 MIL)		DS2012-50	50ns	
	28-Pin DIP (600 MIL)		DS2012-65	65ns	
	28-Pin DIP (600 MIL)			80ns	
		0 to 70	DS2012	120ns	
	28-Pin DIP (600 MIL)		DS2012N-50	50ns	
	28-Pin DIP (600 MIL)		DS2012N-65	65ns	
	28-Pin DIP (600 MIL)		DS2012N-80	80ns	
	28-Pin DIP (600 MIL)		DS2012N	120ns	
			DS2012R-50	50ns	
			DS2012R-65	65ns	
			DS2012R-80	80ns	
			DS2012R	120ns	
		-40 to +85		50ns	
			DS2012RN-65	65ns	
		-40 to +85		80ns	
			DS2012RN	120ns	
S2013	28-Pin DIP (600 MIL)		DS2013-50	50ns	
	28-Pin DIP (600 MIL)		DS2013-65	65ns	

DEVICE	PACKAGE TYPE	TEMP.	NUMBER	SPEED OR VERSION	Rolvat
	28-Pin DIP (600 MIL)		DS2013-80	80ns	
	28-Pin DIP (600 MIL)	0 to 70	DS2013	120ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2013N-50	50ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2013N-65	65ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2013N-80	80ns	
	28-Pin DIP (600 MIL)	-40 to +85	DS2013N	120ns	
	32-Pin DIP (300 MIL)	0 to 70	DS2013D-50	50ns	
	32-Pin DIP (300 MIL)	0 to 70	DS2013D-65	65ns	
	32-Pin DIP (300 MIL)	0 to 70	DS2013D-80	80ns	
	32-Pin DIP (300 MIL)	0 to 70	DS2013D	120ns	
	32-Pin DIP (300 MIL)	-40 to +85	DS2013DN-50	50ns	
	32-Pin DIP (300 MIL)		DS2013DN-65	65ns	
	32-Pin DIP (300 MIL)		DS2013DN-80	80ns	
	32-Pin DIP (300 MIL)		DS2013DN	120ns	
DS2015			DS2015		
	20-Pin SOIC	0 to +70	DS2015S		
DS2016	24-Pin DIP		DS2016		
			DS2016S		
DS2064			DS2064		
			DS2064S		
OS2107			DS2107S		
DS2130			DS2130		
			DS2130N		
			DS2130Q		
			DS2130QN		
DS2132			DS2132		
		-40 to +85			
			DS2132Q		
		and the second second second	DS2132QN		
DS2141			DS2141		
			DS2141N		
			DS2141Q		
			DS2141QN		
DS2145			DS2145		
		-40 to +85			
			DS2145Q		
			DS2145QN		
DS2146					
DS2165					
		-40 to +85			
		-40 to +85			
DS2167					
002101			DS2167N		
			DS2167Q		

DEVICE	PACKAGE TYPE	RANGE	ORDERING NUMBER	SPEED OR VERSION	
	28-Pin PLCC	-40 to +85	DS2167QN	жта	TAUSCRE
DS2168	24-Pin DIP	0 to +70	DS2168		
	24-Pin DIP	-40 to +85	DS2168N		
	28-Pin PLCC	0 to +70	DS2168Q		
	28-Pin PLCC	-40 to +85	DS2168QN		
DS2175	16-Pin DIP	0 to +70	DS2175		
	16-Pin DIP	-40 to +85	DS2175N		
	16-Pin SOIC	0 to +70	DS2175S		
	16-Pin SOIC	-40 to +85	DS2175SN		
DS2176	24-Pin DIP	0 to +70	DS2176		
	24-Pin DIP	-40 to +85	DS2176N		
	28-Pin PLCC	0 to +70	DS2176Q		
	28-Pin PLCC	-40 to +85	DS2176QN		
DS2180A	40-Pin DIP	0 to +70	DS2180A		
	40-Pin DIP	-40 to +85	DS2180AN		
	44-Pin PLCC	0 to +70	DS2180AQ		
	44-Pin PLCC	-40 to +85	DS2180AQN		
DS2181A	40-Pin DIP	0 to +70	DS2181A		
	40-Pin DIP	-40 to +85	DS2181AN		
	44-Pin PLCC		DS2181AQ		
	44-Pin PLCC		DS2181AQN		
DS2182	28-Pin DIP		DS2182		
			DS2182N		
			DS2182Q		
	28-Pin PLCC	-40 to +85	DS2182QN		
DS2186		0 to +70	DS2186		
	20-Pin DIP	-40 to +85	DS2186N		
	20-Pin SOIC	0 to +70			
	20-Pin SOIC		DS2186SN		
DS2187	18-Pin DIP		DS2187		
	20-Pin SOIC		DS2187S		
DS2188			DS2188		
			DS2188N		
			DS2188S		
			DS2188SN		
DS2190-003		0 to +70	DS2190-003		
DS2219			DS2219-150	150ns	
			DS2219-120	120ns	
DS222X			DS2223	STIK	
	SOT-223		DS2223Z		
	TO-92		DS2224		
	SOT-223		DS2224Z		
DS2227			DS2227-120	120ns	
			DS2227-100	100ns	
			DS2227-70	70ns	
DS2229			DS2229-85	85ns	
			DS2229-100	100ns	
			DS2229-120	120ns	

DEVICE PACKAGE TYPE				ORDERING NUMBER	SPEED OR VERSION	
DS2244T	STIK	0 to +70	-85	DS2244T-24	2400bps	
	STIK	0 to +70		DS2244T-12u	1200bps-US only	
DS2245	STIK	0 to +70		DS2245-24	2400bps	
	STIK	0 to +70		DS2245-12	1200bps	
	STIK	0 to +70		DS2245-12u	1200bps-US only	
DS2245M	STIK	0 to +70		DS2245M	2400bps w/MNP	
DS2249	STIK	0 to +70		DS2249		
DS2249PH	STIK	0 to +70		DS2249PH		
DS2250	STIK	0 to +70		DS2250 8-8	8K RAM; 8 MHz	
	STIK	0 to +70		DS2250 8-12	8K RAM; 12 MHz	
	STIK	0 to +70		DS2250 8-16	8K RAM; 16 MHz	
	STIK	0 to +70		DS2250 32-8	32K RAM; 8 MHz	
	STIK	0 to +70		DS2250 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2250 32-16	32K RAM; 16 MHz	
	STIK	0 to +70		DS2250 64-8	64K RAM; 8 MHz	
	STIK	0 to +70		DS2250 64-12	64K RAM; 12 MHz	
	STIK	0 to +70		DS2250 64-16	64K RAM; 16 MHz	
DS2250T	STIK	0 to +70		DS2250T 8-8	8K RAM; 8 MHz	
	STIK	0 to +70		DS2250T 8-12	8K RAM; 12 MHz	
	STIK	0 to +70		DS2250T 8-16	8K RAM; 16 MHz	
	STIK	0 to +70		DS2250T 32-8	32K RAM; 8 MHz	
	STIK	0 to +70		DS2250T 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2250T 32-16	32K RAM; 16 MHz	
	STIK	0 to +70		DS2250T 64-8	64K RAM; 8 MHz	
	STIK	0 to +70		DS2250T 64-12	64K RAM; 12 MHz	
	STIK	0 to +7		0DS2250T 64-16	64K RAM; 16 MHz	
DS2251	STIK	0 to +70		DS2251 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2251 32-16	32K RAM; 16 MHz	
	STIK	0 to +70		DS2251 64-12	64K RAM; 12 MHz	
	STIK	0 to +70		DS2251 64-16	64K RAM; 16 MHz	
	STIK	0 to +70		DS2251 128-12	128K RAM; 12 MHz	
	STIK	0 to +70		DS2251 128-16	128K RAM; 16 MHz	
	STIK	0 to +70		DS2251T 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2251T 32-16	32K RAM; 16 MHz	
	STIK	0 to +70		DS2251T 64-12	64K RAM; 12 MHz	
	STIK	0 to +70		DS2251T 64-16	64K RAM; 16 MHz	
	STIK	0 to +70		DS2251T 128-12	128K RAM; 12 MHz	
	STIK	0 to +70		DS2251T 128-16	128K RAM; 16 MHz	
DS2252	STIK	0 to +70		DS2252 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2252 32-16	32K RAM; 16 MHz	
	STIK	0 to +70		DS2252 64-12	64K RAM; 12 MHz	
	STIK	0 to +70		DS2252 64-16	64K RAM; 16 MHz	
	STIK	0 to +70		DS2252 128-12	128K RAM; 12 MHz	
	STIK	0 to +70		DS2252 128-16	128K RAM; 16 MHz	
	STIK mov	0 to +70		DS2252T 32-12	32K RAM; 12 MHz	
	STIK	0 to +70		DS2252T 32-1	632K RAM; 16 MHz	
	STIK	0 to +70		DS2252T 64-12	64K RAM; 12 MHz	
	STIK	0 to +70		DS2252T 64-16	64K RAM; 16 MHz	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
2-84	STIK MSB 81-58	0 to +70	DS2252T 128-12	128K RAM; 12 MHz
	STIK	0 to +70	DS2252T 128-16	128K RAM; 16 MHz
DS2257	28-Pin DIP	-40 to +85	DS2257	
	28-Pin SOIC	-40 to +85	DS2257S	
DS2262	STIK	0 to +70	DS2262-4	4M x 1
	STIK	0 to +70	DS2262-8	8M x 1
	STIK	0 to +70	DS2262-16	16M x 1
	STIK	0 to +70	DS2262-32	32M x 1
DS2264/8	STIK		DS2264	-EXP uses DS2165Q
	STIK	0 to +70	DS2268	-EXP uses DS2165Q
DS2271	STIK	0 to +70	DS2271	
DS2271DK	Kit	N/A	DS2271DK	
DS2280/1	STIK	0 to +70	DS2280	
	STIK	0 to +70	DS2281-75	75 ohm
	STIK	0 to +70	DS2281-120	120 ohm
DS2282	STIK	0 to +70	DS2282	
DS2283	STIK	0 to +70	DS2283	
DS2284	STIK	0 to +70	DS2284	
	STIK	0 to +70	DS2287-32	32K x 8
DS2290	STIK	0 to +70	DS2290	
DS2291	STIK	0 to +70	DS2291	
DS2340	STIK	0 to +55	DS2340 64B	64K RAM; 10 MHz
	STIK	0 to +55	DS2340 256B	256K RAM; 10 MHz
	STIK	0 to +55	DS2340T 64B	64K RAM; 10 MHz
	STIK	0 to +55	DS2340T 256B	256K RAM; 10 MHz
DS2400	TO-92	-40 to +85	DS2400	
	SOT-223	-40 to +85	DS2400Z	
DS2404	16-Pin DIP	0 to +70	DS2404	512 x 8 RAM
	16-Pin SOIC	0 to +70	DS2404S	512 x 8 RAM
DS2569	16-Pin SOIC	0 to +70	DS2569S	
	16-Pin SOIC	-40 to +85	DS2569N	
DS5000	40-Pin Module	0 to +70	DS5000 8-8	8K RAM; 8MHz
	40-Pin Module	0 to +70	DS5000 8-12	8K RAM; 12MHz
	40-Pin Module	0 to +70	DS5000 8-16	8K RAM; 16MHz
	40-Pin Module		DS5000 32-8	32K RAM; 8MHz
	40-Pin Module	0 to +70	DS5000 32-12	32K RAM; 12MHz
	40-Pin Module		DS5000 32-16	32K RAM; 16MHz
OS5000FP	80-Pin FLAT PACK	0 to +70	DS5000FP-8	8 MHz
			DS5000FP-12	12 MHz
	80-Pin FLAT PACK		DS5000FP-16	16 MHz
				8 MHz
	80-Pin FLAT PACK			12 MHz
	80-Pin FLAT PACK			16 MHz
DS5000T		0 to +70		8K RAM; 8MHz
		0 to +70		8K RAM; 12MHz
		0 to +70		8K RAM; 16MHz
		0 to +70	DS5000T 32-8	32K RAM; 8MHz
	40-Pin Module	0 to +70	DS5000T 32-12	32K RAM; 12MHz

DEVICE	PACKAGE TYPE		TEMP. RANGE	ORDERING NUMBER	SPEED OR VERSION	
sHW S	40-Pin Module	52T 128-12	0 to +70	DS5000T 32-16	32K RAM; 16MHz	
DS5000TK	Kit		N/A	DS5000TK		
DS5001FP	80-Pin FLAT F	PACK	0 to +70	DS5001FP-12	12 MHz	
	80-Pin FLAT F	PACK	0 to +70	DS5001FP-16	16 MHz	
DS5002FP	80-Pin FLAT F	PACK	0 to +70	DS5002FP-12	12 MHz	
DS5311FP	80-Pin FLAT	PACK 8-88	0 to +70	DS5311FP	2.0 MHz	
	80-Pin FLAT	PACK	0 to +70	DS5311FP-A	3.0 MHz	
DS5340FP	80-Pin FLAT	PACK	0 to +70	DS5340FP	8 MHz	
	80-Pin FLAT	PACK	0 to +70	DS5340FP-A	10 MHz	
DS6071K	Kit		N/A	DS6071K		
DS620X			0 to +70	DS6201		
			0 to +70	DS6204U	Generic Code #1	
			0 to +70	DS6204U-2	Generic Code #2	
			0 to +70	DS6204U-3	Generic Code #3	
			0 to +70	DS6204U-4	Generic Code #4	
			0 to +70	DS6204U-5	Generic Code #5	
			0 to +70	DS6204U-xxx	xxx = 001  to  999	
			0 to +70	DS6207	Generic Code #1	
			0 to +70	DS6207-2	Generic Code #2	
			0 to +7	0DS6207-3	Generic Code #3	
			0 to +70	DS6207-4	Generic Code #4	
			0 to +70	DS6207-5	Generic Code #5	
			0 to +70		xx = 001  to  999	
DS6417			0 to +70	DS6417-1	1 Megabit Density	
					2 Megabit Density	
			0 to +70		4 Megabit Density	
DS9000						
DS9002				DS9002		
DS9003						
DS9005						
DS9006 DS9006K	I/A					
	Kit			DS9006K	OO Deer Medical	
			.100" Pitch		30 PosVertical 30 PosInclined	
			.100" Pitch	DS9071-30I DS9071-35V	30 Pos.–Inclined 35 Pos.–Vertical	
			.100 Pitch	DS9071-35V		
			.050" Pitch	DS9071-351	40 PosVertical	
			.050" Pitch		40 Pos.—Rt Angle-	Lii
				DS9072L-40R	40 Pos.—Rt Angle-	
			.050" Pitch		68 PosVertical	-LO
			.050" Pitch	DS9072-68I		
				DS9072H-68R		
			.050" Pitch	DS9072L-68R		
			.050" Pitch			
			.050" Pitch			
			.050" Pitch			-Hi

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				ORDERING INFORMATION
		.050" Pitch	DS9076-40	40 Pins; 40 Pos.
DS908x			DS9080V	Cyber Key-Vertical
			DS9080A	Cyber Key-Angled
			DS9081V	Cyber Key-Vertical
			DS9081A	Cyber Key-Angled
			DS9082V	Cyber Card-Vertical
			DS9082A	Cyber Card-Angled
			DS9084V	Cyber Card EV
				Recessed-Vertical
			DS9084A	Cyber Card EV
			D00004/1	Recessed-Angled
DS9092			DS9092	Panel Mount Reader
D09092			DS9092T	Panel Mount Reader
			D030321	w/ Tactile Pin
			DS9092GT	Wand Reader w/ Tactile Pin
DS9093			DS9093	Key Ring Mount
D09093			DS9093F	Key Ring Mount,
			DS9093S	Permanent Mount.
			D090930	2 Screw Holes
			DS9093P	Permanent Mount.
			D090931	1 Screw Hold, 1 Pin
				Flanged Can(F5)
DS9094			DS9094	3.2mm Can.
D03034			D03034	Thru hole Mount (R3)
			DS9094F	5.8mm Can,
			D030341	Thru hole Mount (F5)
			DS9094FS	5.8mm Can,
			D030341 0	Surface Mount (F5)
DS9096			DS9096	Semi-permanent
D03030			D03030	Adhesive Pad
DS9096P				Permanent Bond
D030301				Adhesive Pad
DS9098			DS9098	5.8 SNAP-IN Retainer(F5)
DS12885	24-Pin DIP	0 to +70	DS12885	114 X 8 RAM
D012000	28-Pin PLCC	0 to +70	DS12885Q	114 X 8 RAM
	28-Pin SOIC	0 to +70	DS12885S	114 X 8 RAM
DS12887	24-Pin Encap. DIP	0 to +70	DS12887	114 X 8 RAM
DS12887A	24-Pin Encap. DIP	0 to +70	DS12887A	114 X 8 RAM
D012007A	LT TIII LIIOAP. DII	0 10 77 0	DOILOUIA	114XOTIAW

DS9098 .		
-DS12887		

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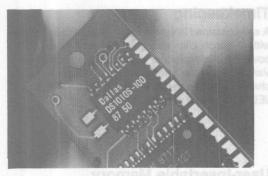
#### SALES OFFICES

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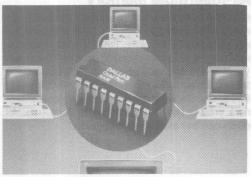
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# **Silicon Timed Circuits**

All-silicon time delay lines can withstand the high temperatures associated with surface mounting in small outline packages. They also offer better accuracy than the hybrid approach to delay lines. Laser writing techniques used to customize chips offer maximum flexibility from tailor-made products at off-the-shelf prices.



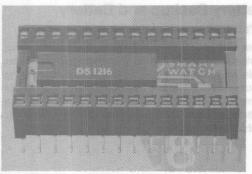
# **Multiport Memory**

A complete line of X9 FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out procedures in storing and retrieving data, the products are dual-ported for simultaneous reads and writes. This product family also includes two- and four-port RAMs that couple up to four computers at low cost.



### Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during powerloss. Partitionable NV SRAM allows the write protection of critical program and data memory.



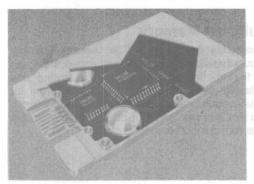
# Intelligent Sockets

Intelligent sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



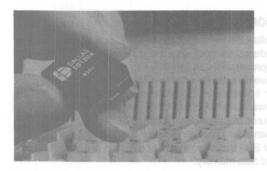
# **Timekeeping**

A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, 1-Wire serial, 3-Wire serial, PC DOS, and JEDEC bytewide memory.



# **User-Insertable Memory**

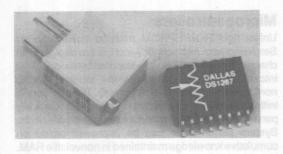
Nonvolatile memories with densities from 256 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. The CyberCard portable data carriers can be inserted and withdrawn 50,000 times. Secured versions of these of these data carriers protect data against unauthorized use. All products can be read or written by a PC.

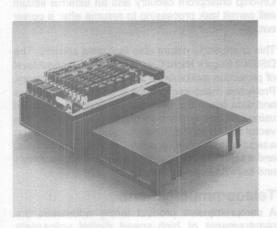


# Battery Backup and Battery Chargers

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These chips crashproof microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Products nonvolatize both static RAM and dynamic RAM. The battery charger chips optimize charging time for rechargeable batteries.







# **System Extension**

These CMOS products add a variety of special features to systems without encumbering design. The CPU Supervision circuits provides all necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. Digital Resistors change their resistance under the control of software. Line Interfaces such as the DS2107 SCSI Terminator quiet transmission lines with a precision voltage regulator and terminating resistors.

#### SIP Stik Prefabs

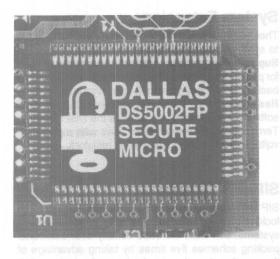
SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.

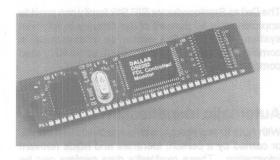
The Dallas Semiconductor SIP Stik family can provide approximately 80 percent of the circuitry in a typical system. With SIP Stik prototype accessories, a complete system can be mocked up quickly and compactly.

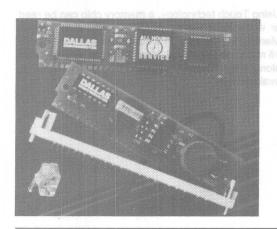
# **Automatic Identification**

With Auto ID technology, a chip attached to an object, or carried by a person, identifies and holds relevant information. These read/write data carriers can be updated via computer while affixed to an object. Auto ID chips can facilitate automation by tracking a work piece as it travels along an assembly line; people can access secure areas with convenience.

Using Touch technology, a memory chip can be read or written with the touch of a probe. Each Touch Memory is packaged in a stainless steel MicroCan<sup>™</sup> 16 mm in diameter. Individual chips are also available along with mounting accessories, probes, and an evaluation kit.







#### Microcontrollers

Unlike rigid ROM/EPROM microcontrollers, Dallas Semiconductor microcontroller chips are designed for change: they convert industry-standard bytewide SRAM into high-performance, read/write storage that is nonvolatile for more than ten years. This memory is initially loaded via a serial port and can be dynamically partitioned to fit program and data storage requirements. System performance can be improved based on cumulative knowledge maintained in nonvolatile RAM. On-chip crashproof circuitry and an external lithium cell permit task processing to resume after a power outage.

This changeable nature also facilitates security. The DS5002 Secure Micro Chip provides the highest level of protection available for firmware or data memory. Protective measures that foil attack include address and data encryption of memory contents (performed using a 64-bit key); random generation of new keys; a vector RAM area that hides reset and interrupt vectors; a security lock that protects keys and memory contents; and a self-destruct input that wipes memory contents and keys if tampering occurs.

#### **Telecommunications**

A comprehensive product family addresses the requirements of high-speed digital voice/data transmission and monitoring in T1, CEPT or Primary Rate ISDN networks. ADPCM processors double or quadruple the capacity of voice communication channels through DSP compression techniques.

# Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments — all from a desktop computer over an ordinary telephone line. A growing family of coordinated hardware and software products offers new solutions to service problems at a price well under the cost of an airplane ticket. Components include cartridges for retrofit, modular components for new designs, and a software tool kit.

The DS6071 TeleMemory w/MNP system retrofits a bytewide RAM device in an existing system. Using a 28-pin ribbon cable, the TeleMemory connects to the RAM socket and provides 32K nonvolatile RAM to the target system. A remote user can call the TeleMemory and view, edit or reload the contents of the RAM device. It is also suitable for retrofitting an EPROM and allows remote loading of firmware. The TeleMemory with MNP features error correction and data compression to ensure fast, reliable communication.

### CORPORATE FACT SHEET

Dallas Semiconductor designs, manufactures, and markets electronic chips and chip-based subsystems. Rather than build products that others have already made, the company concentrates on one-of-a-kind solutions that span many application areas. Through the use of Late Definition technologies, Soft Silicon<sup>TM</sup> chips can be tailored after they are made – even during use

Founded February 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of a variety of industries. The company's development teams constantly attack unsolved problems and introduce new products to the marketplace.

In its eight-year history, Dallas Semiconductor has shipped 150 base products to more than 7,000 customers worldwide. These include Original Equipment Manufacturers (OEMs) in instrumentation, factory automation, personal computers, office equipment, telecommunications, medical equipment, and mainframe computers. Over the last 5 years, the company has spent \$57.6 million on research and development.

Chips and subsystems are sold through a direct sales force, distributors and manufacturers' representatives worldwide. Sales for 1991 totaled \$103.8 million. Dallas Semiconductor has 662 employees. On March 19, 1990, the company started trading on the New York Stock Exchange under the symbol DS.

#### **TECHNOLOGY**

Dallas Semiconductor's special technologies make possible Soft Silicon<sup>TM</sup> solutions – dynamic, flexible, chip—based products that can be molded in the final manufacturing stages or during use. Soft Silicon<sup>TM</sup> is made possible by the Late Definition technologies of lithium energy and direct laser writing.

#### Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crash-proof with minimum current design techniques and spe-

cial freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

#### Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing also allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

#### MANUFACTURING AND FACILITIES

The Company's facilities encompass 230,000 square feet in north Dallas. This location includes a six-inch, submicron plant, one of the most sophisticated wafer production plants in the world. It features Class One cleanliness; automated wafer processing; dry etch using plasma techniques; and 0.15 micron direct step alignment tolerances. Automated modular process technology provides substantial flexibility in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. As an example, our pick and place machine assembles Stik subsystems under computer control and can position up to 4, 500 chips per hour. All products are shipped from Dallas after final quality assurance and testing.

#### MARKETING AND SALES

Dallas Semiconductor coordinates its selling activity from its Dallas, Texas headquarters. Eleven area sales managers call on OEM accounts and coordinate the activities of sales representative offices in North America, Europe and Asia. Dallas Semiconductor also markets its products in North America through national and regional stocking distributors.

# QUALITY AND RELIABILITY

#### QUALITY SYSTEM I good had also a second soft less

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

#### **QUALITY CONTROL PROCESSES**

- Incoming Quality Control (IQC): Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL—STD—105.
- In-Process Inspections: Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- Statistical Process Control (SPC): Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- In-Process Sample Tests: In order to guarantee the accuracy and completeness of in-process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL-STD-105.

#### **RELIABILITY SYSTEM**

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state—of—the—art environmental facility allows accelerated stresses to be performed and monitored inhouse. In addition, a metallurgical laboratory has been equipped to perform real-time x—ray, x—ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing.

Reliability data resides on a customized computerbased tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

#### **PRODUCT QUALIFICATION**

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production—ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- Prototype or Engineering Sample: Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- Prequal: Prequal products meet prototype requirements and are characterized to all data sheet limits.
   Final test and all processes used to manufacture the product are stable and under manufacturing control.
   Qualification of the product has started.
- Fully Qualified: Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

#### **RELIABILITY TESTS**

Table 1 lists the tests which an integrated circuit must pass in order to be classified as fully qualified.

### FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUITS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
Long Term Life	125°C, 5.5V	1000 Hr.	1.5%
Use Condition Prediction	55°C, 5.5V	10 years	*100 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	3.0%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	2.5%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	-55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL-STD-883 Method 2012	has fewy The	15%
Bond Pull	MIL-STD-883 Method 2011	Premold	1.5%
Dimensions	MIL-STD-883 Method 2016	was mark Deep	15%
Lead Integrity	MIL-STD-883 Method 2004	the state of the same of the s	3.0%
Solderability ,	MIL-STD-883 Method 2003	8 Hr. Steamage	3.0%

<sup>\*</sup> Combined high voltage life and long term life requirement.

**Quality Completes Our Innovation** 

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# **Silicon Timed Circuits**

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

Timekeeping

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

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User-Invertable Memory

User Intertable Memory (Secured)

Battery Backup and Battery Chargers

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# **DALLAS**SEMICONDUCTOR

# 5-Tap Silicon Delay Line

#### **PIN ASSIGNMENT FEATURES** All-silicon time delay IN 14 Vcc 16 Vcc NC T 15 NC 5 taps equally spaced 13 NC NC 2 NC 3 14 NC Delays are stable and precise NC 3 12 TAP 1 13 TAP 1 TAP 2 12 NC NC [ TAP 2 11 NC Both leading and trailing edge accuracy TAP 4 6 11 TAP 3 NC 10 TAP 3 NC [ 7 10 NC Delay tolerance ±5% or ±2 ns, whichever is greater 9 NC 9 TAP 5 TAP4 6 GND T Economical DS1000S 16-PIN SOIC 8 TAP 5 GND 7 (300 MIL) See Mech. Drawing Auto-insertable, low profile DS1000 14-PIN DIP (300 MIL) Sect. 16, Pg. 6 DS1000G 14-PIN GULLWING (300 MIL) DS1000K 14-PIN SHEARED NC Low-power CMOS See Mech. Drawings Sect. 16, Pgs. 1 & 3 TTL/CMOS-compatible Also Available Vapor phase, IR and wave solderable In Die Form Custom delays available 8 Vcc IN IN ☐ Vcc Fast turn prototypes TAP 2 7 TAP 1 TAP 2 TAP 1 6 TAP 3 Extended temperature range available TAP 4 TAP 4 6 TAP3 3 5 GND GND L TAP 5 DS1000M 8-PIN DIP (300 MIL) DS1000Z 8-PIN SOIC DS1000H 8-PIN GULLWING (300 MIL) (150 MIL) See Mech. Drawing See Mech. Drawings Section 16, Pgs. 1 & 3 Sect. 16, Pg. 5 PIN DESCRIPTION TAP 1-TAP 5 - Tap Output Number Vcc - +5 Volts GND - Ground NC - No Connection IN - Input

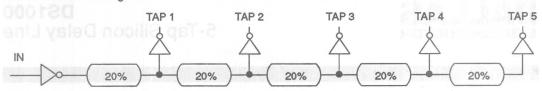
#### DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines pro-

vide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

#### **LOGIC DIAGRAM** Figure 1



# PART NUMBER DELAY TABLE (tpHL, tpLH) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1000-20*	4 ns	8 ns	12 ns	16 ns	20 ns
DS1000-25	5 ns	10 ns	15 ns	20 ns	25 ns
DS1000-30	6 ns	12 ns	18 ns	24 ns	30 ns
DS1000-35	7 ns	14 ns	21 ns	28 ns	35 ns
DS1000-40	8 ns	16 ns	24 ns	32 ns	40 ns
DS1000-45	9 ns	18 ns	27 ns	36 ns	45 ns
DS1000-50	10 ns	20 ns	30 ns	40 ns	50 ns
DS1000-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1000-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1000-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1000-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1000-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1000-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1000-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1000-250	50 ns	100 ns	150 ns	200 ns	250 ns
DS1000-350	70 ns	140 ns	210 ns	280 ns	350 ns
DS1000-450	90 ns	180 ns	270 ns	360 ns	450 ns
DS1000-500	100 ns	200 ns	300 ns	400 ns	500 ns

Custom delays available.

\*Consult Dallas Semiconductor for availability.

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#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current -1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}, \text{V}_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	orny e -zo operanty wan wer exceed 30 mA, etc.	4.75	5.00	5.25	٧	na e ten
High Level Input Voltage	V <sub>IH</sub>	lats sheet.	2.2	na. erit t	V <sub>CC</sub> + 0.5	V	eT-1e8
Low Level Input Voltage	VIL	Paris P	-0.5	a ma	0.8	٧	estatas:
Input Leakage Current	l <sub>l</sub>	0.0V ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0		1.0	uA	
Active Current	Icc	V <sub>CC</sub> = Max; Period= Min.		35	75	mA	2,8
High Level Output Current	ІОН	V <sub>CC</sub> =Min. V <sub>OH</sub> =4		1/2	-1	mA	
Low Level Output Current	loL	V <sub>CC</sub> =Min. V <sub>OL</sub> =0.5	12		Bir Na.c	mA	

#### **AC ELECTRICAL CHARACTERISTICS**

 $(t_A = 25^{\circ}C, V_{CC} = 5V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	40% of Tap 5 tplh	H143		ns	7
Input to Tap Delay (leading edge)	t <sub>PLH</sub>		Table 1		ns	3, 4, 5, 6, 9
Input to Tap Delay (trailing edge)	t <sub>PHL</sub>		Table 1		ns	3, 4, 5, 6, 9
Power-up Time	t <sub>PU</sub>			100	ms	
	Period	4 (t <sub>WI</sub> )			ns	7

#### CAPACITANCE

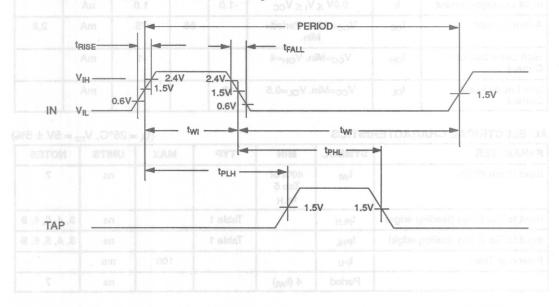
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	

#### NOTES:

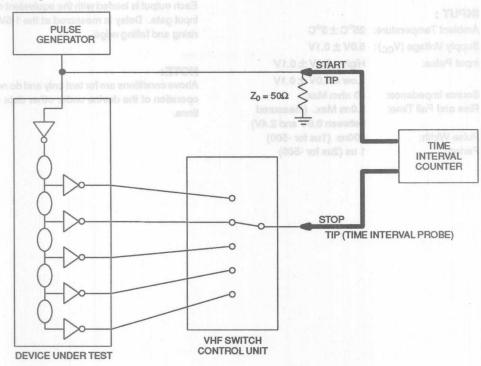
- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. V<sub>CC</sub>= 5V @25°C. Delays accurate on both rising and falling edges within ±2 ns or 5%, whichever is greater.
- 4. For DS1000 delay lines with a TAP 5 delay of 50 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input to tap delay shift of ± 1 ns or ± 3%, whichever is greater.
- 5. For DS1000 delay lines with a TAP 5 delay less than 50 ns, temperature variations from 25°C to 0°C or 70° may produce an additional input to tap delay shift of ± 1 ns or ± 10%, whichever is greater.
- All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
- Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
- 8.  $I_{CC}$  is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and  $V_{CC}$  = 5.25V will have an  $I_{CC}$  = 75 mA. For example a -100 will never exceed 30 mA, etc.
- 9. See "Test Conditions" section at the end of this data sheet.

### **TIMING DIAGRAM-SILICON DELAY LINE Figure 2**





#### **TEST CIRCUIT** Figure 3



#### **TERMINOLOGY**

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t<sub>WI</sub> (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

 $t_{\mbox{RISE}}$  (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

 $t_{\mbox{FALL}}$  (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t<sub>PLH</sub> (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse. t<sub>PHL</sub> (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

#### **TEST SETUP DESCRIPTION**

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### INPUT:

Ambient Temperature:  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ Supply Voltage (V<sub>CC</sub>):  $5.0\text{V} \pm 0.1\text{V}$ 

Input Pulse:

 $High = 3.0V \pm 0.1V$ 

 $Low = 0.0V \pm 0.1V$ 

Source Impedance: Rise and Fall Time: 50 ohm Max.

3.0ns Max. (measured between 0.6V and 2.4V)

Pulse Width: Period:

500ns (1us for -500) 1 us (2us for -500)

#### **OUTPUT:**

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

#### NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

0)

type (Time Delay, Felling): The elapsed time between the 1.5V point on the builing edge of the input pulse and the 1.5V point on the builing edge of any tap output

TEST SETUP DESCRIPTION
Figure 3 flustrates the hardware configuration used for
measuring the timing purameters on the DS1900. The
input waveform is produced by a precision pulse guner
ator under software control. Time dulays are measured
by a time interval counter (30 ps resolution) connected
between the Input and such tap. Bach tap is selected
and connected to the counter by a VHP syrifich contro
unit. All measurements are fully automated, with each
instrument controlled by a control competer over an

ed said out to epha galacid and account the solution of the editor of the editor of the part of the first of the solution of t

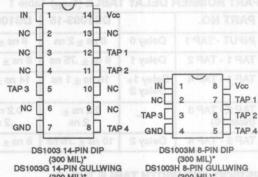
page (Time Telepo) (Neurg). The plaped time between the LUV is an accommon stope of the input pulse and the LUV point on the leading edge of any tap output

# DS1003 4-Tap Silicon Delay Line for RISC Applications

#### **FEATURES**

- All-silicon time delay
- · Four delayed clock phases from input
- Input frequency independent
- Precise tap-to-tap delays
- Leading and trailing edge precision
- Preserves input symmetry
- Output rise time minimizes ringing
- Economical
- 8- and 14-pin packages available in DIP and surface mount
- TTL/CMOS-compatible
- · Vapor phase, IR and wave solderable
- Custom delays and pinouts available
- Fast turn prototypes

#### PIN ASSIGNMENT



(300 MIL)\* See Mech. Drawings Sect. 16, Pgs. 1 & 3

(300 MIL)\* See Mech. Drawings Sect. 16, Pgs. 1 & 3

Also Available In Die Form

\*Consult Factory for Custom Packaging

#### PIN DESCRIPTION

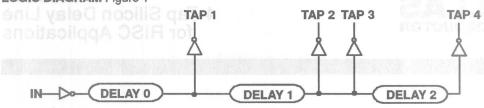
TAP 1 - TAP 4	TAP Output Number
VCC	+5 Volts
GND	Ground
NC	No Connection
IN	Input

#### DESCRIPTION

The DS1003 Delay Line has been specifically designed to supply the four independent clock timing phases required by some RISC microprocessors and their related coprocessors. For optimum compatibility, the DS1003 accepts TTL input levels and supplies CMOS and TTL compatible output levels. The DS1003 is offered in 8and 14-pin DIP and gullwing packages for surface mounting. Low cost and superior reliability is achieved by the combination of a 100% silicon delay line and industry standard packaging. The DS1003 series of delay lines provides precise tap-to-tap delays while preserving input waveform symmetry. Since the DS1003 is not based on Phase Locked Loop (PLL) technology, timing is input frequency-independent. Each tap is capable of driving a minimum of four LSTTL or CMOS loads. Tapto-tap timing accuracy is not affected by the addition of equal capacitive loads (e.g. coprocessors).

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

**LOGIC DIAGRAM** Figure 1



PART NUMBER DELAY TABLE (tplH) Table 1

PART NO.		DS1003-16	DS1003-20	DS1003-25	DS1003-33	DS1003-40*
INPUT - TAP 1	Delay 0	8 ns ± 2 ns	8 ns ± 2 ns	8 ns ± 2 ns	6 ns ± 2 ns	6 ns ± 2 ns
TAP 1 - TAP 2	Delay 1	6 ns ± .75 ns	6 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns
TAP 1 - TAP 4	Delay 1+ Delay 2	16 ns ± 1 ns	14 ns ± 1 ns	12 ns ± .75 ns	9 ns ± .75 ns	8 ns ± .75 ns
TAP 2 - TAP 3 (Note 10)	Dana A	0.2 ns ± .2 ns	0.2 ns ± .2 ns			
TAP 3 - TAP 4	Delay 2	10 ns ± .75 ns	8 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns

#### **PERIOD AND WIDTH TABLE Table 2**

PART NO.	Sect. Y	PERIOD			t <sub>WI</sub>		
	MIN	NOM	MAX	MIN	NOM	MAX	
DS1003-16	29 ns	30 ns	00	12 ns	15 ns	00	
DS1003-20	24 ns	25 ns	00	10 ns	12.5 ns	00	
DS1003-25	19 ns	20 ns	00	8 ns	10 ns	00	
DS1003-33	14 ns	15 ns	00	6 ns	7.5 ns	00	
DS1003-40*	12 ns	12.5 ns	00	5 ns	6.25 ns	00	

#### Los TABLE Table 3

PART NO.	Ic	C
	TYP.	MAX.
DS1003-16	65 mA	75 mA
DS1003-20	75 mA	85 mA
DS1003-25	85 mA	95 mA
DS1003-33	100 mA	110 mA
DS1003-40*	115 mA	125 mA

<sup>\*</sup>Consult factory for availability.

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#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current -1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 5.0V + 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	18 southe ac visco	4.75	5.00	5.25	V	enon1no
High Level Input Voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.5	n; CV=30	MagloV.
Low Level Input Voltage	V <sub>IL</sub>		-0.5	sically tests	0.8	eb yd beel	Ouaras
Input Leakage Current	I <sub>I</sub>	0.0V ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0		1.0	μА	
Active Current	Icc	V <sub>CC</sub> = Max; Period = Min.	P1 SIVEJ	Table 3	Table 3	mA	2
High Level Output Current	Іон	V <sub>CC</sub> = Min. V <sub>OH</sub> = 4		LVo.E	-1	mA	7
Low Level Output Current	loL	V <sub>CC</sub> = Min V <sub>OH</sub> = 0.5	12	Va.o	Va.o	mA	/ PAT

#### AC ELECTRICAL CHARACTERISTICS

 $(t_A = 25^{\circ}C, V_{CC} = 5.0V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	twi va	Table 2	Table 2	Table 2	ns	6
TAP to TAP Delay (leading edge)	t <sub>PLH</sub>	Table 1	Table 1	Table 1	ns	3,4,5,6,7
TAP to TAP Delay (trailing edge)	t <sub>PHL</sub>		Note 9	4.76V	ns	9
Output Symmetry (Input: 50% ± 5%)		40	50	60	%	3,5
Output Rise Time	toR	24/20	2.0	2.5	ns	8,10
Output Fall Time	toF		2.0	2.5	ns	8,10
Power-up Time	tpu			100	ms	541
Period	Period	Table 2	Table 2	Table 2	ns	

#### CAPACITANCE

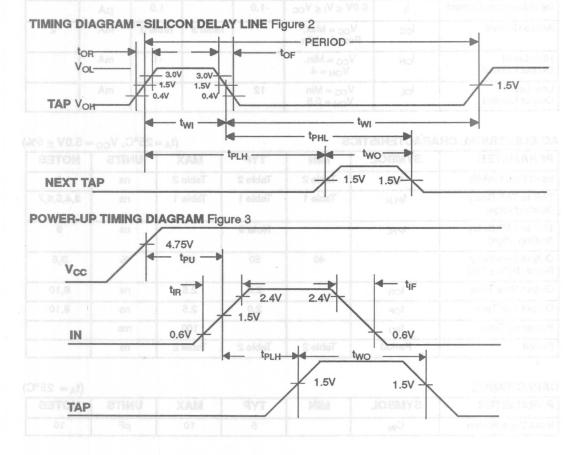
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	10

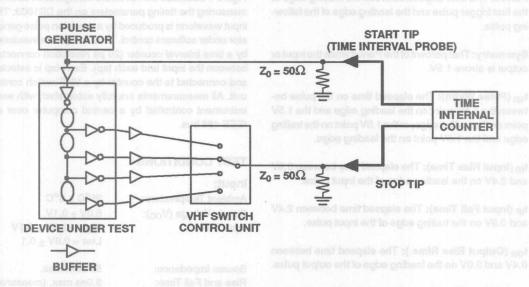
<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### NOTES

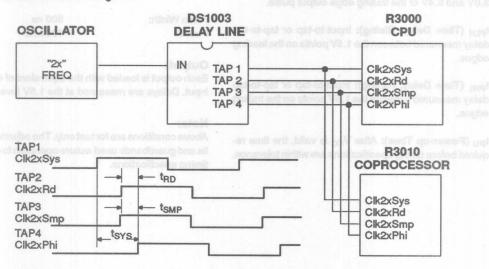
- 1. All voltages are reference to ground.
- 2. Measured with outputs open, minimum period.
- 3.  $V_{CC} = 5V @ 25^{\circ}C$ .
- 4. Temperature variations from 25°C to 0°C or 70°C may produce an additional tap-to-tap delay shift of  $\pm$  0.5ns. Voltage variations from 5.0V to 4.75V or 5.25V produce a worst case tap-to-tap delay shift of 5%.
- 5. All tap-to-tap delays vary unidirectionally over temperature or voltage range. For example, if the TAP 1 -TAP 2 delay, t<sub>PLH</sub>, slows down, the TAP2 - TAP 4 delay, t<sub>PLH</sub>, will also slow down. Since t<sub>PHL</sub> tracks t<sub>PLH</sub>, symmetry is preserved.
- 6. See "Test Conditions" section at the end of this data sheet.
- 7. Since all four taps have identical output stages, tap-to-tap delays and waveform symmetry will exhibit minimal variation when capacitive loading is increased identically on all taps at the same time (e.g., the addition of one or more RISC coprocessors).
- 8. V<sub>CC</sub> = Min; C<sub>L</sub> = 30 pF
- 9. Trailing edge delays, tPHL, are adjusted to maintain waveform symmetry.
- 10. Guaranteed by design. Periodically tested.



#### TEST CIRCUIT Figure 4



#### **TYPICAL APPLICATION Figure 5**



NOTE: TAP 2 can be used for Clk2xSmp with TAP 3 as Clk2xRd.

#### TERMINOLOGY

**Period:** The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following pulse.

Symmetry: That percent of the Period when the input or output is above 1.5V.

t<sub>WI</sub> (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t<sub>IR</sub> (Input Rise Time): The elapsed time between 0.6V and 2.4V on the leading edge of the input pulse.

t<sub>IF</sub> (Input Fall Time): The elapsed time between 2.4V and 0.6V on the trailing edge of the input pulse.

t<sub>OR</sub> (Output Rise Rime): The elapsed time between 0.4V and 3.0V on the leading edge of the output pulse.

toF (Output Fall Time): The elapsed time between 3.0V and 0.4V of the trailing edge output pulse.

t<sub>PLH</sub> (Time Delay, Rising): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the leading edges.

t<sub>PHL</sub> (Time Delay, Falling): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the trailing edges.

t<sub>PU</sub> (Power-up Time): After V<sub>CC</sub> is valid, the time required before timing specifications are within tolerance.

#### TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1003. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution connected between the input and each tap). Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### Input:

Ambient Temperature: Supply Voltage (V<sub>CC</sub>):

 $25^{\circ}C \pm 3^{\circ}C$  $5.0V \pm 0.1V$ 

Input Pulse:

High =  $3.0V \pm 0.1V$ Low =  $0.0V \pm 0.1$ 

Source Impedance:

50 ohm max.

Rise and Fall Time:

3.0ns max. (measured

between 0.6V and 2.4)

Pulse Width:

500 ns

Period:

1000 ns

#### Output:

Each output is loaded with the equivalent of one 74F04 input. Delays are measured at the 1.5V level.

#### Note:

Above conditions are for test only. The adjusted test limits and guardbands used assure operation to data sheet timing specifications.



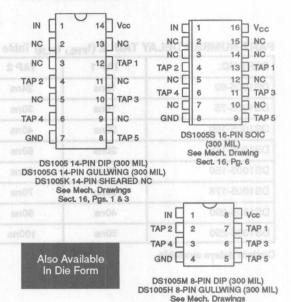
# DS1005 5-Tap Silicon Delay Line

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#### **FEATURES**

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- · Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

#### **PIN ASSIGNMENT**



Sect. 16, Pgs. 1 & 3

#### **PIN DESCRIPTION**

TAP 1 - TAP 5 - Tap Output Number

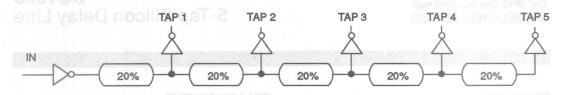
Vcc -+5 Volts
GND - Ground
NC - No Connection
IN - Input

#### DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of  $\pm$  2 ns or  $\pm$  3%, whichever is greater. This device is offered in a standard 14-pin DIP making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. The 14-pin DIP and 8-pin DIP are available in a surface mountable gullwing construction. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC

packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

#### **LOGIC DIAGRAM Figure 1**



PART NUMBER DELAY TABLE (tpHL, tpLH) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1005-60	12ns	24ns	36ns	48ns	60ns
DS1005-75	15ns	30ns	45ns	60ns	75ns
DS1005-100	20ns	40ns	60ns	80ns	100ns
DS1005-125	25ns	50ns	75ns	100ns	125ns
DS1005-150	30ns	60ns	90ns	120ns	150ns
DS1005-175	35ns	70ns	105ns	140ns	175ns
DS1005-200	40ns	80ns	120ns	160ns	200ns
DS1005-250	50ns	100ns	150ns	200ns	250ns

Custom delays available

SND - Ground
NC - No Connection
N - Input
N - Input

packaging, in order to maintain complete pin computibility, DIP packages are available with hybrid lead configurations. The DS 1005 reproduces the input legic level at each tap after the fixed delay apacified by the death number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiopriductor can ingrup to ten 74LS loads. Dallas Semiopriductor can outtomize standard products to meet apacial mode. For special requests and rapid delivery, call (214)

The DS unit filling Silicon Delay Line provides five equally spaced tags with delays ranging from 12.ns to 250 ns, with the service of the consistence of the service of th

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#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current -1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	exceeded; howeve	4.75	5.00	5.25	٧	991
High Level Input Voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.5	٧	1
Low Level Input Voltage	V <sub>IL</sub>	ator under	-0.5		0.8	V	M113
Input Leakage Current	li l	$0.0V \le V_{I} \le V_{CC}$	-1.0	lo sobe	1.0	uА	a sent of
Active Current	Icc	V <sub>CC</sub> = Max; Period = Min.		40	70	mA	2
High Level Output Current	Іон	V <sub>CC</sub> = Min. V <sub>OH</sub> = 4	t out bas	ing edge	-1.0	mA	ant meets
Low Level Output Current	loL	V <sub>CC</sub> = Min. V <sub>OL</sub> = 0.5	12	e galbae	oint on the	mA	bas agb

#### **AC ELECTRICAL CHARACTERISTICS**

 $(t_A = 25^{\circ}C, V_{CC} = 5.0V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	40% of TAP 5 t <sub>PLH</sub>	If noemfool en gai erir to egb	e placed til der traling d	ns ns	despri7
Input to Tap Delay (leading edge)	tPLH	Riso a Pulsa	Table 1	peggla off;	ns	3,4,5,6
Input to Tap Delay (trailing edge)	t <sub>PHL</sub>	Parior	Table 1	an execute gr exacts a colo	ns	3,4,5,6
Power-up Time	t <sub>PU</sub>			100	ms	Legic
I NOTAT a to institutions soft affects	Period	4 (t <sub>WI</sub> )	eminet amil by	nomals adT	ns	7

#### CAPACITANCE

 $t_A = 25^{\circ}C$ 

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	1.000	5	10	pF	

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. V<sub>CC</sub> = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns or ±3%, whichever is greater.
- 4. See Test Conditions.
- 5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional input-to-tap delay shift of ± 1.5ns or ± 4%, whichever is greater.
- 6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.
- 7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

#### **TERMINOLOGY**

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

 $t_{WI}$  (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

 $t_{\mbox{RISE}}$  (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

tFALL (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t<sub>PLH</sub> (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

tpHL (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

#### **TEST SETUP DESCRIPTION**

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### INPUT-

BOIT ZIRETOA	PAROL IN 1
Ambient Temperature	25°C ± 3°C
Supply Voltage (V <sub>CC</sub> )	5.0V ± 0.1V
Input Pulse	High = $3.0V \pm 0.1V$
	Low = $0.0V \pm 0.1V$
Source Impedance	50 ohm maximum
Rise and Fall Time	3.0 ns maximum
Pulse Width	500 ns
Period	1 us

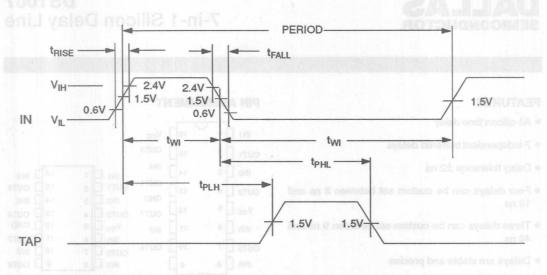
#### **OUTPUT:**

Each output is loaded with the equivalent of a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

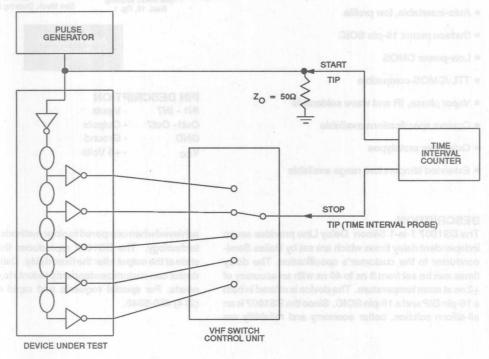
#### NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

# TIMING DIAGRAM-SILICON DELAY LINE Figure 2



# **DALLAS SEMICONDUCTOR TEST CIRCUIT** Figure 3



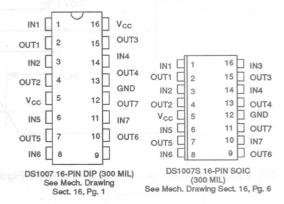


# 7-in-1 Silicon Delay Line

#### **FEATURES**

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance ±2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- · Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes
- Extended temperature range available

#### **PIN ASSIGNMENT**



Also Available In Die Form

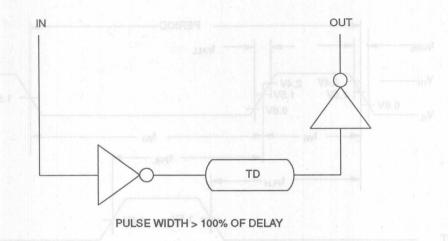
#### PIN DESCRIPTION

#### DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semi-conductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of  $\pm 2$  ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are

achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic state at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

# **LOGIC DIAGRAM** Figure 1

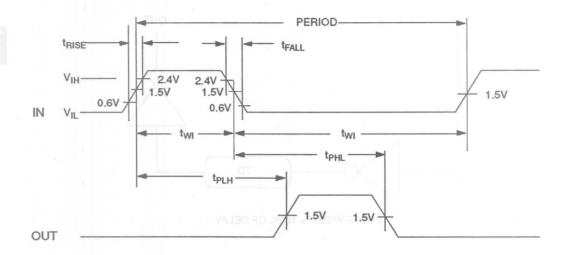


## PART NUMBER DELAY TABLE (tplH) Table 1

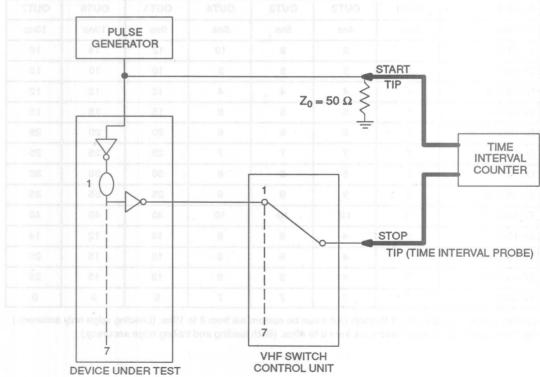
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	. 7	7	7	25	25	25
DS1007-8	8	8	8	- 8	30	30	30
DS1007-9	9	9	9	9	35	35	35
D\$1007-10	10	10	10	10	40	40	40
DS1007-11	3 0 7 8	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10ns. (Leading edge only accuracy.) Out 5 through Out 7 can be custom set from 9 to 40ns. (Both leading and trailing edge accuracy.)

#### **TIMING DIAGRAM SILICON DELAY LINE Figure 2**



# **TEST CIRCUIT** Figure 3



2

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current -1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, \text{V}_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS	NOTES
Supply Voltage	Vcc	ed neewind	4.75	5.00	5.25	٧	DIFFE PER
High Level Input Voltage	V <sub>IH</sub>	A Jinu latineo	2.2	ett to eg	V <sub>CC</sub> +0.5	V	ug ta <b>1</b> a en
Low Level Input Voltage	V <sub>IL</sub>	muntani doga	-0.5		0.8	V	1 <sup>sqlu</sup>
Input Leakage Current	l <sub>l</sub>	0.0V ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0	nd on the	1.0	uA	eaturi) pu
Active Current	Icc	V <sub>CC</sub> = Max; Period= Min.	va. redik gnilled ed	40.0	70.0	mA	2
High Level Output Current	I <sub>OH</sub>	V <sub>CC</sub> = Min. V <sub>OH</sub> = 2.4V	and make and	tel comit by	-1.0	mA	Citar II.
Low Level Output Current	loL	V <sub>CC</sub> = Min. V <sub>OL</sub> = 0.5V	12.0	e agba gri	liested for	mA	10% god th

#### AC ELECTRICAL CHARACTERISTICS

 $(t_A = 25^{\circ}C, V_{CC} = 5V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	100% of t <sub>PLH</sub>	ed time betw	agale eriT :	ns	emi7) <sub>MJ</sub> r
Input to Output (leading edge)	tpLH	tro en	Table 1	a to agou ga a la anha an	ns	3, 4, 5
Power-up Time	t <sub>PU</sub>	on3		100	ms	salug <b>7</b> ugh
o inclever vic. i eth se beluseem	Period	3 (t <sub>WI</sub> )			ns	6

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	iqo 🗆 bes	5	10	pF	a nebriu not

#### NOTES:

- 1. All voltages are referenced to ground,
- 2. Measured with outputs open.
- 3. V<sub>CC</sub> = 5V @2 5°C. Delays accurate on rising edges within ±2 ns.
- See Test Conditions below.
- All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if OUT 2 slows down, all other outputs also slow down).
- 6. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
- 7. tpU = 0 ms for OUT 1 through OUT 4.

#### **TERMINOLOGY**

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t<sub>WI</sub> (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge, and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

 $t_{\mbox{RISE}}$  (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t<sub>FALL</sub> (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

tplH (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

#### TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### INPUT:

**Ambient Temperature:** 

25°C ± 3°C 5.0V ± 0.1V

Supply Voltage (V<sub>CC</sub>): Input Pulse:

High =  $3.0V \pm 0.1V$ 

Low =  $0.0V \pm 0.1V$ 

Source Impedance: Rise and Fall Time: 50 ohm Max. 3.0 ns Max.

Pulse Width: Period: 500 ns 1 μs

#### **OUTPUT:**

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising edge.

#### NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

# **DALLAS**SEMICONDUCTOR

## 10-Tap Silicon Delay Line

#### **FEATURES**

- All-silicon time delay
- 10 taps equally spaced
- · Delays are stable and precise
- · Leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- · Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- · Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

#### **PIN ASSIGNMENT**

IN1	1	14	Vcc				
NC [	2	13	TAP 1	ΙΝΠ	1	16	] V <sub>cc</sub>
TAP 2	3	12	TAP 3	NC	2	15	] NC
TAP 4	4	11	TAP 5	NC	3	14	TAP 1
TAP 6	5	10	TAP 7	TAP 4	4	13	TAP 3
TAP 8	6	9	TAP 9	TAP 6	6	0.11	TAP 7
GND [	7	8	TAP 10	TAP 8 GND	7	10	TAP 9
S	0G 14- (30) ee Med	0 MIL) PIN GUL 0 MIL) h. Drawin , Pgs. 1 8	gs	S	ee Med Sect.	0 MIL) ch. Drawi 16, Pg. 6	10-11-0
		0		Availab ie Form	STATE OF THE PARTY NAMED IN		
		RIPTI 10 – Ta	ON ap Outpi	ut Numb	er		
Vcc		-5	Volts				

- Ground

- Input

- No Connection

#### DESCRIPTION

The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces PC board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy

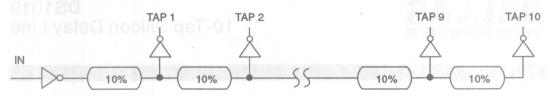
of ±5% or ±2 ns, whichever is greater. The DS1010 reproduces the input logic state at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

GND

NC

IN

#### **LOGIC DIAGRAM** Figure 1



#### PART NUMBER DELAY TABLE (tput, tpt H) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (ns)
DS1010-50	50	5
DS1010-60	60	Tagat 6
DS1010-75	75	7.5
DS1010-80	AT GAT 80	Jagar 8
DS1010-100	100	0иа 10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35 PM D
DS1010-400	400	40
DS1010-450	450	QMO 45
DS1010-500	500	50

Custom delays available.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current

-1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>cc</sub>	CHOMBAR, BODALS	4.75	5.00	5.25	V	1
High Level Input Voltage	V <sub>IH</sub>	or -60 in 16-pin p	2.2	not read	V <sub>CC</sub> +0.5	mex Valled	Sed <b>h</b> io bil
Low Level Input Voltage	V <sub>IL</sub>		-0.5		0.8	٧	1
Input Leakage Current	l <sub>l</sub> .	$0.0V \le V_{I} \le V_{CC}$	-1.0	The Printer	1.0	μА	Co loveling
Active Current	Icc	V <sub>CC</sub> =Max: Period=Min.		40	150	mA	2
High Level Output Current	Іон	V <sub>CC</sub> =Min. V <sub>OH</sub> =4		Lyke	-1.0	mA	W
Low Level Output Current	l <sub>OL</sub>	V <sub>CC</sub> =Min. V <sub>OL</sub> =0.5	12	Flva.r Va.o	V8.1 F	mA	N 100

#### AC ELECTRICAL CHARACTERISTICS

 $(t_A = 25^{\circ}C, V_{CC} = 5V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	40% of TAP 10 t <sub>PLH</sub>	HIM		ns	8
Input to Tap Delay (leading edge)	t <sub>PLH</sub>		Table 1		ns	3,4,5,6,7,9
Input to Tap Delay (trailing edge)	t <sub>PHL</sub>		Table 1		ns	3,4,5,6,7,9
Power-up Time	t <sub>PU</sub>			100	ms	
	Period	4(t <sub>WI</sub> )			ns	8

#### CAPACITANCE

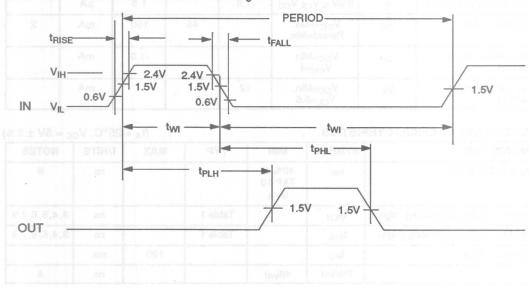
(tA= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	

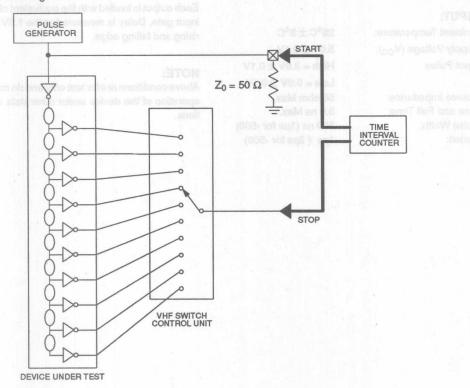
#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. V<sub>CC</sub>= 5V @ 25°C. Input-to-tap delays accurate on both rising and falling edges within ±2 ns or ±5% whichever is greater.
- 4. See "Test Conditions" section.
- 5. For DS1010 delay lines with a TAP 10 delay of 100 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±2ns or ±3%, whichever is greater.
- For DS1010 delay lines with a TAP 10 delay less than 100 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±1 ns or ±9%, whichever is greater.
- 7. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps will also slow dow; TAP 3 can never be faster than TAP 2.
- Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
- 9. Certain high-frequency applications not recommended for -50 in 16-pin package. Consult factory.

#### **TIMING DIAGRAM-SILICON DELAY LINE Figure 2**



#### **TEST CIRCUIT** Figure 3



#### **TERMINOLOGY**

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

 $t_{WI}$  (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

 $t_{\mbox{RISE}}$  (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

 $t_{\rm FALL}$  (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t<sub>PLH</sub> (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and

the 1.5V point on the leading edge of any tap output pulse.

tpHL (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

#### TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### INPUT:

Ambient Temperature:

Supply Voltage (V<sub>CC</sub>):

Input Pulse:

Source Impedance: Rise and Fall Time:

Pulse Width: Period: 25°C ± 3°C

5.0V ± 0.1V

 $High = 3.0V \pm 0.1V$ 

Low =  $0.0V \pm 0.1V$ 50 ohm Max. 3.0 ns Max.

500 ns (1μs for -500) 1μs (2μs for -500)

#### **OUTPUT:**

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

#### NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

# **DALLAS**SEMICONDUCTOR

## 2-in-1 Sub-Miniature Silicon Delay Line with Logic

#### PIN ASSIGNMENT **FEATURES** All-silicon time delay IN1 Vcc оитз П IN2 53 μW max. CMOS quiescent mode OUT1 6 OUT2 Surface mount 8-pin mini-SOIC and standard 8-pin GND 5 OUT4 DS1012 8-PIN DIP (300 MIL) DS1012H 8-PIN GULLWING 2 independent buffered delays per input See Mech. Drawing - Sect. 16, Pgs. 1 & 3 Option of complemented output(s) 8 W Vcc IN1 III 1 · Option of timed AND, NAND, OR, NOR, XOR, OUT3 III 2 7 III IN2 XNOR, HALF-XOR and HALF-XNOR logic outputs OUT1 III 6 III OUT2 5 OUT4 GND III Delay tolerance: ±1.5 ns (delays: 3-10 ns). ±2.0 ns (delays: 11-40 ns) DS1012Z 8-PIN SOIC (150 MIL) See Mech. Drawing - Sect. 16, Pg. 5 Vapor phase, IR and wave solderability Economical Also Available

#### DESCRIPTION

TTL/CMOS-compatible
 Quick turn prototypes

In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. Any of the four outputs can be inverted at the time of manufacture. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration.

Custom delays and logic options available

For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 and  $\overline{D4}$ ), or NOT HALF-XOR ( $\overline{D3}$  OR D4) can be substituted for the simple delay on OUT3. DS1012-2, DS1012-4, and DS1012-5 are examples of

#### PIN DESCRIPTION

IN1, IN2 Inputs
OUT1, OUT2 Outputs (delays)
OUT3, OUT4 Outputs (delays, logic)
GND Ground
VCC +5 volts

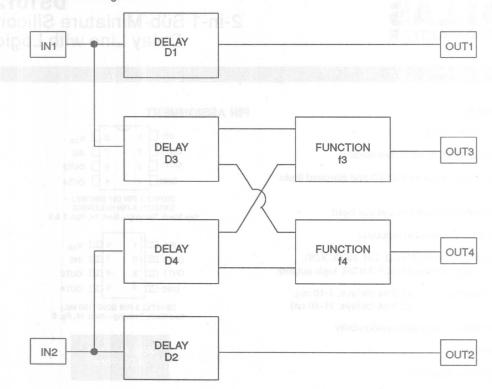
catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In Die Form

In any configuration, delays D1 ( $t_{D1}$ ) and D2 ( $t_{D2}$ ) can be specified within the range of ~3 ns to 10 ns. Delays D3 ( $t_{D3}$ ) and D4 ( $t_{D4}$ ) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is  $\pm 2$  ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (214) 450-5348.

#### **LOGIC DIAGRAM** Figure 1



Function f3 can be one of the following:

D3

D3 AND D4

D3 HALF-XOR D4

Function f4 can be one of the following:

D4

**D3 OR D4** 

D3 XOR D4

D4

D3

D3 NOR D4

D3 NAND D4

D3 HALF-XNOR D4

D3 XNOR D4

NOTE: Any output(s) can be inverted at time of manufacture.

If D1 > 10 ns, D1 = D3.

If D2 > 10 ns, D2 = D4.

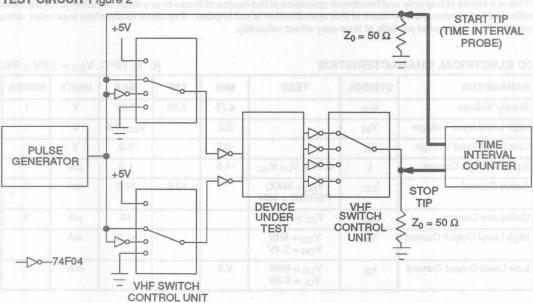
#### PART NUMBER DELAY AND CONFIGURATION Table 1

CATALOG P/N	t <sub>D1</sub> (ns)	t <sub>D2</sub> (ns)	t <sub>D3</sub> (ns)	t <sub>D4</sub> (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	- 5	10	10	D1	D2	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4
DS1012-7	15	4	4	14	D1	D2	D3	D3XD4
DS1012-D16	4	19.6	ol el 4 ighu	19.6	D1	D2	D3.D4	D3XD4
DS1012-D20	4	16.5	4	16.5	D1	D2	D3.D4	D3XD4
DS1012-D25	4	14	4	14	D1	D2	D3.D4	D3XD4
DS1012-D33	4	11.5	4	11.5	D1	D2	D3.D4	D3XD4
DS1012-D50	9734 915	9	4	9	D1	D2	D3.D4	D3XD4
DS1012-V20	25	50	25	50	D1	D2	D3.D4	D3+D4
DS1012-V40	12.5	25	12.5	25	D1 .	D2	D3.D4	D3XD4
DS1012-V50	10	20	10	20	D1	D2	D3.D4	D3XD4
DS1012-V60	8.3	8.3	8.3	8.3	D1	D2	D3.D4	D3+D4

NOTE: . = AND, + = OR, X = XOR, HX = HALF-XOR

Contact Dallas Semiconductor for information on custom configurations and timing delays.

#### **TEST CIRCUIT** Figure 2



#### TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters on the DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

INPUT:

Ambient Temperature: Supply Voltage (Vcc):

25°C ± 3°C 5.0V + 0.1V

Input Pulse:

High =  $3.0V \pm 0.1V$ Low = 0.0V + 0.1V

Source Impedance:

50 ohms max. 3.0 ns max.

Rise and Fall Time: Pulse Width:

3.0 ns ma 50 ns

Period:

50 ns

#### OUTPUT:

Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE:

These conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V

-55°C to +125°C -55°C to 125°C

260°C for 10 seconds

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ} \text{ to } 70^{\circ}\text{C}, V_{CC} = 5.0\text{V} + 5\%)$ 

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.5	V	1
Low Level Input Voltage	VIL	>	-0.5		8.0	V	1
Input Leakage Current	, I <sub>1</sub>	0.0V ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0		1.0	μА	100000
Active Current quite	I <sub>CC1</sub>	V <sub>CC</sub> = MAX; PERIOD = MIN		40.0	70.0	mA	2
Quiescent Current	I <sub>CC2</sub>	V <sub>CC</sub> = MAX.			10	μА	5
High Level Output Current	Іон	$V_{CC} = MIN$ $V_{OH} = 2.4V$			-1.0	mA	
Low Level Output Current	l <sub>OL</sub>	V <sub>CC</sub> = MIN. V <sub>OL</sub> = 0.5V	8.0	Learning	her.	mA	

<sup>\*</sup>This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### AC ELECTRICAL CHARACTERISTICS

(tA = 25°C, VCC	=5V + 5%
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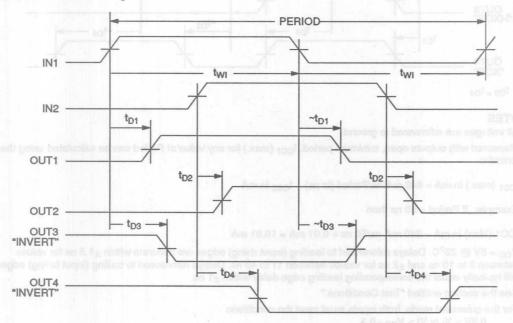
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	/			ns	6
Input to Output (leading edge)	t <sub>D1</sub> , t <sub>D2</sub> , t <sub>D3</sub> , t <sub>D4</sub>				ns	3, 4
Power-up Time	t <sub>PU</sub>			0	ns	7
4	Period	2(t <sub>WI</sub> )			ns	. INC

#### CAPACITANCE

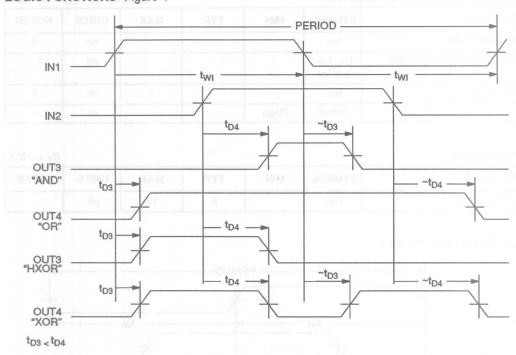
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	

#### **DELAY FUNCTION** Figure 3



#### **LOGIC FUNCTIONS** Figure 4



#### **NOTES**

1. All voltages are referenced to ground.

 Measured with outputs open, minimum period. I<sub>CC1</sub> (max.) for any value of Period can be calculated using the formula:

I<sub>CC1</sub> (max.) in mA = 840 mA-ns/Period (in ns) + I<sub>CC2</sub> in mA

Example: If Period = 50 ns then

ICC1 (Max) in mA = 840 mA-ns/50 ns + 0.01 mA = 16.81 mA

- 3. V<sub>CC</sub> = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
- 4. See the section entitled "Test Conditions."
- 5. For the quiescent mode, both inputs must meet the conditions  $0.3V > V_1$  or  $VI > V_{CC} 0.3$
- 6. For specified accuracy, T<sub>WI</sub> (min) is the longer of 3(t<sub>D1</sub>), 3(t<sub>D2</sub>), 3(t<sub>D2</sub>), or 3(t<sub>D4</sub>). Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., 2(T<sub>WI</sub>) = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when T<sub>WI</sub> is longer than t<sub>D1</sub>, t<sub>D2</sub>, t<sub>D3</sub>, and t<sub>D4</sub>.
- On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V<sub>CC</sub> achieves nominal value.

# **DALLAS**SEMICONDUCTOR

## 3-in-1 Silicon Delay Line

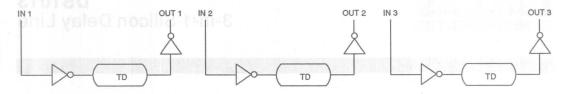
#### **FEATURES** PIN ASSIGNMENT All-silicon time delay 14 Vcc IN 1 16 Vcc 3 independent buffered delays 15 NC NC [ 2 NC 2 13 NC 14 NC NC [ 3 Delay tolerance ±2ns for -10 through -65 IN 2 3 12 OUT 1 13 OUT 1 IN 2 NC [ 5 12 NC Stable and precise over temperature and voltage NC 11 NC 11 OUT 2 IN 3 6 range IN 3 5 10 OUT 2 10 NC NC [ 7 9 OUT3 Leading and trailing edge accuracy on -15 NC GND through -150 **DS1013S 16-PIN SOIC** GND 7 8 OUT3 (300 MIL) Economical See Mech. Drawing DS1013 14-PIN DIP (300 MIL) Sect. 16, Pg. 6 DS1013G 14-PIN GULLWING (300 MIL) Auto-insertable, low profile DS1013K 14-PIN SHEARED NC See Mech. Drawings Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC Sect. 16, Pgs. 1 & 3 IN 1 Vcc Low-power CMOS IN 2 2 7 OUT1 TTL/CMOS-compatible IN 3 6 OUT 2 3 Also Available GND [ In Die Form OUT 3 Vapor phase, IR and wave solderable DS1013M 8-PIN DIP (300 MIL) DS1013H 8-PIN GULLWING (300 MIL) Custom delays available See Mech. Drawings Sect. 16, Pgs. 1 & 3 Quick turn prototypes **PIN DESCRIPTION** Extended temperature ranges available IN 1, IN 2, IN 3 - Inputs OUT 1, OUT 2, OUT 3 - Outputs GND - Ground -+5 Volts Vcc NC - No Connection

#### DESCRIPTION

The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of  $\pm 2$ ns for delay times ranging from 10 ns to 65 ns, in-

creasing to 5% for delays of 150 ns. The DS1013 delay line reproduces the input logic state at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

### **LOGIC DIAGRAM** Figure 1



### PART NUMBER DELAY TABLE (tphL, tplH,) Table 1

PART NO.		DELAY PER OUTPUT (ns)			
DS1013-10*	ar s]sw	10/10/10			
DS1013-12*	NO E A 11	12/12/12 have grade assertion			
DS1013-15	वः इ। इ॥	15/15/15			
DS1013-20	NO 9 ON	20/20/20			
DS1013-25	8 4 000	25/25/25			
DS1013-30	C) THE MITTER STORES	30/30/30			
DS1013-35	Hales Misser Actoreo	35/35/35			
DS1013-40	The same of the sa	40/40/40			
DS1013-45	distribution of the second	45/45/45			
DS1013-50	anklistiyya bala	50/50/50			
DS1013-55		55/55/55			
DS1013-60		60/60/60			
DS1013-65		65/65/65			
DS1013-70**	ONTSIN DESCRIPTION	70/70/70 asdaliave asg			
DS1013-75**	TUO S TUO , TUÖ	75/75/75			
DS1013-80**	OWE	80/80/80			
DS1013-90**	Ok	90/90/90			
DS1013-100**		100/100/100			
DS1013-150***	nh and Mill de maine and	150/150/150			
DS1013-200***	ine reproduces the in	200/200/200			

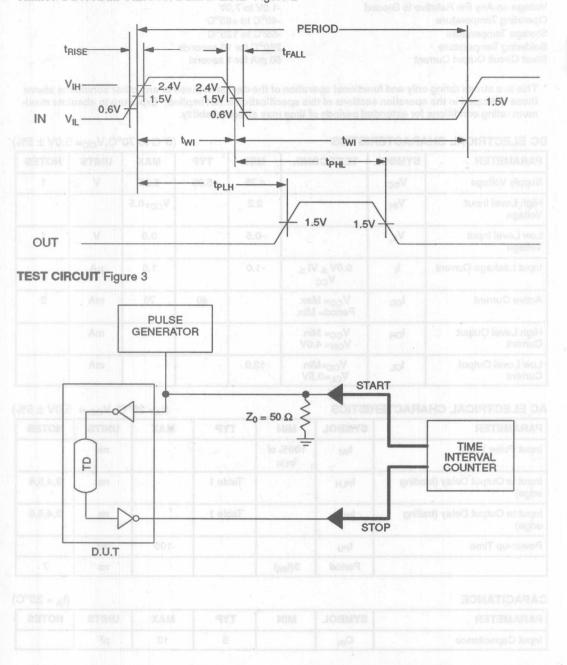
<sup>\*</sup>Leading edge accuracy only.

Custom delays available.

<sup>\*\* ±3%</sup> tolerance.

<sup>\*\*\* ±5%</sup> tolerance.

#### TIMING DIAGRAM-SILICON DELAY LINE Figure 2



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current -1.0V to 7.0V -40°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

#### DC FLECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C.V}_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	-	4.75	5.00	5.25	V	1
High Level Input Voltage	VIH	. va. V	2.2		V <sub>CC</sub> +0.5		
Low Level Input Voltage	V <sub>IL</sub>		-0.5		0.8	V	1
Input Leakage Current	- I <sub>I</sub>	0.0V ≤ VI ≤ V <sub>CC</sub>	-1.0		1.0	μА	and the same
Active Current	Icc	V <sub>CC</sub> = Max Period= Min.		40	70	mA	2
High Level Output Current	ГОН	V <sub>CC</sub> = Min. V <sub>OH</sub> = 4.0V		. 80	-1.0	mA	
Low Level Output Current	l <sub>OL</sub>	V <sub>CC</sub> =Min V <sub>OL</sub> =0.5V	12.0			mA	

#### **AC ELECTRICAL CHARACTERISTICS**

 $(t_A = 25^{\circ}C, V_{CC} = 5.0V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t <sub>WI</sub>	100% of t <sub>PLH</sub>			ns	
Input to Output Delay (leading edge)	t <sub>PLH</sub>		Table 1		ns	3,4,5,6
Input to Output Delay (trailing edge)	t <sub>PHL</sub>		Table 1		ns	3,4,5,6
Power-up Time	t <sub>PU</sub>			100	ms	
	Period	3(t <sub>WI</sub> )			ns	7

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	рF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3.  $V_{CC}$ = 5V @ 25°C. Delays accurate on both rising and falling edges within  $\pm 2$  ns for -15 to -65,  $\pm 3\%$  for -70 to -100 and  $\pm 5\%$  for -150 and longer delays. Delays accurate on rising edge only within  $\pm 2$  ns for -10 and -12.
- 4. See "Test Conditions" section.
- 5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional delay shift of ± 1.5 ns or ± 3%, whichever is greater.
- All output delays tend to vary unidirectionally over temperature or voltage ranges (i.e., if OUT 1 slows down, all other outputs also slow down).
- Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

#### **TERMINOLOGY**

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t<sub>WI</sub> (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t<sub>RISE</sub> (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

 $t_{\sf FALL}$  (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t<sub>PLH</sub> (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

t<sub>PHL</sub> (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the corresponding output pulse.

#### TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between each input and corresponding output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### INPUT:

Ambient Temperature:  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ Supply Voltage (V<sub>CC</sub>):  $5.0\text{V} \pm 0.1\text{V}$ 

Input Pulse: High =  $3.0V \pm 0.1V$ 

Low =  $0.0V \pm 0.1V$ 

Source Impedance: 50 ohms Max.
Rise and Fall Time: 3.0 ns Max.
Pulse Width: 500 ns
Period: 1us

#### **OUTPUT:**

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

#### NOTE

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

2



### DS1020 Programmable 8-Bit Silicon Delay Line

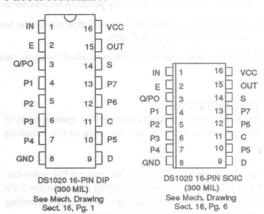
#### **FEATURES**

- All-silicon time delay
- Models with 0.25 ns, 0.5 ns, 1 ns, and 2 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Standard 16-pin DIP or 16-pin SOIC
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Extended temperature range available

#### DESCRIPTION

The DS1020 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The fastest model (-025) offers a maximum delay of 73.75ns with an incremental delay of 0.25ns, while the slowest model (-200) has a maximum delay of 520ns with an incremental delay of 2ns. All models have an inherent (step zero) delay of 10ns. After the user-determined delay, the input logic

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

	Poditil Hall
IN	Delay Input
P0-P7	Parallel Program Pins
GND	Ground
OUT	Delay Output
VCC	+5 Volts
S	Mode Select
E	Enable
C	Serial Port Clock
Q	Serial Data Output
D	Serial Data Input

state is reproduced at the output without inversion. The DS1020 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1020 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC.

#### PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V<sub>CC</sub> and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t<sub>DSE</sub>) and data hold (t<sub>DHE</sub>) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t<sub>EDV</sub> or t<sub>PDV</sub>) is required before input logic levels are accurately delayed.

Since the DS1020 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

#### SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (tDSC) and data hold (tDHC) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (tEDV) is required before the delay is accurate.

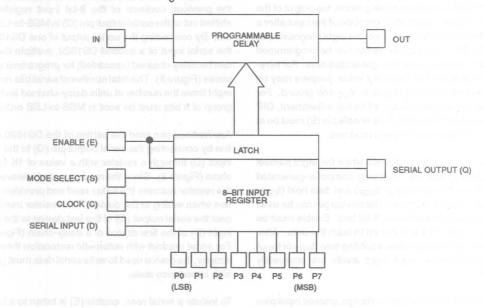
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1020 to the serial input of a second DS1020, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1020 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

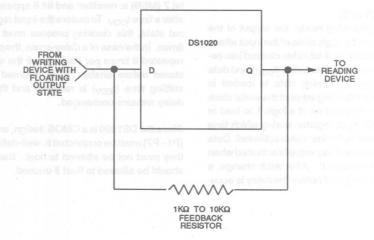
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time ( $t_{EQV}$ ), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 -> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time  $t_{CQV}$ . To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time ( $t_{EDV}$ ) is required and the programmed delay remains unchanged.

Since the DS1020 is a CMOS design, unused input pins (P1-P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

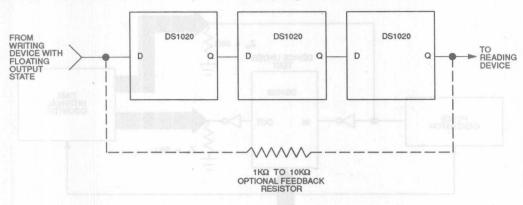
#### FUNCTION BLOCK DIAGRAM Figure 1



### **SERIAL READOUT** Figure 2



### CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



#### **PART NUMBER TABLE** Table 1

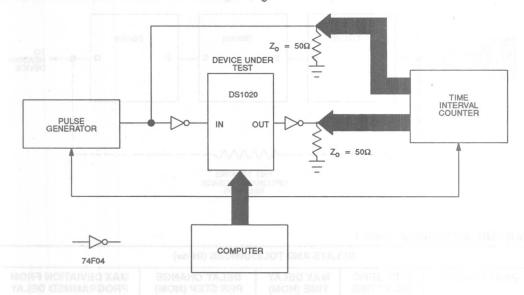
DELAYS AND TOLERANCES (IN ns)										
PART NUMBER	STEP ZERO DELAY TIME	MAX DELAY TIME (NOM)	DELAY CHANGE PER STEP (NOM)	MAX DEVIATION FROM PROGRAMMED DELAY						
DS1020-025	10 ± 2	73.75	0.25	±6						
DS1020-050	10 ± 2	137.5	0.5	±8						
DS1020-100	10 ± 2	265	sanos calus calainese a	±20						
DS1020-200	10±3	520	benusen 2 is sysleb en	T Jordaco e±40 los recorus						

#### **DELAY VS. PROGRAMMED VALUE** Table 2

s (DS1020-080) s (DS1020-100) s (DS1020-200)	STEP				ine	nerduni .aud 88	one div	mated v ir over a	MAX DELAY	PARALLE	SERIAL
BINARY	0	0	0	0	0	0	1	1	1	P7	MSB
PROGRAMMED	0	0	0	0	0	0	1	1	1	P6	11.02.00
VALUE	0	0	0	0	0	0	1	1	1.010/3	P5	Heidin
	0	0	0	0	0	0	1	1	1	P4	Codings
	0	0	0	0	0	0	10-9	1	1	P3	
	0	0	0	0	1	1 39	1amile	1	1 190	P2	- acritico
PART	0	0	1	1 300	0	0	0	1	1	P1	
NUMBER	0	1	0	1	0	1	1	0	1	P0	LSB
DS1020-025	10.00	10.25	10.50	10.75	11.00	11.25	73.25	73.50	73.75		
DS1020-050	10.0	10.5	11.0	11.5	12.0	12.5	136.5	137.0	137.5		
DS1020-100	10	11	12	13	14	15	263	264	265		
DS1020-200	10	12	14	16	18	20	516	518	520		

All delays in nanoseconds, referenced to input pin.

#### DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



#### **TEST SETUP DESCRIPTION**

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1020. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1020 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

Rise and Fall Time:	3.0 ns max.					
	(measured between	n				
	0.6V and 2.4V)					
Pulse Width:	500 ns (DS1020-	025)				
	2 μs (DS1020-	050)				
	4 μs (DS1020-	100)				
	4 μs (DS1020-	200)				
Period:	1 μs (DS1020-	025)				
	4 μs (DS1020-	050)				
	8 μs (DS1020-	100)				
	8 μs (DS1020-	200)				

TEST CONDITIONS INPUT:	
Ambient Temperature:	25°C ± 3°C
Supply Voltage (V <sub>CC</sub> ):	5.0V ± 0.1V
Input Pulse:	High = $3.0V \pm 0.1V$
	$Low = 0.0V \pm 0.1V$
Source Impedance:	50 ohms max.

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

#### OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature
Short Circuit Output Current

-1.0V to 7.0V 0°C to +85°C -55°C to 125°C 260°C for 10 seconds 50 mA for 1 second

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	TEST CONDITION	MIN	ТҮР	MAX	UNITS	NOTES
Supply Voltage	Vcc	Debat	4.75	5.00	5.25	٧	1
High Level Input Voltage	VIH	wiete?	2.2		V <sub>CC</sub> +0.5	٧	1 of high
Low Level Input Voltage	V <sub>IL</sub>	(4,4)(0	-0.5	ig .	0.8	٧	ne'l luoni
Input Leakage Current	I <sub>1</sub>	0 ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0		1.0	μА	
Active Current	Icc	V <sub>CC</sub> = MAX; PERIOD = 1 μs			30.0	mA	10 A 1A
High Level Output Current	Іон	V <sub>CC</sub> = MIN V <sub>OH</sub> = 2.7V	2061	IVE	-1.0	mA	eC tuoni
Low Level Output Current	l <sub>OL</sub>	V <sub>CC</sub> = MIN. V <sub>OL</sub> = 0.5V	12.0			mA	

#### AC ELECTRICAL CHARACATERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	fc			10	MHz	
Enable Width	t <sub>EW</sub>	50	H VAS	VA.S.	ns	HV.
Clock Width	t <sub>CW</sub>	50	Va.o		ns	W M
Data Setup to Clock	t <sub>DSC</sub>	30			ns	
Data Hold from Clock	tDHC	10			ns	
Data Setup to Enable	t <sub>DSE</sub>	30			ns	
Data Hold from Enable	tDHE	10	HL9		ns	
Enable to Serial Output Valid	t <sub>EQV</sub>	.//		50	ns	
Enable to Serial Output High Z	t <sub>EQZ</sub>	0		50	ns	gwr
Clock to Serial Output Valid	tcav			50	ns	
Clock to Serial Output Invalid	tcax	10			ns	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

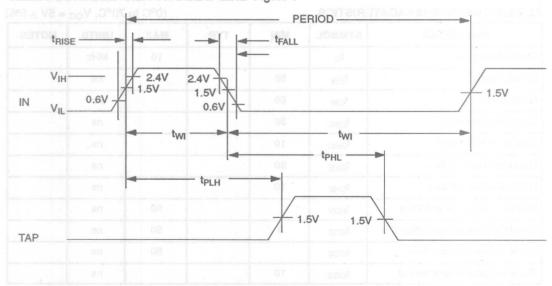
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Enable Setup to Clock	t <sub>ES</sub>	50			ns	
Enable Hold from Clock	t <sub>EH</sub>	50			ns	T NEW Y
Parallel Input Valid to Delay Valid	t <sub>PDV</sub>	Petroc		50	μѕ	
Parallel Input Change to Delay Invalid	t <sub>PDX</sub>	ation o the	ctional oper ections of thi	nal brim visa na nasha	ns	
Enable to Delay Valid	t <sub>EDV</sub>			50	μѕ	
Enable to Delay Invalid	t <sub>EDX</sub>	0	emes	REACTER	ns	maja c
V <sub>CC</sub> Valid to Device Functional	t <sub>PU</sub>	12	FT   1	100	ms	1-4-
Input Pulse Width	t <sub>WI</sub>	100% of Output Delay	COND	LSV	ns	
Input to Output Delay	t <sub>PLH</sub> , t <sub>PHL</sub>		Table 2	MIY	ns	2
Input Period	Period	3(t <sub>WI</sub> )		117	ns	4

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	4472	- HOA	10	pF	

### TIMING DIAGRAM: SILICON DELAY LINE Figure 5



#### **TERMINOLOGY**

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

two (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

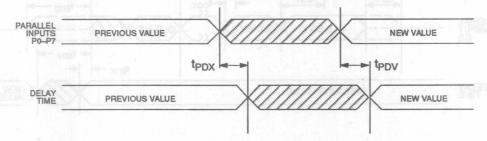
 $t_{\mbox{RISE}}$  (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

 $t_{\sf FALL}$  (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

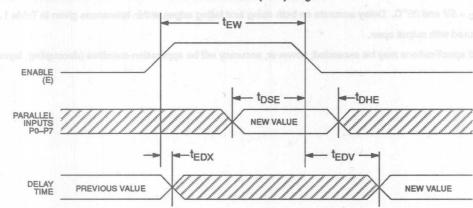
tpLH (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

tpHL (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

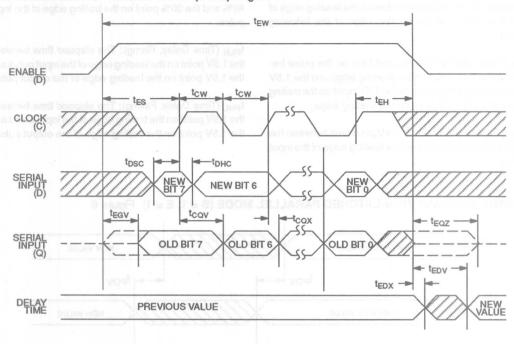
#### TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



#### TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



#### TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



#### **NOTES**

- 1. All voltages are referenced to ground.
- 2. @V<sub>CC</sub> = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.
- 3. Measured with output open.
- Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

## **DS1040** Programmable One-Shot Pulse Generator

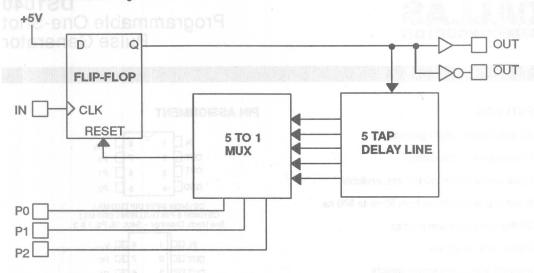
FEATURES			PIN A	SSIGNMENT			
All-silicon pulse width gene	rator				IN 1	8 Vcc	
• Five programmable widths				OUT 2	7 P0		
Equal and unequal increme	Equal and unequal increments available						
<ul> <li>Maximum pulse widths from</li> </ul>	n 50 ns 1	to 500 ns			DS1040M 8-PIN		
Widths are stable and prec	ise				DS1040H 8-PIN GU See Mech. Drawings -		
					IN III 1	8 W Vcc	
Rising edge-triggered					OUT III 2	7 III P0	
<ul> <li>Inverted and non-inverted of</li> </ul>	outputs				OUT III 3	6 III P1	
• Width tolerance ±5% or ±2	ns. whic	hever is	greater		GND III 4	5 III P2	
Economical	ŧ				DS1040Z 8-PIN See Mech. Drawing		
Auto-insertable, low profile					Also Av	ailable	
Low-power CMOS					n Die	Form	
TTL/CMOS-compatible					0 09	- 80,1	
Vapor phase, IR and wave	solderab	ole		PIN DI	ESCRIPTION		
Custom widths available				IN	Trigger Input		
Fast turn prototypes				P0-P2 GND	Programming F Ground	ins	
150 150 150	120	90		OUT	Pulse Output		
<ul> <li>Extended temperature range</li> </ul>	e availa	ble		OUT	Inverted Pulse	Output	
				Vcc	+5V		
DESCRIPTION							

The DS1040 Pulse Generator is a user-programmable one-shot with a choice of five precise pulse widths. Maximum widths range from 50 ns to 500 ns; increments range from 2.5 ns to 100 ns. For maximum flexibility in applications such as magneto-optical read/write disk laser power control, varieties are offered with equal and unequal increments. The DS1040 is offered in standard 8-pin DIPs and 8-pin mini-SOICs. Low cost and superior reliability over hybrid technology are achieved by the combination of a 100% CMOS silicon design and industry standard packaging. The DS1040 series of pulse generators provide a nominal width accuracy of +5% or

± 2 ns, whichever is greater. In response to the rising edge of the input (trigger) pulse, the DS1040 produces an output pulse with a width determined by the logic states of the three parallel programming pins. For convenience, both inverting and non-inverting outputs are supplied. The intrinsic delay between the trigger pulse and the output pulse is no more than 10ns. Each output is capable of driving up to five 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special request and rapid delivery, call (214) 450-5348.

### **LOGIC DIAGRAM** Figure 1



### PULSE WIDTH VS. PROGRAMMED VALUE Table 1

. 8	PROGRAMMING PINS		MAX WIDTH	MIN	$\longrightarrow$			MAX WIDTH	MAX WIDTH	MAX WIDTH
	MSB P2	P2	0	0	0	0	1	1	1	1
		P1	0	0	-1	1	0	0	0.1	1.
	LSB	P0	0	1	0	1	0	1	0	1
PART NUMBER		иопъ	ROSBO	per .		o.	fareblos	8217 W (20)		1120
DS1040-75		mont re	75	15	30	45	60	75	75	75
DS1040-100	. 10214	per Fernisarios	100	20	40	60	80	100	100	100
DS1040-150		ruqasO e	150	30	60	90	120	150	150	150
DS1040-200	tuqibO	estay ber	200	40	80	120	160	200	200	200
DS1040-250			250	50	100	150	200	250	250	250
DS1040-500			500	100	200	300	400	500	500	500
DS1040-B50	aver in resp	eng si sovi	50	30	35	40	45	50	50	50
DS1040-D60	meteb dibiv	v o ritivo es	60	20	30	40	50	60	60	60
DS1040-A15	amengora is	itensq ear	15	5	2.5	10	12.5	15	15	15
DS1040-A20	MHIDH DAS	grimweni i	20	10	12.5	15	17.5	20	20	20
DS1040-A32	nurth chain (	pulse is no	32.5	22.5	25	27.5	30	32.5	32.5	32.5
DS1040-B40	o five 74LS	de Suivit	40	20	25	30	35	40	40	40
DS1040-D70			70	30	40	50	60	70	70	70

All times in nanoseconds.

Custom pulse widths available.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature Short Circuit Output Current

-1.0V to +7.0V -40°C to +85°C -55°C to +125°C 260°C for 10 seconds 50mA for 1 second

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC} = 5.0V \pm 5\%$ )

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	ce seven lilw 001	4.75	5.00	5.25	V	Vest .
High Level Input Voltage	V <sub>IH</sub>	data shoot.	2.2	edt is acu	V <sub>CC</sub> + 0.5	lono <b>V</b>	rest .
Low Level Input Voltage	V <sub>IL</sub>		-0.5	2	0.8	IAROAI	аныя
Input Leakage Current		0.0 ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1.0		1.0	μА	9-09
Active Current	Icc	V <sub>CC</sub> = Max; Period = Min		35	75	mA	2,6
High Level Output Current	ОН	V <sub>CC</sub> = Min V <sub>OH</sub> = 4	0	MR39 -	-1	mA	
Low Level Output Current	lou	V <sub>CC</sub> = Min V <sub>OL</sub> = 0.5	8	THINA		mA	m <sup>1</sup>

#### **AC ELECTRICAL CHARACTERISTICS**

 $(t_A = 25^{\circ}C, V_{CC} = 5.0V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Setup	tps	5	ψį	-5-4-0	ns	
Programming Hold	t <sub>PH</sub>	0			ns	
Input Pulse Width at Logic 1	twiH	5	470.0	N	ns	
Input Pulse Width at Logic 0	twiL	5			ns	TUO
Intrinsic Delay	t <sub>D</sub>	0	5	10	ns	antis, quantitative
Output Pulse Width	two	- OX3	Table 1	- of	ns	3,4,5,7
Power-up Time	t <sub>PU</sub>			100	ms	
Period	Period	two + 50	1/		ns	77.05

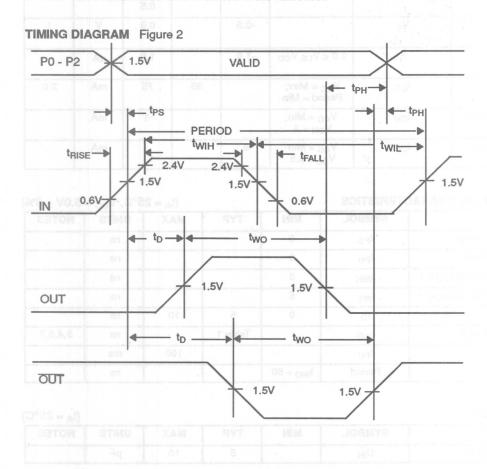
#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

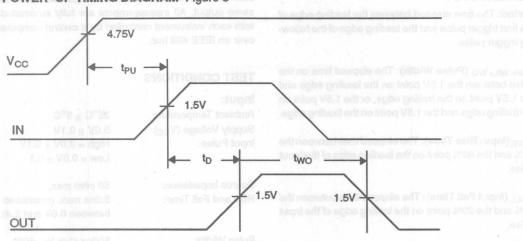
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	

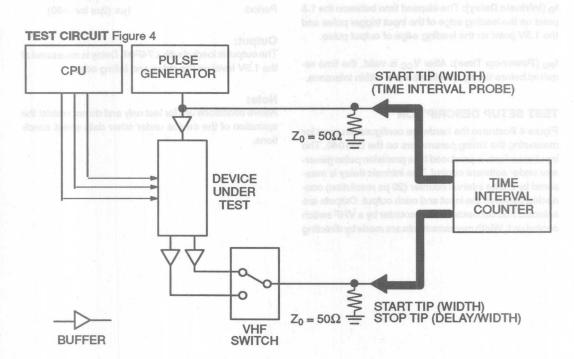
#### NOTES

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open, minimum period.
- 3. V<sub>CC</sub> = 5V @ 25°C. Width accurate to within ± 2 ns or 5%.
- Temperature variations between 0°C and 70°C may increase or decrease width by an additional ±1 ns or ±3%, whichever is greater.
- 5. For DS1040 pulse generators with maximum widths less than 50ns, temperature variations between  $0^{\circ}$ C and  $70^{\circ}$ C may increase or decrease width by  $\pm$  1ns or  $\pm$  9%, whichever is greater.
- I<sub>CC</sub> is a function of frequency and maximum width. Only a pulse generator operating with 40 ns period and V<sub>CC</sub> = 5.25V will have an I<sub>CC</sub> = 75mA. For example, a -100 will never exceed 30mA, etc.
- 7. See "Test Conditions" sections at the end of this data sheet.



#### POWER -UP TIMING DIAGRAM Figure 3





#### **TERMINOLOGY**

**Period:** The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following trigger pulse.

t<sub>WIH</sub>, <sub>WIL</sub>, <sub>WO</sub> (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t<sub>RISE</sub> (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t<sub>FALL</sub> (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t<sub>D</sub> (Intrinsic Delay): The elapsed time between the 1.5 point on the leading edge of the input trigger pulse and the 1.5V point on the leading edge of output pulse.

t<sub>PU</sub> (Power-up Time): After V<sub>CC</sub> is valid, the time required before timing specifications is within tolerance.

#### **TEST SETUP DESCRIPTION**

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1040. The input waveform is produced by a precision pulse generator under software control. The intrinsic delay is measured by a time interval counter (20 ps resolution) connected between the input and each output. Outputs are selected and connected to the counter by a VHF switch control unit. Width measurements are made by directing

both the start and stop functions of the counter to the same output. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

#### **TEST CONDITIONS**

#### Input:

Input Pulse:

Ambient Temperature: Supply Voltage (V<sub>CC</sub>):

5.0

 $25^{\circ}C \pm 3^{\circ}C$  $5.0V \pm 0.1V$ 

High =  $3.0V \pm 0.1V$ Low =  $0.0V \pm 0.1$ 

Source Impedance:

50 ohm max.

Rise and Fall Time:

3.0ns max. (measured between 0.6V and 2.4)

Detwe

Pulse Width: Period: 500ns (1μs for -500) 1μs (2μs for -500)

#### Output:

The output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

#### Note:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

**General Information** 

Silicon Timed Circuits

### **Multiport Memory**

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

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# DALLAS

3-Wire to Bytewide Converter Chip

#### **FEATURES**

- Adapts JEDEC bytewide memory to a 3-wire serial port
- Supports 512K bytes of memory
- 68-pin version provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- Available in 44- or 80-pin quad flat pack for high density requirements

#### **ORDERING INFORMATION**

DS1280FP-XX -80 80-pin Flat Pack -44 44-pin Flat Pack

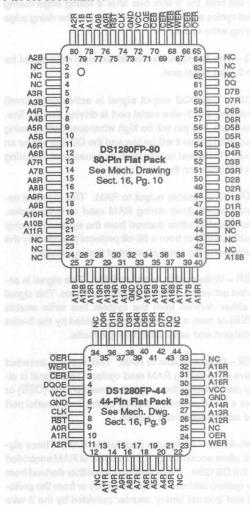
#### PIN DESCRIPTION

RST Reset For Serial Port DQ Data Input/Output For Serial Port CLK Clock Input For Serial Port DQE Serial Port Active Output CEB System Bus Enable System Bus Read Enable OEB WEB System Bus Write Enable A0B-A18B System Address Bus D0B-D7B System Data Bus CER RAM Chip Enable **RAM Write Enable** OER RAM Output Enable AOR-A18R RAM Address Bus DOR-D7R **RAM Data Bus** GND Ground Vcc +5 Volts

#### DESCRIPTION

The DS1280 adds a 3-wire serial port to a bytewide static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and bytewide port is accomplished by handshaking or using predict-

#### **PIN ASSIGNMENT**



able idle time as an access window. The serial port requires a 6-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmission for error.

#### PIN DESCRIPTION

RST – The 3-wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK – The clock input signal is used to input or extract data from the 3-wire serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven out onto the 3-wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ – The DQ signal is the bidirectional data signal for the 3-wire serial port.

DQE – The DQE output signal is active (high level) whenever the 3-wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

CER – Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable (CEB) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

WER – Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable (WEB) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

OER – Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable (OEB) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

A0R-A18R — Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3-wire serial port and associated timing circuits.

DOR-D7R - Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external bytewide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3-wire serial port and associated timing circuits.

CEB – System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM (68-pin package only).

**OEB** – System bus output enable (read) for transfer of data from RAM to the parallel system bus (68-pin package only).

WEB – System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM (68-pin package only).

A0B-A18B - System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM (68-pin package only).

**DOB-D7B** – System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM (68-pin package only).

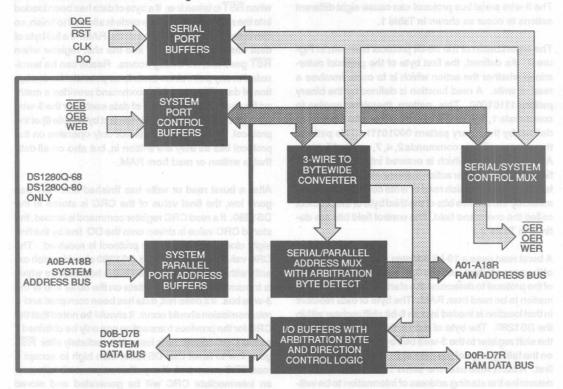
Vcc - +5volt power from the DS1280 (2 pins).

GND - Ground for the DS1280 (2 pins).

#### **OPERATION**

Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections: a 3-wire to bytewide converter and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3-wire serial port or a bytewide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3-wire to bytewide converter. The 3-wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3-wire to bytewide converter.

# **DS1280 BLOCK DIAGRAM Figure 1**



#### SYSTEM BYTEWIDE PARALLEL BUS

If the RST signal for the 3-wire serial port is low (inactive), the bytewide parallel port can access associated RAM directly. The bytewide parallel bus addresses (A0B-A18B) and control signals (CEB, OEB and WEB) are buffered by the DS1280 and become outputs A0R-A18R, CER, OER, and WER respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the bytewide parallel bus to RAM when CEB and WEB inputs are both active (low). The OEB signal is a "don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when CEB and OEB signals are both low and WEB is high.

#### **3-WIRE SERIAL BUS**

If the RST signal for the 3-wire serial port is active (high). the 3-wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3-wire to bytewide converter uses a 56-bit protocol written serially using RST, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered into the 3-wire while RST is high on the low-to-high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last eight bits of the 56-bit protocol are a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56-bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

## **PROTOCOL: 3-WIRE SERIAL BUS**

The 3-wire serial bus protocol can cause eight different actions to occur as shown in Table 1.

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7, and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2.

A burst read uses a 19-bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an 8-bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3-wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19-bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3-wire bus into an 8-bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte-by-byte basis, automatically incrementing the selected address by one location for each successive byte.

#### **PROTOCOL COMMANDS** Table 1

- 1. Burst read
- 2. Burst write
- 3. Read protocol select bits
- 4. Write protocol select bits
- Burst read masking portions of the protocol select bits
- 6. Read CRC register
- 7. Set the address arbitration byte location
- 8. Poll arbitration byte for status and control

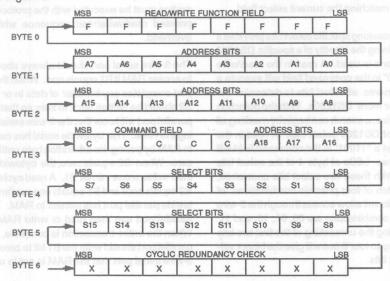
Termination of a current operation will occur at any time when RST is taken low. If a byte of data has been loaded into the shift register, a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when RST goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the protocol. The 8-bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM.

After a burst read or write has finished and RST has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3-wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the CRC for the previous transaction can only be obtained if a read CRC command is issued immediately after RST goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever RST goes low again, destroying the CRC value of interest. Generation of the CRC byte by the external unit on the 3-wire bus will be covered later in this data

#### **CONTROL FIELD** Table 2

00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 7FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

# **PROTOCOL** Figure 2



In any 2-port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports.

Two commands are used by the 3-wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel bytewide port, a command is added to move the arbitration byte to either address location "00000" or address location "7FFFF." When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 7FFFF in addition to accessing the arbitration byte.

The second command used by the 3-wire serial port provides for polling of the arbitration byte to determine

the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed readwrite-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56-bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111) and the correct command field.

Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, multiple DS1280s can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have multiple DS1280s in use and uniquely identify each. A read can occur suc-

cessfully without knowing the select bits but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS1280 when more than one is used. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of one or more DS1280s. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (see Figure 3). With these two select bits unmasked, only an exact match of four possible combinations of these two select bits will allow access through the 3-wire port to RAM. The combinations are 00, 01, 10, and 11. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits.

Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. Repetition of unmasking select bit pairs will yield an exact match of 65,536 possible DS1280s in no more than 32 attempts.

#### **ARBITRATION**

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3-wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 7FFFF as determined by the protocol input from the 3-wire serial port. The arbitration byte has special restrictions and disciplines so that the 3-wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4.

As defined, the 3-wire serial port can read the whole byte but can only write bits S2-S0. The bytewide parallel port can read the whole byte but can only write bits B1-B0. An internal counter controls bits C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3-wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3-wire serial port should then write a one into bit S2. After the write of bit S2, the 3-wire serial port should then read the

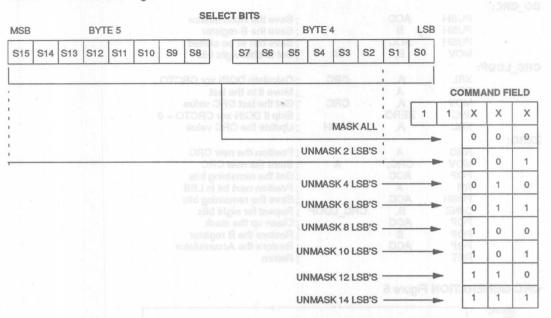
arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read/write/read sequence which minimizes overhead.

The 3-wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3-wire serial port completes any transfer of data to or from RAM, bit S2 should be written back to zero so that the bytewide parallel port will know that the 3-wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signaling the 3-wire serial port that the RAM is not in use.

The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information, making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a port desires access to RAM or the amount of RAM written. Another method of arbitration between the 3-wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3-wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3-wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3-wire port.

Since the 3-wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3-wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3-wire clock input. Essentially the 3-wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3-wire serial port.

# **SELECT BITS MASK** Figure 3



# **ARBITRATION BYTE Figure 4**

MSB					T-B-		LSB
P1	P0	S2	S1	SO	C2	C1	CO
PARALLEL BUS STATUS BITS	NOT USED	SERIAL PORT STATUS BITS	NOT USED	NOT USED	COUNT	COUNT	COUNT

# **CRC GENERATION**

The logic involved in CRC generation is shown in Figure 5. It is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and, at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire serial bus.

The reset signal (RSB) must be high while the CRC generator is being used, as an inactive state will disable the 8-bit shift register. This signal is the same as the reset

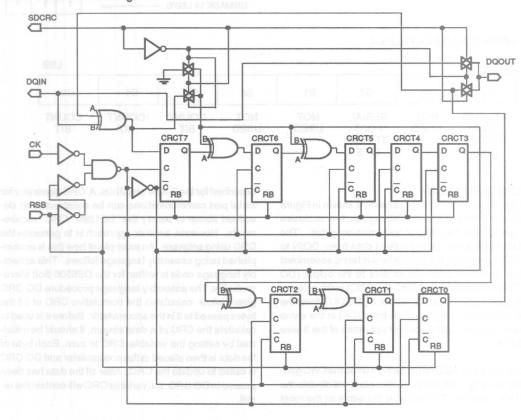
described for the 3-wire serial bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

# **CRC GENERATION LOGIC Table 3**

100	_	0	-	0-
1.7	•		н	

DO_Chc.				
	PUSH	ACC		; Save the Accumulator
	PUSH	В		; Save the B register
	PUSH	ACC		; Save bits to be shifted
	MOV	B,	#8	; Set to shift eight bits
CRC LOOP:	-			i i i i i i i i i i i i i i i i i i i
_	XRL	Α,	CRC	: Calculate DQIN xor CRCTO
	RRC	Α		: Move it to the last
	MOV	Α,	CRC	; Get the last CRC value
	JNC	ZERO		; Skip if DQIN xor CRCTO = 0
	XRL	Α,	0CCH	; Update the CRC value
ZERO:				
	RRC	Α		; Position the new CRC
	MOV	CRC.	A	: Store the new CRC
	POP	ACC		: Get the remaining bits
	RR	A		; Position next bit in LSB
	PUSH	ACC		; Save the remaining bits
	DJNZ	В,	CRC_LOOP	; Repeat for eight bits
	POP	ACC	0110_2001	; Clean up the stack
	POP	В		; Restore the B register
	POP	ACC		; Restore the Accumulator
	RET	700		: Return
	DE			. netuiii

# **CRC GENERATION** Figure 5



#### **ABSOLUTE MAXIMUM RATINGS\***

ADDOCED IE INDIVINION INTERIOR	
Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to+125°C
Soldering Temperature	260°C for 10 seconds

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# RECOMMENDED DC OPERATING CONDITIONS

(ta=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	Vcc	4.5	5.0	5.5	٧	1500
Logic 1	V <sub>IH</sub>	2.0	In shor be	V <sub>CC</sub> +0.3V	A DE AHA	Negatired a
Logic 0	V <sub>IL</sub>	-0.3		+0.8	A	10001

# DC ELECTRICAL CHARACTERISTICS (t<sub>A</sub>=0°C to 70°C; V<sub>CC</sub>=+5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	gs assidit ricitiv	e coeiāln mu	söllug ever	ano to me	μА	9
Output Leakage	LOS 10 20	ook frequen	o mumbosn	s is because	μА	Authitustion
Output Current @ 2.4V	I <sub>OH</sub>	-1			mA	
Output Current @ 0.4V	THE IOL LAND	+2	MISPER	RT ATAG E	mA O	AID BHIN
Supply Current	l <sub>CC1</sub>			15	mA	2
Supply Current	I <sub>CC2</sub>			50	mA	3

## AC ELECTRICAL CHARACTERISTICS

(Vac-5V+10%: 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	T Th		ns	4
Data to CLK Hold	<sup>t</sup> CDH	40			ns	4
Data to CLK Delay	tcdd			125	ns	4,5,6
CLK Low Time	t <sub>CL</sub>	500	1111	Hao'_p	ns	4
CLK High Time	t <sub>CH</sub>	500	W	FITTEN	ns	4
CLK Frequency	fclk	DC	N/	V77 <b>1</b> 57.7	MHz	4,10
CLK Rise & Fall Time	t <sub>R</sub> t <sub>F</sub>			100	ns	
RST to CLK Setup	tcc	1			μs	4
CLK to RST Hold	t <sub>CCH</sub>	40			ns	4
RST Inactive Time	tcwH	125			ns	4
RST to D/Q High Z	t <sub>CDZ</sub>			50	ns	4,6
Serial Port Active	t <sub>DI</sub>			25	ns	4,6
Serial Port Inactive	t <sub>DI</sub>			25	ns	4,6
Parallel Port Propagation	t <sub>PD</sub>		12	20	ns	4,6,8

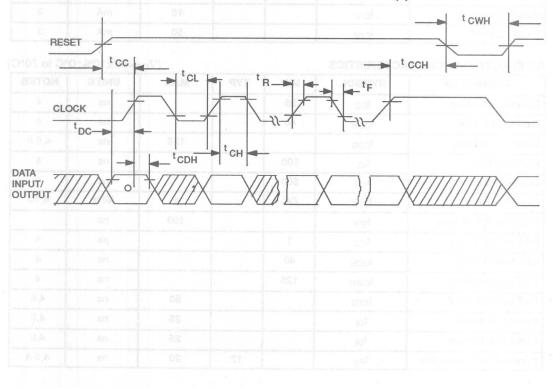
## CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	-67 O*88-		10	pF	1 1985
Output Capacitance	C <sub>OUT</sub>			15	pF	

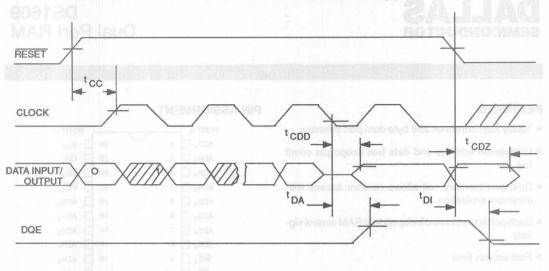
# NOTES

- 1. All voltages are referenced to ground.
- 2. I<sub>CC1</sub> is measured with all outputs open and both the 3-wire serial port or the bytewide parallel port inactive.
- 3. I<sub>CC2</sub> is measured with all outputs open.
- 4. Measured at  $V_{IH} = 2.0 \text{ V}$  or  $V_{IL} = 0.8 \text{V}$  and 10ns maximum rise and fall time.
- 5. Measured at  $V_{OH}$ = 2.4 V and  $V_{OL}$  = 0.4V.
- 6. Measured with a load capacitance of 50 pF.
- 7. The 3-wire serial port will correctly read and write any static RAM with an effective access time of 200ns.
- 8. Propagation delay is the same for data going either way on the bytewide parallel bus.
- 9. Pins A0B through A18B, RST, DQ, CEB have pulldown resistors which will leak approximately 50 μA.
- 10. Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symmetrical waveform.

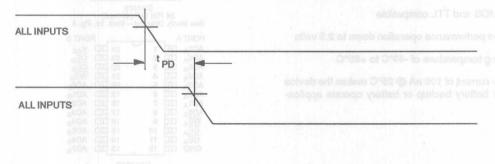
# TIMING DIAGRAM-WRITE DATA TRANSFER 3-WIRE SERIAL PORT (7)



# TIMING DIAGRAM-READ DATA TRANSFER 3-WIRE SERIAL PORT (7)



# 



121891 11/11

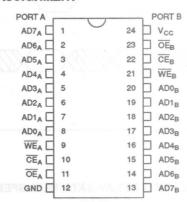


# Dual Port RAM

#### **FEATURES**

- Totally asynchronous 256 byte dual port memory
- Multiplexed address and data bus keeps pin count low
- Dual port memory cell allows random access with minimum arbitration
- Each port has standard independent RAM control signals
- Fast access time
- Low power CMOS design
- 24 pin DIP or 24 pin SOIC surface mount package
- Both CMOS and TTL compatible
- Reduced performance operation down to 2.5 volts
- Operating temperature of -40°C to +85°C
- Standby current of 100 nA @ 25°C makes the device ideal for battery backup or battery operate applications.

#### **PIN ASSIGNMENT**



DS1609 24 PIN DIP (600 mil) See Mech. Drawing – Sect. 16, Pg. 4

PORT	Α ,				P	ORT B
AD7A	田	/1	$\circ$	24	Ш	Vcc
AD6A		2		23	Ш	OEB
AD5A	Ш	3		22	Ш	CEB
AD4A	Ш	4		21		WEB
AD3A	Ш	5		20	Ш	AD0 <sub>B</sub>
AD2A		6		19	$\Box$	AD1 <sub>B</sub>
AD1A	Щ	7		18	Ш	AD2 <sub>B</sub>
ADO <sub>A</sub>	Щ	8		17	Ш	AD3 <sub>B</sub>
WEA		9		16	Ш	AD4 <sub>B</sub>
CEA	Щ	10			Ш	AD5 <sub>B</sub>
OEA	Щ	11			Ш	AD6 <sub>B</sub>
GND		12		13 [	Ш	AD7 <sub>B</sub>

DS1609S 24 PIN SOIC (300 mil) See Mech. Drawing - Sect. 16, Pg. 6

#### **PIN DESCRIPTION**

 Vcc
 - +5 volt supply

 GND
 - Ground

 AD0-AD7
 - Port address/data

 CE
 - Port enable

 OE
 - Output enable

 WE
 - Write enable

#### DESCRIPTION

The DS1609 is a random access 256 byte dual port memory designed to connect two asyncronous address/data buses together with a common memory element. Both ports have unrestricted access to all 256 bytes of memory and with modest system discipline no arbitration is required. Each port is controlled by three

control signals: output enable, write enable, and port enable. The device is packaged in plastic 24 pin DIP and 24 pin SOIC. Output enable access times of 35 ns are available when operating at 5 volts. Reduced performance operation at reduced voltage can be achieved down to 2.5 volts.

# OPERATION - READ CYCLE

The main elements of the dual port RAM are shown in Figure 1.

A read cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ( $\overline{CE}$ ) is then transitioned low. This control signal causes address to be latched internally. Addresses can be removed from the bus provided address hold time is met. Next, the output enable control ( $\overline{OE}$ ) is transitioned low, which begins the data access portion of the read cycle. With both  $\overline{CE}$  and  $\overline{OE}$  active low, data will appear valid after the output enable access time  $t_{OEA}$ . Data will remain valid as long as both port enable and output enable remains low. A read cycle is terminated with the first occurring rising edge of either  $\overline{CE}$  or  $\overline{OE}$ . The address/data bus will return to a high impedance state after time  $t_{CEZ}$  or  $t_{OEZ}$  as referenced to the first occurring rising edge.  $\overline{WE}$  must remain high during read cycles.

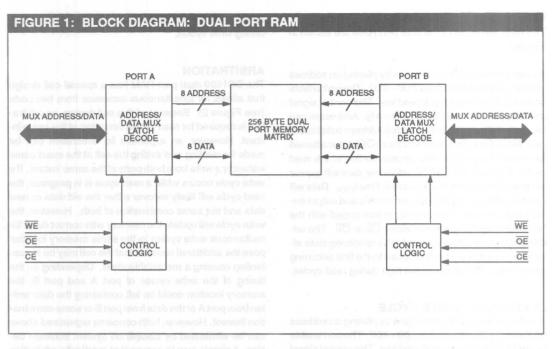
# **OPERATION - WRITE CYCLE**

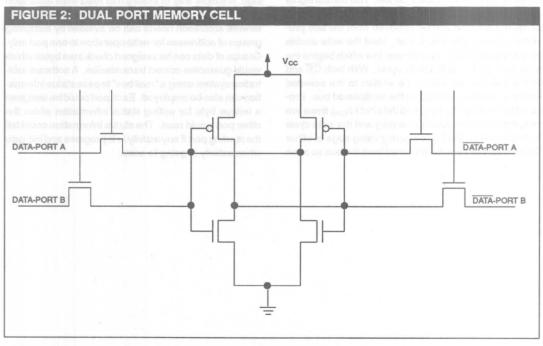
A write cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ( $\overline{CE}$ ) is then transitioned low. This control signal causes address to be latched internally. As with a read cycle, the address can be removed from the bus provided address hold time is met. Next the write enable control signal ( $\overline{WE}$ ) is transitioned low which begins the write data portion of the write cycle. With both  $\overline{CE}$  and  $\overline{WE}$  active low the data to be written to the selected memory location is placed on the multiplexed bus. Provided that data setup ( $t_{DS}$ ) and data hold ( $t_{DH}$ ) times are met, data is written into the memory and the write cycle is terminated on the first occurring rising edge of either  $\overline{CE}$  or  $\overline{WE}$ . Data can be removed from the bus as soon

as the write cycle is terminated.  $\overline{OE}$  must remain high during write cycles.

#### **ARBITRATION**

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports (see Figure 2). Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write arbitration doesn't occur is to perform redundant read cycles. Write/write arbitration needs can be avoided by assigning groups of addresses for write operation to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.





3

**ABSOLUTE MAXIMUM RATINGS\*** 

Voltage on Any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

O.5V to 7.0V

-40°C to +85°C

-55°C to 125°C

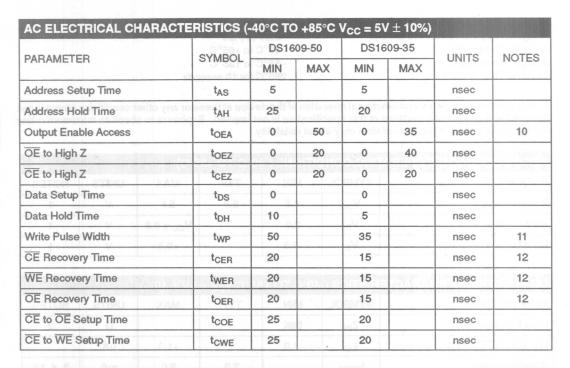
260°C for 10 seconds

<sup>\*</sup>This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

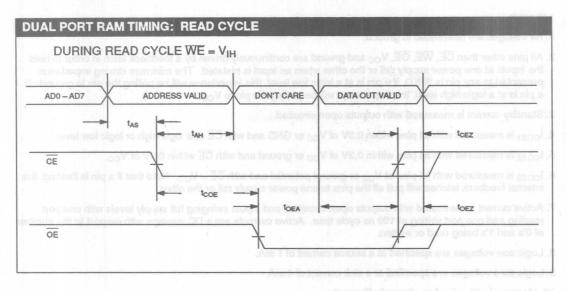
RECOMMENDED DC	OPERATING COND	ITIONS (-	40°C TO +	85°C)		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	Vcc	4.5	5.0	5.5	V	1
Input Logic 1	V <sub>IH</sub>	2.0	4837	V <sub>CC</sub> + 0.3	٧	1
Input Logic 0	V <sub>IL</sub>	-0.3	700	+0.8	V	1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance	Z <sub>IN</sub>	50K	360		Ω	2
CE, WE, OE Leakage	I <sub>LO</sub>	-1.0	3wo7	+1.0	μА	S HALFOR H
Standby Current	Iccs1		3.0	5.0	mA	3, 4, 13
Standby Current	I <sub>CCS2</sub>	e a la l	50	300	μА	3, 5, 13
Standby Current	I <sub>CCS3</sub>	o evolució	100		nA 🖺	3, 6, 13
Operating Current	Icc		18	30	mA	7, 13
Logic 1 Output	V <sub>OH</sub>	2.4		-	V	8
Logic 0 Output	V <sub>OL</sub>		PLA <sup>2</sup>	0.4	V	9

CAPACI	CAPACITANCE (t <sub>A</sub> = 25°C)							
PARAMET	TER	98	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capa	acitance		CIN	0	5	10	pF	QUAST IUSC
I/O Capac	itance		C <sub>VO</sub>	91	5	10	pF	DIDPF ELSC
27	- baen		0  -	991	- AMI		(SEDIM)	adu 4 em vi
			20					

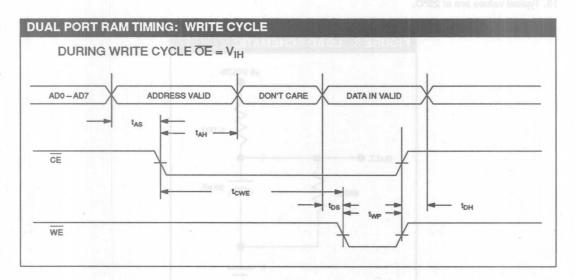


PARAMETER	SYMBOL	DS16	609-50	DS16	09-35	UNITS	NOTES
PARAMETER	STMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Address Setup Time	t <sub>AS</sub>	5		5		nsec	
Address Hold Time	t <sub>AH</sub>	25		25		nsec	
Output Enable Access	t <sub>OEA</sub>	0	100	0	75	nsec	10
OE to High Z	toez	0	20	0	20	nsec	10170
CE to High Z	t <sub>CEZ</sub>	0	20	0	20	nsec	
Data Setup Time	t <sub>DS</sub>	0		0		nsec	11-11-11-1
Data Hold Time	t <sub>DH</sub>	10		10		nsec	
Write Pulse Width	t <sub>WP</sub>	100		75		nsec	11
CE Recovery Time	t <sub>CER</sub>	20		20		nsec	12
WE Recovery Time	twer	20		20		nsec	12
OE Recovery Time	toer	20		20		nsec	12
CE to OE Setup Time	t <sub>COE</sub>	25		25	-	nsec	
CE to WE Setup Time	tcwe	25		25		nsec	



# NOTES

- 1. During read cycle the address must be off the bus prior to t<sub>OEA</sub> minimum to avoid bus contention.
- 2. Read cycles are terminated by the first occurring rising edge of OE or CE.

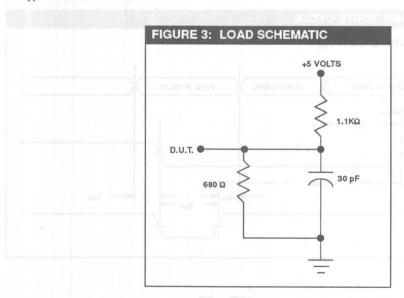


# NOTE

1. Write cycles are terminated by the first occurring edge of WE or CE.

#### NOTES

- 1. All Voltages are referenced to ground.
- 2. All pins other than CE, WE, OE, V<sub>CC</sub> and ground are continuously driven by a feedback latch in order to hold the inputs at one power supply rail or the other when an input is tristated. The minimum driving impedance presented to any pin is 50KΩ If a pin is at a logic low level, this impedance will be pulling the pin to ground. If a pin is at a logic high level, this impedance will be pulling the pin to V<sub>CC</sub>.
- 3. Standby current is measured with outputs open circuited.
- 4. I<sub>CCS1</sub> is measured with all pins within 0.3V of V<sub>CC</sub> or GND and with  $\overline{\text{CE}}$  at a logic high or logic low level.
- I<sub>CCS2</sub> is measured with all pins within 0.3V of V<sub>CC</sub> or ground and with CE within 0.3V of V<sub>CC</sub>.
- 6. I<sub>CCS3</sub> is measured with all pins at V<sub>CC</sub> or ground potential and with \(\overline{CE} = V\_{CC}\). Note that if a pin is floating, the internal feedback latches will pull all the pins to one power supply rail or the other.
- 7. Active current is measured with outputs open circuited, and inputs swinging full supply levels with one port reading and one port writing at 100 ns cycle time. Active currents are a DC average with respect to the number of 0's and 1's being read or written.
- 8. Logic one voltages are specified at a source current of 1 mA.
- 9. Logic zero voltages are specified at a sink current of 4 mA.
- 10. Measured with a load as shown in Figure 3.
- 11. t<sub>WP</sub> is defined as the time from WE going low to the first of the rising edges of WE and CE.
- 12. Recovery time is the amount of time control signals must remain high between successive cycles.
- 13. Typical values are at 25°C.



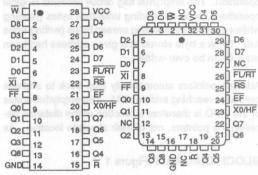


# **DS2009** 512 x 9 FIFO Chip

#### **FEATURES**

- · First-in, first-out memory-based architecture
- Flexible 512 x 9 organization
- Low-power HCMOS technology
- · Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- · Empty and full warning flags
- · Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 35ns, 50ns, 65ns, 80ns, and 120ns access times

# PIN ASSIGNMENT



28-Pin DIP(300 and 600 Mll) See Mech. Drawings Sect. 16, Pgs. 1 & 4 32-Pin PLCC See Mech. Drawing Sect. 16, Pg. 11

# PIN DESCRIPTION

₩ - WRITE

R - READ

RS - RESET

FL/RT - First Load/Retransmit

 $\begin{array}{lll} \mathsf{D}_{0\text{-8}} & & \mathsf{-} \ \mathsf{Data} \ \mathsf{In} \\ \mathsf{Q}_{0\text{-8}} & & \mathsf{-} \ \mathsf{Data} \ \mathsf{Out} \\ \hline \mathsf{XI} & & \mathsf{-} \ \mathsf{Expansion} \ \mathsf{In} \end{array}$ 

XO/HF - Expansion Out/Half Full

FF - Full Flag

EF - Empty Flag

V<sub>CC</sub> - 5 Volts

GND - Ground

NC - No Connect

#### DESCRIPTION

The DS2009 512 x 9 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2009 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-de-

vice and width-expansion configurations. The data is loaded and emptied on a first-in, first-out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

3

#### **OPERATION**

Unlike conventional shift register-based FIFOs, the DS2009 employs a memory-based architecture wherein a byte written into the device does not ripple through. Instead, a byte written into the DS2009 is stored at a specific location where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the address required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing unread bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

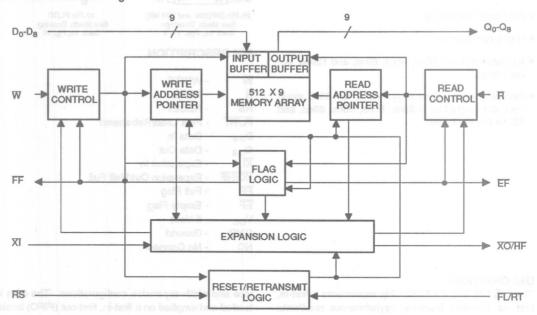
Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As

long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

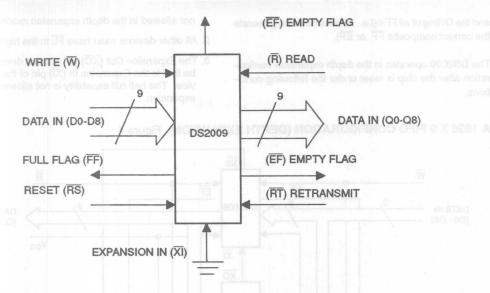
With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2009 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2009 can connect the read, write, data in, and data out lines of the DS2009 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion in and expansion out pins as appropriate (see the "Expansion Timing" section for a more complete discussion).

# **BLOCK DIAGRAM** Figure 1

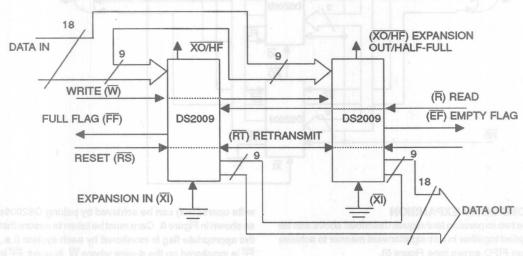


# SINGLE DEVICE CONFIGURATION

A single DS2009 can be used when application requirements are for 512 words or less. The DS2009 is placed in single device configuration mode when the chip is reset with the Expansion In pin  $(\overline{XI})$  grounded (see Figure 2).



# A 512 X 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



#### NOTE:

Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

# **DEPTH EXPANSION (DAISY CHAIN)**

The DS2009 can easily be adapted to applications where more than 512 words are required. Figure 4 dem-

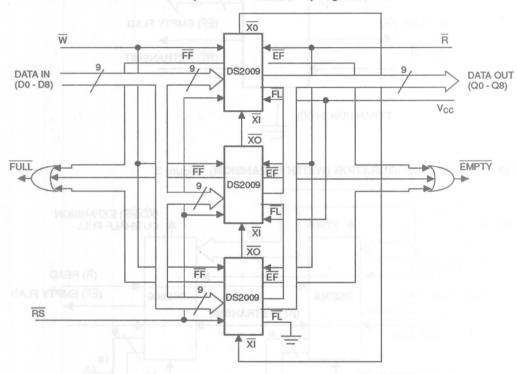
onstrates depth expansion using three DS2009s. Any depth can be attained by adding DS2009s.

External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all EFs and the ORing of all FFs (i.e., all must be set to generate the correct composite FF or EF).

The DS2009 operates in the depth expansion configuration after the chip is reset under the following conditions.

- The first device must be designated by grounding the First Load pin (FL). The retransmit function is not allowed in the depth expansion mode.
- 2. All other devices must have FL in the high state.
- The Expansion Out (XO) pin of each device must be tied to the Expansion In (XI) pin of the next device. The half-full capability is not allowed in depth expansion.

# A 1536 X 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



#### COMPOUND EXPANSION

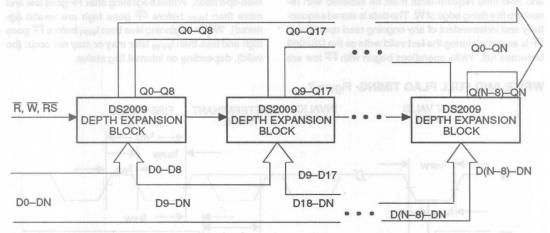
The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

# **BIDIRECTIONAL APPLICATIONS**

Bidirectional applications that require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing DS2009s as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e.,  $\overline{\text{FF}}$  is monitored on the device where  $\overline{\text{W}}$  is used;  $\overline{\text{EF}}$  is monitored on the device where  $\overline{\text{R}}$  is used). Both depth expansion and width expansion can be used in this mode.

# 3

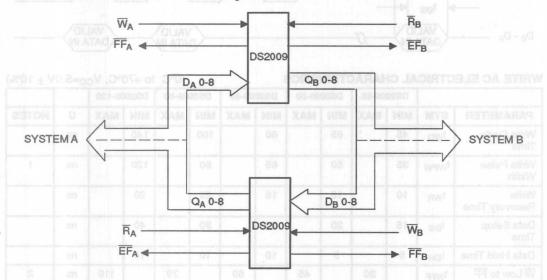
## **COMPOUND FIFO EXPANSION Figure 5**



## NOTES:

- 1. For depth expansion block diagram see "Depth Expansion" section and Figure 4.
- 2. For flag operation see "Width Expansion" section and Figure 3.

# **BIDIRECTIONAL FIFO APPLICATION Figure 6**



## HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the  $\overline{\text{XO/HF}}$  output acts as an indication of a half-full memory. ( $\overline{\text{XI}}$  must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ( $\overline{\text{HF}}$ ) will be set to low and will remain low until the difference between the write pointer and read

pointer is less than or equal to one half of the total memory of the device. The half-full flag is then reset (forced high) by the rising edge of the read operation.

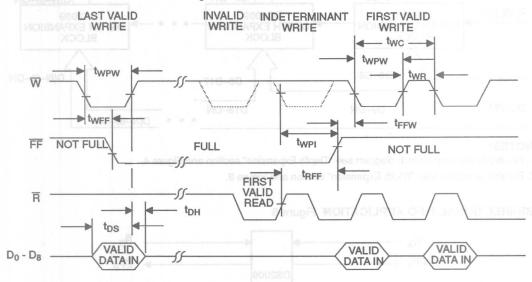
#### WRITE MODE

The DS2009 initiates a write cycle (see Figure 7) on the falling edge of the write enable control input  $(\overline{W})$ , pro-

vided that the Full Flag (FF) is not asserted. Data setup and hold time requirements must be satisfied with respect to the rising edge of  $\overline{W}$ . The data is stored sequentially and independent of any ongoing read operations. FF is asserted during the last valid write as the DS2009 becomes full. Write operations begun with  $\overline{\text{FF}}$  low are

inhibited.  $\overline{FF}$  will go high  $t_{RFF}$  after completion of a valid read operation. Writes beginning after  $\overline{FF}$  goes low and more than  $t_{WPI}$  before  $\overline{FF}$  goes high are invalid (ignored). Writes beginning less than  $t_{WPI}$  before  $\overline{FF}$  goes high and less than  $t_{FFW}$  later may or may not occur (be valid), depending on internal flag status.

# WRITE AND FULL FLAG TIMING Figure 7



#### WRITE AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V<sub>CC</sub>=5.0V ± 10%)

		DS20	009-35	DS20	009-50	DS20	009-65	DS20	009-80	DS20	09-120		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	NOTES
Write Cycle Time	twc	45		65		80		100		140		ns	TSYN
Write Pulse Width	t <sub>WPW</sub>	35		50		65		80		120		ns	1
Write Recovery Time	t <sub>WR</sub>	10		15		15		20		20		ns	
Data Setup Time	t <sub>DS</sub>	15	-	20	-	25		30		40		ns	
Data Hold Time	t <sub>DH</sub>	5		5		10		10		10		ns	
W Low to FF Low	t <sub>WFF</sub>	liese to	30	aat si	45		60		70	VOID	110	ns	2
FF High to Valid Write	t <sub>FFW</sub>	e pris	5	ets to y	5	9	10	tm nei tut-tia	n 10 o	diaw disabl	10	ns	2
R High to FF High	t <sub>RFF</sub>		30		45		60	terner	70	the n	110	ns	2
Write Protect Indeterminate	t <sub>WPI</sub>	effiw a	15	9003	20	30 5	25	netnio	25	setto un the	35	ns	2

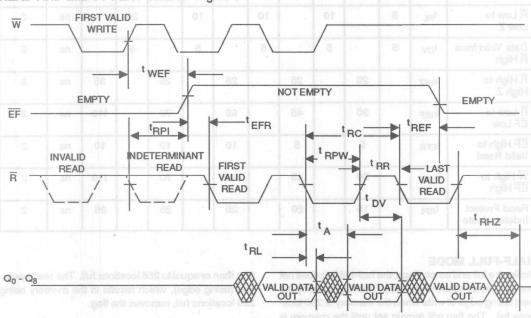
# 3

# READ MODE WY OF OWN of OFO

The DS2009 initiates a read cycle (see Figure 8) on the falling edge of Read Enable control input  $(\overline{R})$ , provided that the Empty Flag  $(\overline{EF})$  is not asserted. In the read mode of operation, the DS2009 provides fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing write operations. After  $\overline{R}$  goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the  $\overline{EF}$  will go low, and further read operations will be inhibited (the data outputs will remain in high impedance).  $\overline{EF}$  will go high  $t_{WEF}$  after completion of a valid write operation. Reads beginning  $t_{EFR}$  after  $\overline{EF}$  goes high are valid. Reads begun after  $\overline{EF}$  goes low and more than  $t_{RPI}$  before  $\overline{EF}$  goes high are invalid (ignored). Reads beginning less than  $t_{RPI}$  before  $\overline{EF}$  goes high and less than  $t_{EFR}$  later may or may not occur (be valid) depending on internal flag status.







# READ AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C,  $V_{CC}=5.0V \pm 10\%$ )

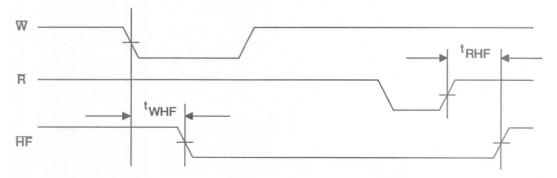
e of this enotioned	r road o	DS20	009-35	DS20	009-50	DS20	009-65	DS20	009-80	DS20	09-120		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	NOTES
Read Cycle Time	t <sub>RC</sub>	45	unbed s	65	nodsæ I blisv	80	ge arra	100	selveve Isle erl	140	Major III	ns	ati to stroi
Access Time	t <sub>A</sub>	led equ	35	ng lead	50		65	d asog	80	mo	120	ns	agil in
Read Recovery Time	t <sub>RR</sub>	10	may of flag st	15	gi narê no gri	15	ne noit	20	KOKTADAK	20	n e et oote	ns	ist etocila orrase er
Read Pulse Width	t <sub>RPW</sub>	35		50		65	8 610	80	MMATT	120	i Insi	ns	1 0 (3)
R Low to Low Z	t <sub>RL</sub>	5		10		10	-	10	7	20	ev fela Reigin	ns	2
Data Valid from R High	t <sub>DV</sub>	5		5		5		5	7	5		ns	2
R High to High Z	t <sub>RHZ</sub>		20	YT	25		25		25		35	ns	2
R Low to EF Low	t <sub>REF</sub>	paj-	30		45	893	60		70		110	ns	2
EF High to Valid Read	t <sub>EFR</sub>		5	yqa i	5		10	TMA	10	BC-1	10	ns	2
W High to EF High	tweF	7	30		45	1	60	1	70		110	ns	2
Read Protect Indeterminate	t <sub>RPI</sub>	150	15		20		25	3	25		35	ns	2

# HALF-FULL MODE

Unlike the full and empty flags, the half-full flag does not prevent device reads and writes. This flag is set by the next falling edge of write when the memory is 256 locations full. The flag will remain set until the memory is

less than or equal to 256 locations full. The read operation (rising edge), which results in the memory being 256 locations full, removes the flag.

# **HALF-FULL FLAG TIMING** Figure 9



# HALF-FULL FLAG AC CHARACTERISTICS

 $(0^{\circ}C \text{ to } +70^{\circ}C, V_{CC}=5.0V \pm 10\%)$ 

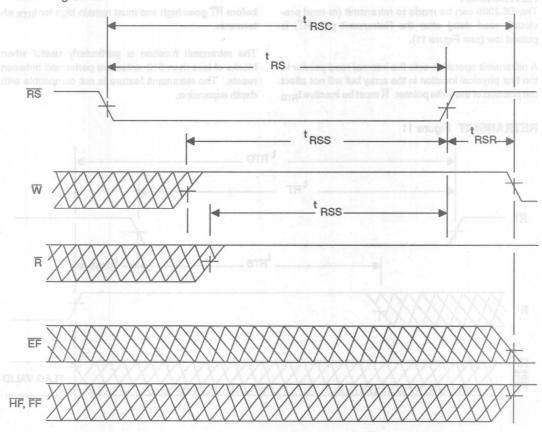
		DS20	09-35	DS20	009-50	DS20	09-65	DS20	009-80	DS20	09-120	na vivi
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Write Low to Half-Full Flag Low	t <sub>WHF</sub>	08-00 MAM	45	39-65 XAM	65	08-00 XAM	80	88-90 NAM	100	Mva	140	ns
Read High to Half-Full Flag High	t <sub>RHF</sub>		45		65		80		100	ase!	140	ns

## RESET

The DS2009 is reset (see Figure 10) whenever the Reset pin  $(\overline{\rm RS})$  is in the low state. During a reset, both the internal read and write pointer are set to the first location. Reset is required after a power-up before a write operation can begin .

Although neither  $\overline{W}$  or  $\overline{R}$  need be high when  $\overline{RS}$  goes low, both  $\overline{W}$  are  $\overline{R}$  must be high  $t_{RSS}$  before  $\overline{RS}$  goes high and must remain high  $t_{RSR}$  afterwards. Refer to the following discussion for the required state of  $\overline{FL/RT}$  and  $\overline{XI}$  during reset.

# **RESET** Figure 10



# NOTES 10.8 -- 20 V , 2007 - 01 200

EF, FF and HF may change status during reset, but flags will be valid at t<sub>RSC</sub>.

# RESET AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V<sub>CC</sub>=5.0V ± 10%)

		Door	200.05	Door	200.00	Door	200.05	, Door	00.00	D000	00 400		
140 ns		DS20	009-35	DS20	009-80	DS20	009-65	DS20	09-80	DS20	09-120	1-118	- 5
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	N
Reset Cycle Time	t <sub>RSC</sub>	45		65		80		100		140		ns	
Reset Pulse Width	t <sub>RS</sub>	35	Wierb	50	orbiA	65		80		120		ns	1
Reset Recovery Time	t <sub>RSR</sub>	10	are R r lement	15	low, high	15	draever seet, bo	20	t enug. ud - de	20	2 2 0 E	ns	1.3
Reset Setup Time	t <sub>RSS</sub>	30	noraeud Jer	40	yb.IX	50	ne met etore a	60	ana yeur	100	V DETECT	ns	2

#### RETRANSMIT

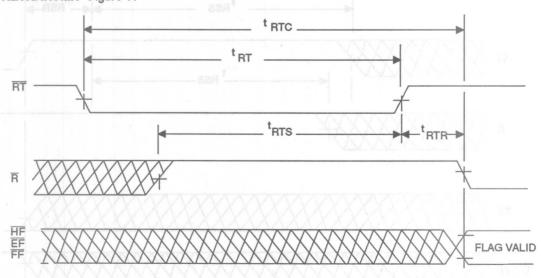
The DS2009 can be made to retransmit (re-read previously read data) after the Retransmit pin  $(\overline{RT})$  is pulsed low (see Figure 11).

A retransmit operation sets the internal read pointer to the first physical location in the array but will not affect the position of the write pointer.  $\overline{R}$  must be inactive terms

before  $\overline{\text{RT}}$  goes high and must remain high for  $t_{\text{RTR}}$  afterwards.

The retransmit function is particularly useful when blocks of less than 512 writes are performed between resets. The retransmit feature is not compatible with depth expansion.

# **RETRANSMIT** Figure 11



#### NOTE:

EF, FF and HF may change status during retransmit, but flags will be valid at t<sub>RTC</sub>.

RETRANSMIT
AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V<sub>CC</sub>=5.0V + 10%)

		DS20	009-35	DS20	09-80	DS20	009-65	DS20	009-80	DS20	09-120		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	N
Retransmit Cycle Time	t <sub>RTC</sub>	45		65		80	IASI	100	N BAIR C	140	R <sup>2</sup>	ns	
Retransmit Pulse Width	t <sub>RT</sub>	35 NBA	La	50		65		80	OJ	120		ns	1
Retransmit Recovery Time	t <sub>RTR</sub>	10	1	15		15		20		20		ns	
Retransmit Setup Time	t <sub>RTS</sub>	30	7	40		50		60		100		ns	

#### **EXPANSION TIMING**

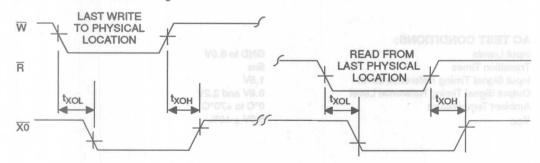
Figures 12 and 13 illustrate the timing of the expansion out and expansion in signals. Discussion of expansion out/expansion in timing is provided to clarify how depth expansion works. Inasmuch as expansion out pins are generally connected only to expansion in pins, the user need not be concerned with actual timing in a normal depth expanded application unless extreme propagation delays exist between the  $\overline{\rm XO}$  and  $\overline{\rm XI}$  pin pairs.

Expansion out pulses are the image of the write and read signals that cause them: delayed in time by  $t_{XOL}$  and  $t_{XOH}$ . The expansion out signal is propagated when the last physical location in the memory array is written and again when it is read (last read). This is in contrast

to when the full and empty flags are activated, which is in response to writing and reading a last available location.

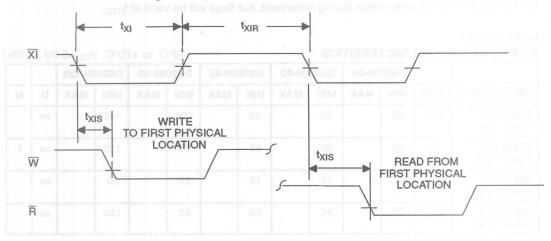
When in depth expansion mode, a given DS2009 will begin writing and reading as soon as valid write and read signals begin, provided  $\overline{FL}$  was grounded at reset time. A DS2009 in depth expansion mode with  $\overline{FL}$  high at reset will not begin writing until after an expansion in pulse occurs. It will not begin reading until a second expansion in pulse occurs and the empty flag has gone high. Expansion in pulses must occur  $t_{XIS}$  before the write and read signals they are intended to enable. Minimum expansion in pulse width,  $t_{XI}$ , and recovery time,  $t_{XIR}$ , must be observed.

#### **EXPANSION OUT TIMING** Figure 12



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# **EXPANSION IN TIMING** Figure 13



# EXPANSION LOGIC and strong beas that and medianot

AC ELECTRICAL CHARACTERISTICS

nolans are entire (0°C to +70°C,  $V_{CC} = 5.0V \pm 10\%$ )

		DS20	009-35	DS20	009-80	DS20	009-65	DS20	009-80	DS20	09-120	-1 134	872
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	N
Expansion Out Low	txoL	e ritge	30	signati A DS:	45	lisms.	55	nimit ta	70	y Lam	100	ns	ens on s
Expansion Out High	tхон	pacitor	30	huopo i	45	43 (200)	55	IX box	70	ing track	100	ns	> 150
Expansion in Pulse Width	t <sub>XI</sub>	35	ni noian angle bi	50	rigiri Mrw	65	iliw ed id emit	80	rmi odi Isla zama	120	luc, luci a lind ri	ns	1
Expansion in Recovery Time	t <sub>XIR</sub>	10	sión in s nazdo a	15	eusen vanc <sup>†</sup>	15	basaga ray is v	20	angan tu am am	20		ns	pri co
Expansion in Setup Time	t <sub>XIS</sub>	15		20		25	M2 ( B C)	30		40		ns	

# **AC TEST CONDITIONS:**

Input Levels
Transition Times
Input Signal Timing Reference Level
Output Signal Timing Reference Level
Ambient Temperature
Vcc

GND to 3.0V 5ns 1.5V 0.8V and 2.2V 0°C to +70°C 5.0V ± 10%

# 3

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature
Total Device Power Dissipation
Output Current per Pin

0°C to 70°C -55°C to +125°C 1 Watt 20 mA

\*This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

-0.5V to +7.0V

# RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	3
Ground	GND		0	5.7	VOAC	Tuerra
Logic 1 Voltage All Inputs	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	3
Logic 0 Inputs	VIL	-0.3		+0.8	V	3, 4

## DC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V<sub>CC</sub>=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I <sub>IL</sub>	-1		REG/IU TRET	μА	5
Output Leakage Current	loL	-10		10	μА	6
Output Logic 1 Voltage I <sub>OUT</sub> = -1mA	V <sub>OH</sub>	2.4	80 088		V	3
Output Logic 0 Voltage I <sub>OUT</sub> = 4mA	V <sub>OL</sub>	H		0.4	V	3
Average V <sub>CC</sub> Power Supply Current – 35ns, 50ns, 60ns, 80ns, 120ns	l <sub>CC1</sub>			100	mA	7, 9
Average Standby Current (R = W = RST = FL/RT = V <sub>IH</sub> )	I <sub>CC2</sub>			8	mA	7
Power Down Current (All Input = V <sub>CC</sub> -0.2V)	I <sub>CC3</sub>			500	μА	7, 10

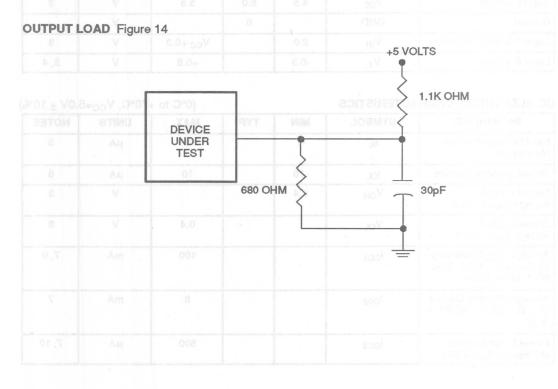
CAPACITANCE

(t<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	CI	7	pF	
Capacitance on Output Pins	Co	12	pF	8

# NOTES:

- 1. Pulse widths less than minimum values are not allowed.
- 2. Measured using output load shown in Output Load diagram.
- 3. All voltages are referenced to ground.
- 4. -1.5 volt undershoots are allowed for 10ns once per cycle.
- 5. Measured with  $0.4 \le V_{IN} \le V_{CC}$ .
- 6.  $\overline{R} \ge V_{IH}$ ,  $0.4 \ge V_{OUT} \le V_{CC}$ .
- 7. I<sub>CC</sub> measurements are made with outputs open.
- 8. With output buffer deselected.
- 9. DS2010, DS2011, DS2012, and DS2013 have I<sub>CC1</sub>, = 120 mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
- 10. DS2010 has  $I_{CC3} = 1$ mA MAX; DS2011, DS2012, DS2013 have  $I_{CC3} = 2$ mA MAX.

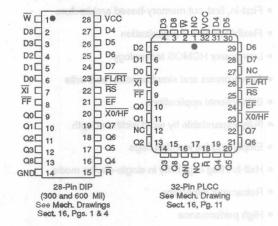


# DS2010 1024 x 9 FIFO Chip

#### **FEATURES**

- · First-in, first-out memory-based architecture
- Flexible 1024 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access times

#### PIN ASSIGNMENT



#### PIN DESCRIPTION

$\overline{W}$	- WRITE
R	- READ
RS	- RESET

FL/RT - First Load/Retransmit

- Data In D<sub>0-8</sub> Q<sub>0-8</sub> - Data Out - Expansion In XO/HF

- Expansion Out/Half Full

- Full Flag EF - Empty Flag Vcc - 5 Volts GND - Ground NC - No Connect

#### DESCRIPTION OF THE PROPERTY OF

The DS2010 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the

DS2009 512 x 9 FIFO, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

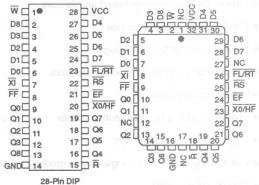


# **DS2011** 2048 x 9 FIFO Chip

#### **FEATURES**

- · First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access.

# **PIN ASSIGNMENT**



28-Pin DIP (300 and 600 Mil) See Mech. Drawings Sect. 16, Pgs. 1 & 4

32-Pin PLCC See Mech. Drawing Sect. 16, Pg. 11

# PIN DESCRIPTION

W - WRITE

R - READ

RS - RESET

FL/RT - First Load/Retransmit

D<sub>0-8</sub> - Data In Q<sub>0-8</sub> - Data Out

XI - Expansion In

XO/HF - Expansion Out/Half Full

FF - Full Flag

EF - Empty Flag

V<sub>CC</sub> - 5 Volts

GND - Ground

NC - No Connect

# DESCRIPTION

The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the

DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

# 3

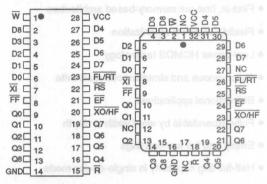
# DALLAS

# **DS2012** 4096 x 9 FIFO Chip

#### **FEATURES**

- · First-in, first-out memory-based architecture
- Flexible 4096 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- · Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

#### PIN ASSIGNMENT



28-Pin DIP (600 Mil) See Mech. Drawing Sect. 16, Pg. 4 32-Pin PLCC See Mech. Drawing Sect. 16, Pg. 11

# **PIN DESCRIPTION**

W - WRITE

R - READ

RS - RESET

FL/RT - First Load/Retransmit

D<sub>0-8</sub> - Data In Q<sub>0-8</sub> - Data Out

XI - Expansion In

XO/HF - Expansion Out/Half Full

- No Connect

FF - Full Flag
EF - Empty Flag
V<sub>CC</sub> - 5 Volts
GND - Ground

NC

#### DESCRIPTION

The DS2012 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half full flags, and unlimited expansion capability in both word size and depth. The DS2012 is functionally and electrically equivalent to the DS2009

512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.



# **DS2013** 8192 x 9 FIFO Chip

## **FEATURES**

- · First-in, first-out memory-based architecture
- Flexible 8192 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

# PIN ASSIGNMENT

W	10	28	b vcc
D8□	2	27	D4
D3 🗆	3	26	□ D5
D2	4 000	25	□ D6
D1 🗆	5	24	□ D7
D0□	6	23	□ FL/RT
XI 🗆	7	22	RS
FF	8	21	□ EF
Q0 C	9	20	XO/HF
Q1 [	10	19	Q7
Q2 🗆	11	18	□ Q6
Q3 🗆	12	17	Q5
Q8 🗆	13	16	□ Q4
GND	14	15	□ R

28-Pin DIP (300 and 600 Mil) See Mech. Drawings - Sect. 16, Pgs. 1 & 4

# **PIN DESCRIPTION**

W - WRITE
R - READ
RS - RESET

FL/RT - First Load/Retransmit

D0<sub>-8</sub> - Data In Q0<sub>-8</sub> - Data Out XI - Expansion In

XO/HF - Expansion Out/Half Full

 FF
 - Full Flag

 EF
 - Empty Flag

 V<sub>CC</sub>
 - 5 Volts

 GND
 - Ground

 NC
 - No Connect

#### DESCRIPTION

The DS2013 8192 x 9 FIFO Chip implements a first-in, first-out algorithm, featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2013 is functionally and electrically equivalent to the

DS2009 512 x 9 FIFO with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to DS2009 512 x 9 FIFO Chip data sheet for detailed device description.

# 3

# DALLAS

# Quad Port Serial RAM Chip

#### **FEATURES**

- · Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin-count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes | MAR MAR most
- Low-power CMOS
- Space saving 18-pin DIP
- Directly interfaces to the DS1206 Phantom Serial Interface Chip
- Provides a low cost interconnect for up to four microprocessor based systems

### DESCRIPTION

The DS2015 Quad Port Serial RAM Chip is a low-cost device which can loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for

#### PIN ASSIGNMENT



18-Pin DIP (300 Mil) See Mech. Drawing Sect. 16, Pg. 1

#### PIN DESCRIPTION

RST0-RST3	Port 0 - Port 3 Reset		
D/Q0-D/Q3	Port 0 - Port 3 Data I/O		
CLK0-CLK3	Port 0 - Port 3 Clock		
MO-M3	Port 0 - Port 3 Message Ready		
GND	Ground		
Vcc	+5 Volts		

each port is 64 bits. Access to and from each port takes place over a 3-wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

#### **OPERATION**

The DS2015 has four separate three-wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes, each of which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quadported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three-wire serial ports contains a threebyte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

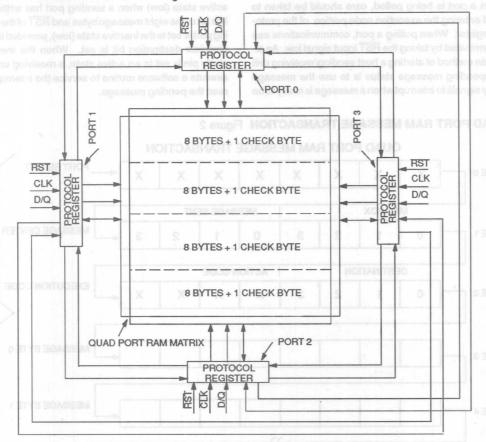
**Protocol Register** 

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight-bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles: messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the RST input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while RST is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles: the action code and the destination. This byte is write only and data is input on the D/Q line with RST inactive and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight-byte message is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

# **Quad Port RAM**

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

#### QUAD PORT BLOCK DIAGRAM Figure 1



#### **Check Byte**

A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the

sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

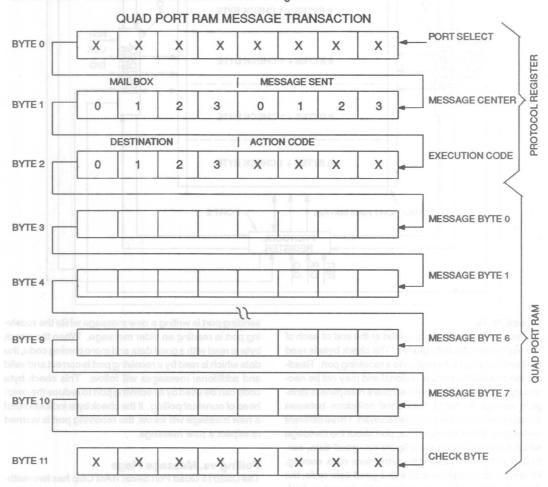
#### Polling vs. Message Flags

The DS2015 Quad Port Serial RAM Chip has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of

the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the RST input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be

read. The message ready pins (M0-M3) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and RST of the sending port is set to the inactive state (low), provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

#### **QUAD PORT RAM MESSAGE TRANSACTION** Figure 2



NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE. BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

## PORT SELECT CODE Figure 3

A DESIGNATION OF THE PERSON NAMED IN	ATT DITIE SHO	Protocolt	plock	ent.bns;	id ines eg	LSB	being rend, th
All mes	0	0	pnillet est <mark>i</mark> n	0	wol nevhi Isro <b>1</b> go a	al Tan	PORT 0
H TEST	m namvi : anelijens	ance sone	Rugo hecluii				or ignored.
1 50	0	dgir¶ls a Report 4.0	atah	0	1	1	PORT 1
				ed teem	rateo eur	Emdu e	For messing
1	1	0	1	A session (T	1 8999	MAST 3	PORT 2
1	1	1	1	0	1	1	PORT 3
	eem IIA anili OV II seess 1	1 0	1 0 1 1 1 0	1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 0	1 1 0 1 0 1	1 1 0 1 0 1 1 A MUDEL RESIDENCE

MSE		CODES	LSB	_
0	10 100 B	0	0	READ
01110	0	0	W AO G	WRITE
1	1	0	0	WRITE DATE, MORE COMING

MSB		CI	HECK BY	TE COD	ES		LSB	seráting Temperatura orage Temporature
0	1 po terito y	0	noe at the	0	1 noils rega	0	ul bas vin	GOOD DATA
1	0	1	0	1	0	1	0	CORRUPTED DATA
0	тем	Ö	1	1 1	0	- 1dan	0	GOOD DATA, MORE COMING

#### **RST** Control

All message transactions are initiated by driving the RST port input high. The RST input serves two functions. First, it turns on control logic which allows access to the protocol register. Second, the RST signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

- I. While polling the message center for new messages, always terminate the transaction by driving RST low after completing a read of the message center byte and before entering the execution code byte.
- 2. When sending a message, all eight message bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

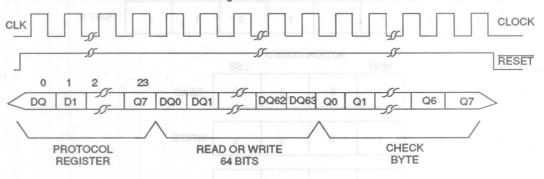
sage which is being read, the message sent bit and the mailbox bit are cleared as RST is driven low. When reading a message, the check byte is optional and can be either read or ignored.

clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if  $\overline{RST}$  is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using  $\overline{RST}$ , the transition of  $\overline{RST}$  must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

#### CLOCK CONTROL

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be

QUAD PORT MESSAGE TRANSFER Figure 4



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature -1.0V to 7.0V 0°C to 70°C -55°C to 125°C

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		V <sub>CC</sub> +0,3	٧	1
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1 -
Supply and private and molifor	V <sub>CC</sub>	4.5	5.0	5.5	V	100 100

## DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V<sub>CC</sub> = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>IL</sub>	-1		1	μА	RES
Output Leakage	ILO	and beauti		1	μА	
Output Current @ 2.4V	Іон	-1		101 19-1	mA	
Output Current @ .4V	l <sub>OL</sub>	+4	1 h	_f \	mA N	Q40
Supply Current	Icc	_	mi HOT has	6	mA	2

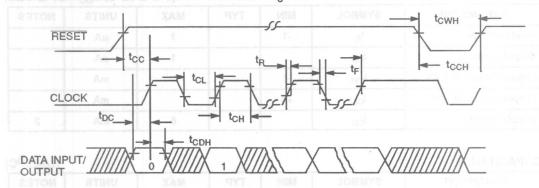
						17
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	and extends on
Output Capacitance	C <sub>OUT</sub>	o empli	Little solizion.	7	pF	and and signed

#### AC ELECTRICAL CHARACTERISTICS

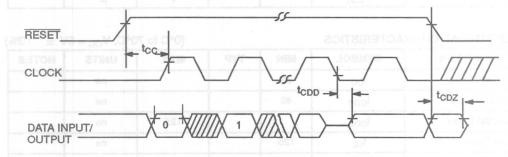
 $(0^{\circ}\text{C to } 70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	1	/ - `	ns	- Dinora
CLK to Data Hold	t <sub>CDH</sub>	40			ns	
CLK to Data Delay	tcod	TYM	( - N	125	ns	BELATAGE
CLK Low Time	t <sub>CL</sub>	125	Investment William	Albert Samuel Se	ns	TUTTUO
CLK High Time	t <sub>CH</sub>	125			ns	
CLK Frequency	t <sub>CLK</sub>	DC	nupFI YC	4.0	MHz	MO EMBM
CLK Rise and Fall	t <sub>R</sub> , t <sub>F</sub>			500	ns	
RST to CLK Setup	tcc	1			μs	
CLK to RST Hold	t <sub>CCH</sub>	40			ns	
RST Inactive Time	tcwH	125			ns	-
RST to I/O High Z	t <sub>CDZ</sub>			50	ns	
RST to Message Ready	t <sub>RF</sub>			100	ns	

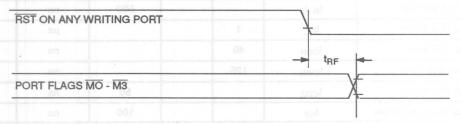
## TIMING DIAGRAM-WRITE DATA TRANSFER Figure 5



## TIMING DIAGRAM-READ DATA TRANSFER Figure 6



## TIMING DIAGRAM-MESSAGE READY Figure 7



#### NOTES:

- 1. All voltages are referenced to ground.
- 2. All outputs are open.

# DALLAS

**Dual Port RAM** Application Note - 62

TOT ENABLE		36	

OF is inactive, and CE becoming active lateres the address to be accessed, with Will becoming active,

The DS1 509 dual port RAM has a special cell design hat allows for simultaneous accesses from two ports

Memory devices and systems are diversifying and becoming more complex out of necessity to support information processing needs. The need to centralize data storage in multiprocessor applications challenges both hardware and software designers. New ways must be found that consolidate system information that is controllable by more than one bus. In addition, systems are becoming more power conscious, particularly portable systems as they typically rely on some kind of rechargeable battery for power. For systems where shared bus access requirements are infrequent, but require many megabytes of memory to be transferred, a shared mass storage device such as a floppy disk drive or networked hard disk drive may suffice. However, for frequent, low density access, media such as hard drives or floppy diskettes are impractical and would greatly slow the rate at which data could be stored and retrieved. The DS1609 Dual Port Ram has been specifically designed to be able to meet high frequency, low volume data storage and retrieval between two asynchronous systems. With its ability to operate at voltages as low as 2.5 volts, the DS1609 also fits easily into any portable application where power availability is limited.

PORTA	36			PORT B
AD7A	1	0	24	□ V <sub>CC</sub>
AD6 <sub>A</sub>	2		23	OEB
AD5A	3		22	CEB
AD4 <sub>A</sub>	4		21	□ WE <sub>B</sub>
AD3A	5		20	AD0 <sub>B</sub>
AD2A	6		19	AD1 <sub>B</sub>
AD1A	7		18	AD2 <sub>B</sub>
ADO <sub>A</sub>	8		17	AD3 <sub>B</sub>
WE <sub>A</sub>	9		16	AD4 <sub>B</sub>
CE <sub>A</sub>	10		15	AD5 <sub>B</sub>
OE <sub>A</sub>	11		14	AD6 <sub>B</sub>
GND [	12		13	AD7 <sub>B</sub>
	24 P	DS1609 IN DIP (6		
PORT	A			PORT B
AD7 <sub>A</sub> AD6 <sub>A</sub> AD5 <sub>A</sub> AD4 <sub>A</sub> AD3 <sub>A</sub> AD2 <sub>A</sub> AD1 <sub>A</sub> AD0 <sub>A</sub> WEA CEA GND	REBEBBBBB	1 1 2 3 4 4 5 6 6 7 8 9 10 11 12	24	OEB CEB WEB AD0B AD1B AD2B AD3B AD4B AD5B AD5B AD6B

PIN NAME	DESCRIPTION
Vcc	+5 VOLT SUPPLY
GND	GROUND
AD0-AD7	PORT ADDRESS/DATA
CE	PORT ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE

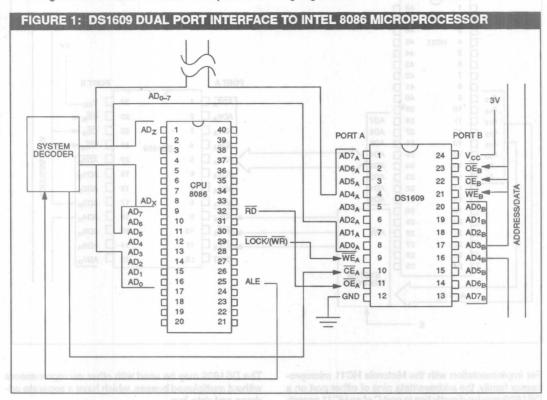
The type of bus which may be connected to either port of the DS1609 is not limited to system level. A multiplexed microprocessor address and data bus can be connected directly to either or both ports of the DS1609. The device can be controlled from either bus port separately by only three signals,  $\overline{OE}$ ,  $\overline{CE}$ , and  $\overline{WE}$ . The obvious disadvantage of the multiplexed bus is the slightly reduced system performance because address and data information is being transmitted serially. The equally obvious advantage is the reduced pin count achievable by multiplexing the addressing and data buses.

Read/Write access of either port is transferred as 8 bits address, followed by 8 bits of data. In a read cycle to a port,  $\overline{WE}$  is inactive, and the cycle is initiated when  $\overline{CE}$  goes active, which with the address latched, data is retrieved under the control of  $\overline{OE}$ . The rising edge of either  $\overline{CE}$  or  $\overline{OE}$  terminates the read cycle. For a write cycle,  $\overline{OE}$  is inactive, and  $\overline{CE}$  becoming active latches the address to be accessed, with  $\overline{WE}$  becoming active.

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports. Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write contention does not occur is to perform redundant read cycles. Write/write contention needs can be avoided by assigning groups of addresses for write operations to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using

3

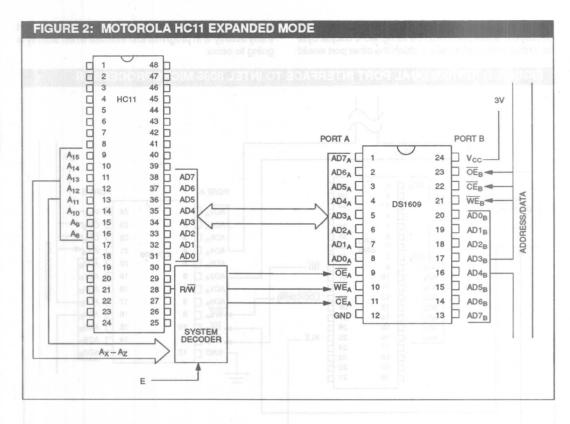
a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.



The DS1609 is ideally suited for small microprocessor based systems which frequently utilize dedicated 8 bit multiplexed address/data busses the following examples deal with interfacing with the Intel 8086/8088 series and the Motorola HC11 series microprocessors.

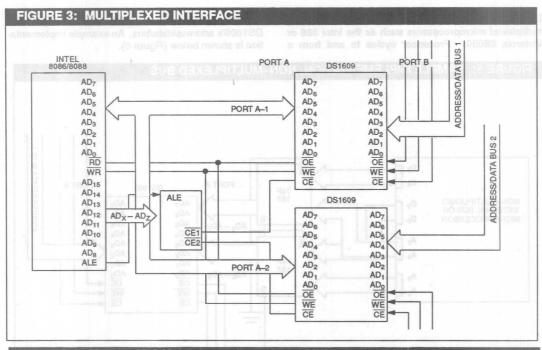
For implementation with the Intel 8086/8088 microprocessor family, the address/data pins of either port may be tied directly to the lower 8 address data lines of the Intel 8086 or 8088 microprocessor (Figure 1). The RD pin from the microprocessor provides the OE input to the port on the DS1609, while WR provides the WE in-

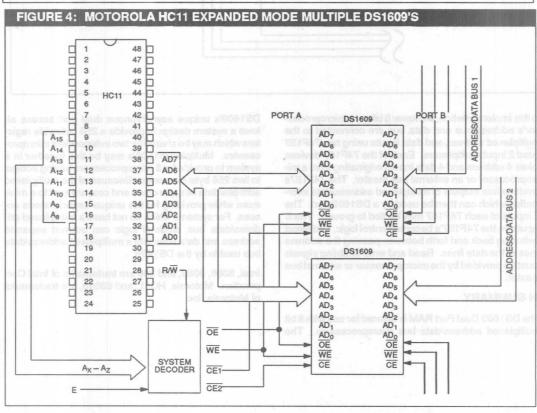
put to the port. The port's  $\overline{CE}$  input may be conditioned by a system decoder, which would require the 8086's ALE output as an input to provide address latching. Several of the unused address/data lines from the 8086 would also be required as inputs to indicate where the DS1609 resides in the system memory map. In applications where multiple DS1609 ports are required, multiple  $\overline{CE}$  outputs could be provided from a system decoder using the ALE signal from an Intel 8086/8088 with user specified address lines to generate multiple chip selects (Figure 3).



For implementation with the Motorola HC11 microprocessor family, the address/data pins of either port on a DS1609 may be directly ties to port C of an HC11 operating in expanded mode (Figure 2). Address pins from port B of the HC11 (A<sub>8</sub> - A<sub>15</sub>) may be used to provide the DS1609's location in the system memory map. The E signal, which is also an input to the HC11, provides a bus clock to the system decoder indicating whether the HC11 is in an address or data cycle. The R/W input to the decoder indicates whether the HC11 is writing or reading data in a data cycle. From these inputs, a system decoder can provide OE, WE, and CE outputs to DS1609. For applications where more density is required, two DS1609's may be used. The same inputs, including a user selected combination of address lines A<sub>8</sub> - A<sub>15</sub> can be used to provide OE, WE, and multiple CE signals for individual DS1609 devices (Figure 4).

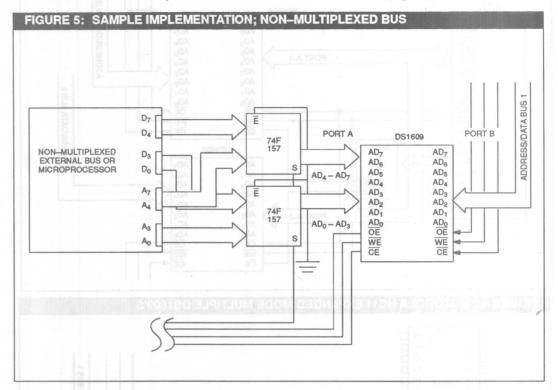
The DS1609 may be used with other microprocessors without multiplexed busses, which have a separate address and data bus.





The DS1609 can be used as a go between with non-multiplexed microprocessors such as the Intel 386 or Motorola 68030. Processor cycles to and from a

DS1609 must then be multiplexed specifically for the DS1609's address/data/bus. An example implementation is shown below (Figure 5).



In this implementation, the lower 8 bits of a microprocessor's address bus and data bus are connected to the multiplexed address and data inputs using two 74F157 quad 2 input multiplexers. Each of the 74F157 devices takes 4 address and 4 data inputs originating from a microprocessor or an external bus master. The 74F157s produce four outputs of multiplexed address/data information which can then be used by a DS1609 port. The E inputs of each 74F157 may be tied to ground. The S inputs on the 74F157's become control logic, and direct switching back and forth between passing the address lines or the data lines. Read and write enabling signals must be provided by the microprocessor or external bus master.

#### IN SUMMARY

The DS1609 Dual Port RAM is tailored for use with 8 bit multiplexed address/data bus microprocessors. The

DS1609's unique asynchronous dual port access allows a system design to provide a 256 bytewide registers which may be shared by two independent microprocessors. Multiple DS1609's may be tied together in a system to provide for 3 microprocessors having access to two 256 byte memories. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while providing for the unique asynchronous access. For systems which do not have a multiplexed address/data bus, minimal logic can convert separate address and data lines into a multiplexed address/data bus usable by the DS1609.

Intel, 8086, 8088, and 386 are trademarks of Intel Corporation. Motorola, HC11, and 68030, are trademarks of Motorola, Inc.

**General Information** 

**Silicon Timed Circuits** 

**Multiport Memory** 

Nonvolatile RAM

Intelligent Sockets

Timekeeping

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

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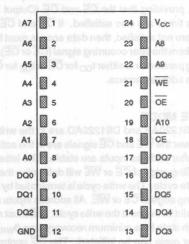


## DS1220AB/AD 16K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- · Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



24-PIN ENCAPSULATED PACKAGE (720 Mil Extended)

#### PIN DESCRIPTION

A<sub>0</sub>-A<sub>10</sub> - Address Inputs
CE - Chip Enable
GND - Ground

 DQ0-DQ7
 - Data In/Data Out

 VCC
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

#### DESCRIPTION

The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be

used in place of existing 2Kx8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220AB/AD also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

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#### READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever WE (Write Enable) is inactive (high) and CE (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A<sub>0</sub>-A<sub>10</sub>) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t<sub>ACC</sub> (Access Time) after the last address input signal is stable, providing that the CE and OE (Output Enable) access times are also satisfied. If OE and CE access times are not satisfied, then data access must be measured from the later occurring signal (CE or OE) and the limiting parameter is either t<sub>CO</sub> for CE or t<sub>OE</sub> for OE rather than address access.

#### WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in toppy from its falling edge.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature The DS1220AB provides full functional capability for V<sub>CC</sub> greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V<sub>CC</sub> greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V<sub>CC</sub> without any additional support circuitry. The nonvolatile static RAM constantly monitors V<sub>CC</sub>. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V<sub>CC</sub> falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V<sub>CC</sub> rises above approximately 3.0 volts, the power switching circuit connects external V<sub>CC</sub> to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V<sub>CC</sub> exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

#### SHIPPING AND START-UP

The DS1220AB/AD is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

-0.3V to +7.0V 0°C to +70°C; -40°C to +85°C for IND parts -40°C to +70°C; -40°C to +85°C for IND parts 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN as	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	Min Not go
DS1220AD Power Supply Voltage	V <sub>CC</sub>	4.50	5.0	5.50	V mark	alt silve yth
Logic 1	VIH	2.2	NO SHAIR CAN	V <sub>CC</sub>	٧.	AS OF BUILDING
Logic 0	V <sub>IL</sub>	0.0		+0.8	V	

1

(0°C to 70°C;  $V_{CC}=5V \pm 10\%$  for DS1220AD)

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C;  $V_{CC}=5V \pm 5\%$  for DS1220AB)

 $V_{TP}$ 

DE ELECTRICAL CHARACTE	MISTICS		(0 C to 70 C, VCC=5V ± 576 for D31220AB				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μА	from Decel	
I/O Leakage Current CE≥V <sub>IH</sub> ≤V <sub>CC</sub>	I <sub>IO</sub>	-1.0	à	+1.0	μА	non Output Hold	
Output Current @2.4V	Пон	-1.0			mA	roup Adduna. Charge	
Output Current @0.4V	loL	2.0	120	100	mA	White Cycle	
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	genit	
Standby Current $\overline{CE} = V_{CC}$ -0.5V	I <sub>CCS2</sub>		3.0	5.0	mA	Pulled Pulled Wickley	
Operating Current t <sub>CYC</sub> =200ns (Commercial)	I <sub>CC01</sub>		0	75	mA ou	Address Set Time	
Operating Current t <sub>CYC</sub> =200ns (Industrial)	I <sub>CC01</sub>		101	85	mA	Vocafi ethiV emiT	
Write Protection Voltage (DS1220AB)	≥ V <sub>TP</sub>	4.5	4.62	4.75	Maoi V E	Output High from WE	

## DC TEST CONDITIONS

Write Protection Voltage (DS1220AD)

Outputs open.

All voltages are referenced to ground.

#### CAPACITANCE

(t<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	in!
Input/Output Capacitance	C <sub>VO</sub>		5	12	pF	ocken for

4.25

4.37

4.5

## AC ELECTRICAL CHARACTERISTICS

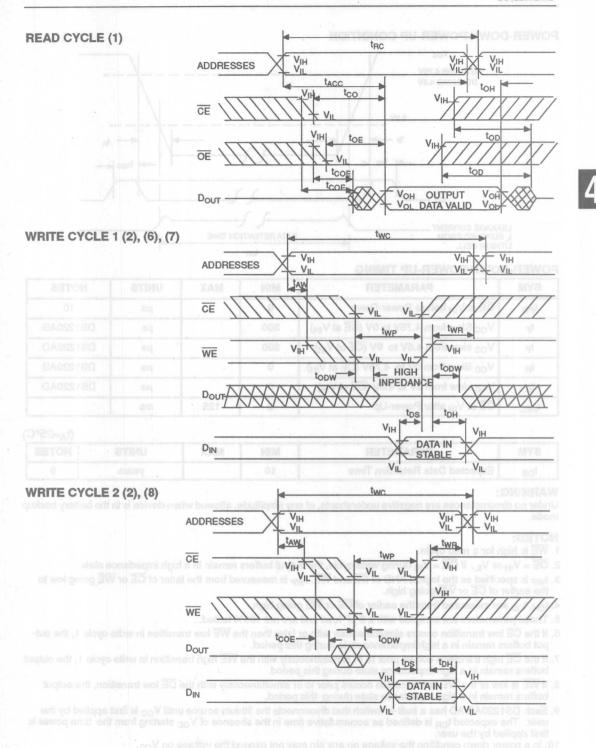
(0°C to 70°C;  $V_{CC}$ =5.0V  $\pm$  10% for DS1220AD) (0°C to 70°C;  $V_{CC}$ =5.0V  $\pm$  5% for DS1220AB)

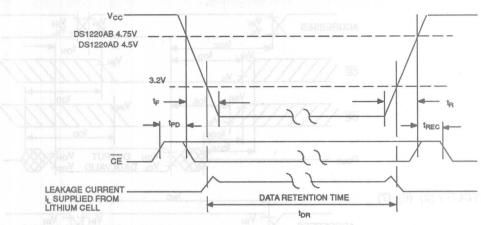
		DS1220A	B/AD-100	DS1220A	B/AD-120	DS1220A	AB/AD-150	DS1220/	B/AD-200		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Read Cycle Time	t <sub>RC</sub>	100		120		150		200		ns	
Access Time	tACC		100		120		150		200	ns	
OE to Output Valid	<sup>t</sup> OE		50		60		70		100	ns	
CE to Output Valid	tco		100		120		150		200	ns	
OE or CE to Output Active	tCOE	5		5		5		5		ns	5

UAUSSIEU 101 a	KOL Ŧ	DS1220A	B/AD-100	DS1220A	B/AD-120	DS1220/	AB/AD-150	DS1220A	B/AD-200	all a life and	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Output High Z from Deselec- tion	t <sub>OD</sub>	+1.0	35		35		35		35	ns	5
Output Hold from Address Change	t <sub>OH</sub>	5		5	-1.0	5	101	5	1000	ns	utoglu (
Write Cycle Time	twc	100		120	2.0	150	iol lool	200		ns	l Juglus
Write Pulse Width	t <sub>WP</sub>	75		90		100	lool	150	0 1	ns	3
Address Setup Time	t <sub>AW</sub>	0		0		0	1301	0	h= //2	ns	Speration Comme
Write Recovery Time	t <sub>WR</sub>	10		10		10	30 <sup>1</sup>	10		ns	idensed Victoria
Output High Z from WE	topw	4,75	35	4.61	35		35		35	ns	5
Output Active from WE	toew	5		5	4.25	5	qV	5	HOSPIN	ns	5
Data Setup Time	t <sub>DS</sub>	40		- 50		60		80		ns	4
Data Hold Time	t <sub>DH</sub>	10		10		10		10	1	ns	4

#### **AC TEST CONDITIONS**

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns





#### POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	/0//	// BD	μs	10
t <sub>F</sub>	V <sub>CC</sub> Slew from 4.75V to 0V (CE at V <sub>IH</sub> )	300		μs	DS1220AB
tF	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300	30	μs	DS1220AD
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.75V (CE at V <sub>IH</sub> )	0	and the second	μs	DS1220AB
tR	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0	Zhaid	μs	DS1220AD
tREC	CE at VIH after Power-Up	2	125	ms	

(tA=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10		years	9

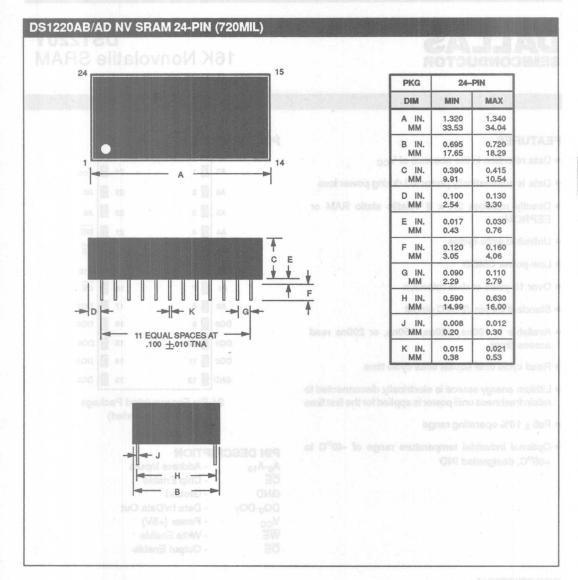
#### **WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

#### NOTES:

- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{II}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the CE low transition occurs simultaneously with or later than the WE low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the CE high transition occurs prior to or simultaneously with the WE high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1220AB/AD has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the
  user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is
  first applied by the user.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.





used in place of existing 2K x 6 BRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DB1 220Y also matches the pinout of the 27 16 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor insertace.

The DS1220Y 16K Nonvolatile SMAM is a 16,884-bit, bully statio, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained filhium energy source and control circuitry that constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent carbied data. The NV SRAM can be enabled to prevent carbied data. The NV SRAM can be

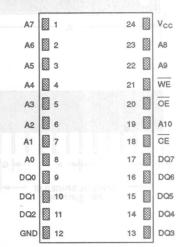


## DS1220Y 16K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- · Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ± 10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



24-Pin Encapsulated Package (720 mil Extended)

#### PIN DESCRIPTION

A<sub>0</sub>-A<sub>10</sub> - Address Inputs
CE - Chip Enable
GND - Ground

 DQ0-DQ7
 - Data In/Data Out

 VCC
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

#### DESCRIPTION

The DS1220Y 16K Nonvolatile SRAM is a 16,384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be

used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

## 1

#### **OPERATION**

#### READ MODE

The DS1220Y executes a read cycle whenever WE (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A<sub>0</sub>-A<sub>10</sub>) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t<sub>ACC</sub> (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either t<sub>CO</sub> for  $\overline{CE}$  or t<sub>OE</sub> for  $\overline{OE}$  rather than address access.

#### WRITE MODE

The DS1220Y is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout

the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in t<sub>ODW</sub> from its falling edge.

#### **DATA RETENTION MODE**

The DS1220Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1220Y constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

### ABSOLUTE MAXIMUM RATINGS\*

Voltage on Any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature

-0.3V to +7.0V 0°C to +70°C; -40°C to +85°C for IND parts -40°C to +70°C; -40°C to +85°C for IND parts 260°C for 10 seconds

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	a sesso na saminos
Input Logic 1 flow y/aqua and b	North SVIH moth	2.2	rebbs nedtra	V <sub>CC</sub>	of to Value	elther to
Input Logic 0	V <sub>IL</sub>	0.0		+0.8	V	,888,7

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	o Huo lingaini	-1.0	ling edge of	+1.0	μА	da ana savo
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0	to egge grie	+1.0	μА	el eloyo efe NE All se
Output Current @ 2.4V	Іон	-1.0			mA	
Output Current @ 0.4V	loL	2.0			mA	
Standby Current CE = 2.2V	I <sub>CCS1</sub>	1	3.0	7.0	mA	
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>		2.0	4.0	mA	
Operating Current t <sub>CYC</sub> =200ns (Commercial)	I <sub>CCO1</sub>			75	mA	
Operating Current t <sub>CYC</sub> =200ns (Industrial)	I <sub>CCO1</sub>			85	mA	
Write Protection Voltage	V <sub>TP</sub>		4.25		V	

#### DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>VO</sub>		· 5	12	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC}$ =5.0V  $\pm$  10%)

#¥ 1x1	HIV.	DS122	OY-100	DS122	OY-120	DS122	20Y-150	DS122	0Y-200		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Read Cycle Time	t <sub>RC</sub>	100	0-1-10	120	1//	150	/ 35	200		ns	
Access Time	tACC		100	1	120	- Markey	150		200	ns	
OE to Output Valid	toE		50	VI	60	111	70		100	ns	
CE to Output Valid	tco	Volum	100	3001	120		150		200	ns	
OE or CE to Output Active	tCOE	5	188	5		5		5		ns	5
Output High Z from Deselection	top		35		35		35	(6), (7)	35	ns	5
Output Hold from Address Change	tон	5		5	X	5	NGCIA	5		ns	
Write Cycle Time	twc	100		120	100	150		200		ns	
Write Pulse Width	t <sub>WP</sub>	75	ux X	90	111	100	30	150		ns	3
Address Setup Time	t <sub>AW</sub>	0		0	V	0	566	0		ns	
Write Recovery Time	t <sub>WR</sub>	10	T	10	7	10		10		ns	
Output High Z from WE	topw	in st	35	XX	35	XX	35		35	ns	. 5
Output Active from WE	toew	5		5		5	-	5		ns	5
Data Setup Time	t <sub>DS</sub>	40		50		60	-	80		ns	4
Data Hold Time	t <sub>DH</sub>	10		10		10		10		ns	4

#### **AC TEST CONDITIONS**

Output Load: 100pF + 1TTL Gate

Input Pulse Levels: 0-3.0V

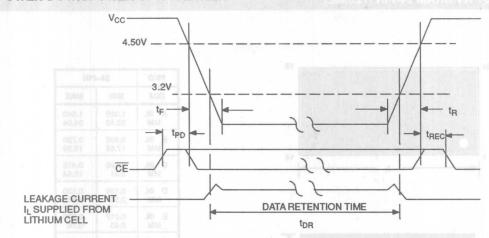
Timing Measurement Reference Levels

Input:1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

#### POWER-DOWN/POWER-UP CONDITION



#### POWER-DOWN/POWER-UP TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0	1 1 1 1	μѕ	10
t <sub>F</sub>	V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	100	N. A. Salar	μѕ	
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0	DUAL SPACES	μѕ	
tREC	CE at V <sub>IH</sub> after Power-Up		2	ms	

 $(t_A = 25^{\circ}C)$ 

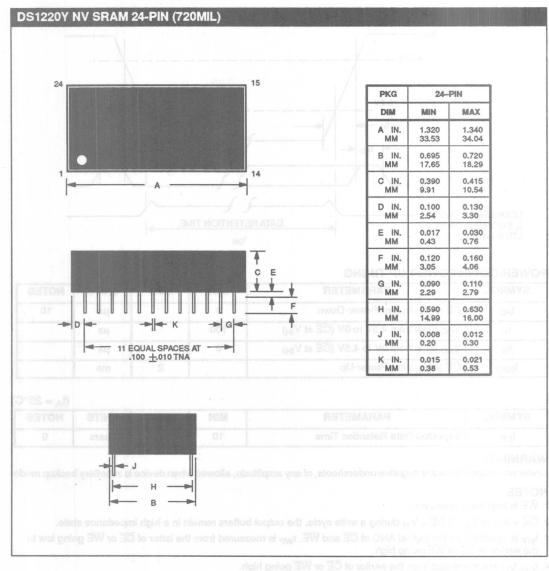
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10		years	9

#### WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during a write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the CE low transition occurs simultaneously with or later than the WE low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- In a power down condition the voltage on any pin may not exceed the voltage of V<sub>CC</sub>.



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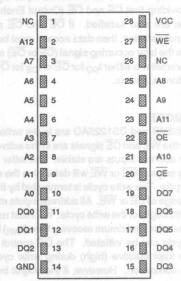


## DS1225AB/AD 64K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of Vcc.
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EE-PROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 150ns, 170ns, or 200ns read access times
- · Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### PIN ASSIGNMENT



28-Pin Encapsulated Package (720 Mil Extended)

#### **PIN DESCRIPTION**

A0 - A12	- Address Inputs
CE	- Chip Enable

GND - Ground

DQ0-DQ7 - Data In/Data Out

VCC - Power (+5V)

WE - Write Enable

OE - Output Enable

NC - No Connect

#### DESCRIPTION

The DS1225AB and DS1225AD 64K Nonvolatile SRAMs are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data.

The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225AB/AD also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

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#### **OPERATION**

#### **READ MODE**

The DS1225AB and DS1225AD execute a read cycle whenever WE (Write Enable) is inactive (high) and CE (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A<sub>0</sub>-A<sub>12</sub>) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t<sub>ACC</sub> (Access Time) after the last address input signal is stable, providing that CE and OE (Output Enable) access times are also satisfied. If OE and CE access times are not satisfied, then data access must be measured from the later occurring signal (CE or OE) and the limiting parameter is either t<sub>CO</sub> for CE or t<sub>OE</sub> for OE rather than address access.

#### WRITE MODE

The DS1225AB and DS1225AD are in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (twR) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has

been enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in topy from its falling edge.

#### **DATA RETENTION MODE**

The DS1225AB provides full functional capability for V<sub>CC</sub> greater than 4.75 volts and write protects at 4.5 volts. The DS1225AD provides full functional capability for V<sub>CC</sub> greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V<sub>CC</sub> without any additional support circuitry. The NV SRAM constantly monitors V<sub>CC</sub>. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V<sub>CC</sub> falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V<sub>CC</sub> rises above approximately 3.0 volts, the power switching circuit connects external V<sub>CC</sub> to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V<sub>CC</sub> exceeds 4.5 volts for the DS1225AD and 4.75 volts for the DS1225AB.

#### FRESHNESS SEAL

The DS1225AB and DS1225AD are shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

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#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground
Operating Temperature
Storage Temperature
Occ to +70°C; -40°C to +85°C for IND parts
-40°C to +70°C; -40°C to +85°C for IND parts
-40°C to +70°C; -40°C to +85°C for IND parts
-40°C for 10 seconds

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	Vcc	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V <sub>CC</sub>	4.50	5.0	5.5	V	THE RESIDENCE
Logic 1	VIH	2.2		V <sub>CC</sub>	V	olu O at 3
Logic 0	V <sub>IL</sub>	0.0	1 8	+0.8	V	4 25 to 3

(0°C to 70°C; V<sub>CC</sub>=5V ± 10% for DS1225AD)

#### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0	081	+1.0	μА	alasta adal
I/O Leakage Current CE>V <sub>IH</sub> <v<sub>CC</v<sub>	I <sub>IO</sub>	05-1.0	100	+1.0	μА	Vitte Pulse
Output Current @2.4V	Іон	-1.0		VEA.	mA	PO BERADA
Output Current @0.4V	loL	2.0		2100	mA	
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>	Ave.	3.0	5.0	mA	
Operating Current t <sub>CYC</sub> =200ns (Commercial)	I <sub>CC01</sub>	01	10	75	mA	biol-i atak
Operating Current t <sub>CYC</sub> =200ns (Industrial)	I <sub>CC01</sub>			85	mA	TEST O
Write Protection Voltage (DS1225AB)	V <sub>TP</sub>	4.50	4.62	4.75	evelvo urement Re	out Puise I ning Mean
Write Protection Voltage (DS1225AD)	V <sub>TP</sub>	4.25	4.37	4.5	VeV duq	Ou out Pulse

#### DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### CAPACITANCE

(t<sub>A</sub> =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	t Orone	5	10	pF	mail egeno
Input/Output Capacitance	C <sub>VO</sub>	tringal, 4	5	10	pF	-

transful code of enurope 3. bedget for all notine lines (0°C to 70°C;  $V_{CC}$ =5.0V  $\pm$  10% for DS1225AD) AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V<sub>CC</sub>=5.0V ± 5% for DS1225AB)

		DS12	25-150	DS12	25-170	DS12	25-200	R ATTOMS	Recossil
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	tRC	150	tunian incom	170		200	Clay share	ns	0.82000.07
Access Time	tACC		150	en a	170		200	ns	
OE to Output Valid	toE		70		80	-	100	ns	
CE to Output Valid	tco		150		170		200	ns	1 0000
OE or CE to Output Active	tCOE	5		5	-  Y	5		ns	5
Output High Z from Deselection	top	07 to 70 °C to 7	35	3 7	35	HAST:	35	ns	5
Output Hold from Address Change	фон	5		5	Toeru	5	AS.	ns	
Write Cycle Time	twc	150		170	.]]	200		ns	TOTAL TOTAL
Write Pulse Width	twp	100		120	. 08	150		ns	3
Address Setup Time	t <sub>AW</sub>	0		0	estimação mono	0		ns	
Write Recovery Time	t <sub>WR</sub>	10	distribution of	10	110	10		ns	
Output High Z from WE	topw	0.5	35		35		35	ns	5
Output Active from WE	toew	5		5	1200	5		ns	5
Data Setup Time	t <sub>DS</sub>	60	-	70	1500	80	- On	ns	4
Data Hold Time	t <sub>DH</sub>	10		10	160001	10	entrang.	ns	4

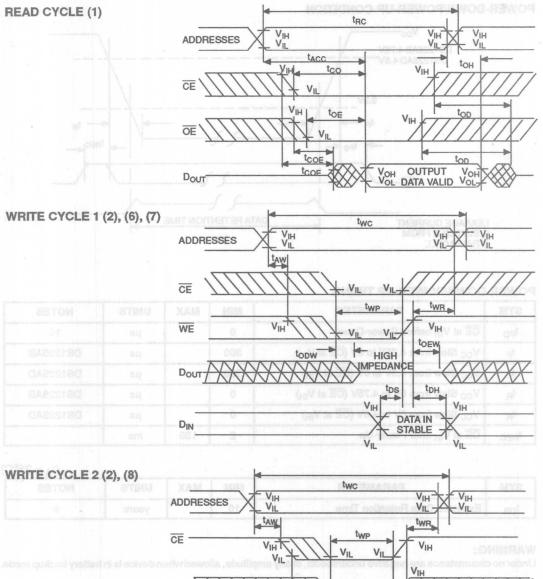
AC TEST CONDITIONS
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V

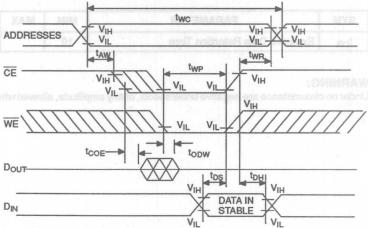
Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

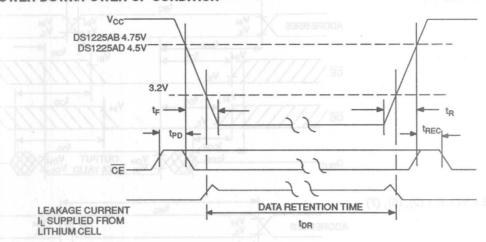








#### POWER-DOWN/POWER-UP CONDITION



#### POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0	SIVV	μs	10
t <sub>F</sub>	V <sub>CC</sub> Slew from 4.75V to 0V (CE at V <sub>IH</sub> )	300		μs	DS1225AB
tF	V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300	Dout	μs	DS1225AD
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.75V (CE at V <sub>IH</sub> )	0		μs	DS1225AB
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.5V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	0	- 0	μs	DS1225AD
tREC	CE at VIH after Power-Up	2	125	ms	

 $(t_A = 25^{\circ}C)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10	ESMUUM.	years	9

#### **WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

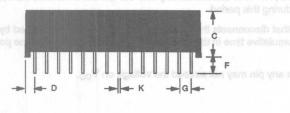
#### NOTES

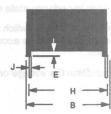
- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{II}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1225AB/AD has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the
  user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is
  first applied by the user.
- 10. In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

0.012	

#### DS1225AB/AD NONVOLATILE SRAM 28-PIN 720 MIL MODULE







PKG	28-F	MI
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395 10.03	0.415 10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017 0.43	0.030 0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008	0.012
MM	0.20	0.30
K ÍN.	0.015	0.021
MM	0.38	0.53

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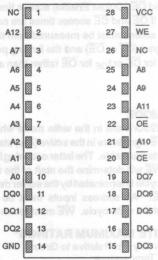
# **DALLAS**SEMICONDUCTOR

# DS1225D/E 64K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, or 120 ns read access times
- · Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



28-Pin Encapsulated Package (740 Mil Flush Bottom)

#### **PIN DESCRIPTION**

A0 - A12	- Address Inputs
CE	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
Vcc	- Power (+5V)
WE	- Write Enable
ŌĒ	- Output Enable
NC OO	- No Connect
NOTE: Pins 1	& 26 missing by design

#### DESCRIPTION

The DS1225D and DS1225E are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be

used in place of existing 8Kx 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225D/E also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

#### READ MODE

The DS1225D/E executes a read cycle whenever WE (Write Enable) is inactive (high) and  $\overline{\text{CE}}$  (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  (Output Enable) access times are also satisfied. If  $\overline{\text{OE}}$  and  $\overline{\text{CE}}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{\text{CE}}$  or  $\overline{\text{OE}}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{\text{CE}}$  or  $t_{OE}$  for  $\overline{\text{OE}}$  rather than address access

#### WRITE MODE

The DS1225D/E are in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topy from its falling edge.

#### **DATA RETENTION MODE**

The DS1225E provides full functional capability for V<sub>CC</sub> greater than 4.75 volts and write protects at 4.5 volts. The DS1225D provides full functional capability for V<sub>CC</sub> greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V<sub>CC</sub> without any additional support circuitry. The DS1225D/E constantly monitors V<sub>CC</sub>. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As Vcc falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external V<sub>CC</sub> to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V<sub>CC</sub> exceeds 4.5 volts for the DS1225D and 4.75 volts for the DS1225E.

-0.3V to +7.0V 0°C to +70°C; -40°C to +85°C for IND parts -40°C to +70°C; -40°C to +85°C for IND parts 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225D Power Supply Voltage	Vcc	4.50	5.0	5.5	V	
DS1225E Power Supply Voltage	Vcc	4.75	5.0	5.25	V	
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub>	VMOS	ESCRIP
Logic 0	V <sub>IL</sub>	0.0	6-bit, fully st	+0.8	18CV	ha D\$122

(0°C to 70°C;  $V_{CC}=5V \pm 10\%$  for DS1225D) (0°C to 70°C;  $V_{CC}=5V \pm 5\%$  for DS1225E)

## DC ELECTRICAL CHARACTERISTICS

0.00 0.00 0.00 0.00	186.557886		BIO 8 18 18 18			
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	CAMPL MB	-1.0	MIN XAN	+1.0	μΑ	PARAMI
I/O Leakage Current CE>V <sub>IH</sub> <v<sub>CC</v<sub>	I <sub>IO</sub> 00	-1.0	85	+1.0	μΑ	kyO bsef
Output Current @2.4V	loH	-1.0			mA	STA SSISTOR
Output Current @0.4V	loL	2.0	96		mA	DE to Outp
Standby Current CE = 2.2V	Iccs1	78	5.0	10.0	mA	abu O ot To
Standby Current $\overline{\text{CE}} = \text{V}_{\text{CC}}\text{-0.5V}$	I <sub>CCS2</sub>		3.0	5.0	mA	bild/
Operating Current t <sub>CYC</sub> =100ns (Commercial)	I <sub>CC01</sub>		8	75	mA S	DE or GE of Output Act
Operating Current t <sub>CYC</sub> =100ns (Industrial)	I <sub>CC01</sub>	25	25	85	mA S	Sutput High com Dese
Write Protection Voltage (DS1225D)	V <sub>TP</sub>	4.50	4.62	4.75	anga to	Output Horo Address On
Write Protection Voltage (DS1225E)	V <sub>TP</sub>	4.25	4.37	4.5	V	Vrite Cycle

# DC TEST CONDITIONS

**Outputs Open** 

All Voltages Are Referenced to Ground.

#### CAPACITANCE

(t<sub>A</sub> =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	IDA Molio
Input/Output Capacitance	C <sub>VO</sub>		5	10	pF	or the Codes

# AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}; V_{\text{CC}}=5.0\text{V} + 10\% \text{ for DS1225D})$ (0°C to 70°C; V<sub>CC</sub>=5.0V ± 5% for DS1225E)

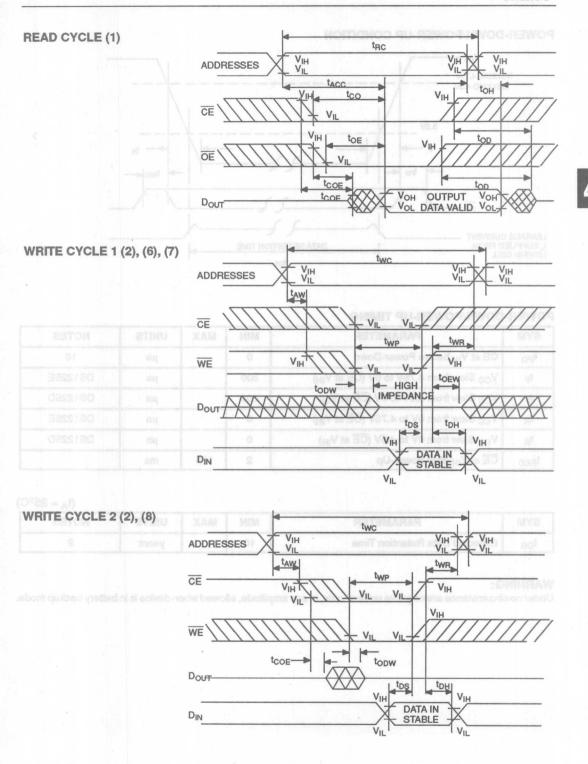
earon emin		DS12	25D/E-70	DS12	25D/E-85	DS122	5D/E-100	DS1225D/E-120		PARAS	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	70		85	0.1-	100	Dist.	120	(7 mi	ns	I/O Leaks
Access Time	tACC		70		85		100		120	ns	O tuesto O
OE to Output Valid	toE		35		45		50		60	ns	Output C
CE to Output Valid	tco	5.0	70	e	85	100	100	Va.o.	120	ns	Standay
OE or CE to Output Active	tCOE	5		5		5	bol	5	f=ovel	ns	nilm5qO punmoO)
Output High Z from Deselection	top	85	25		25	·	25	gn00	25	ns	nites5q0 indeubni)
Output Hold from Address Change	<sup>‡</sup> ОН	5	- \$1	5	4.50	5	TΛ	5	ingsile	ns	Write Pri (DS 1225
Write Cycle Time	twc	70	7	85	4.25	100	W	120	рунас	ns	Write Pre
Write Pulse Width	t <sub>WP</sub>	55		65		75		90		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		0		0	Мош	ns	Outputs C
Write Recovery Time	twR	10		10		10	.8713	10	soneras	ns	QuileV ib
Output High Z from WE	topw	XAM	25	r T	25	1.0	25		25	ns	5
Output Active from WE	toew	5		5		5	0	5		ns	5
Data Setup Time	t <sub>DS</sub>	30	J	35		40	80	50	901,851101	ns	4
Data Hold Time	t <sub>DH</sub>	10		10		10		10		ns	4

AC TEST CONDITIONS
Output Load: 100 pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V

Timing Measurement Reference Levels

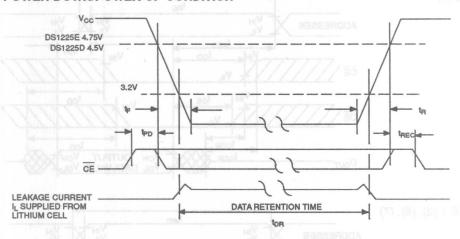
Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5ns



012292 5/8

## POWER-DOWN/POWER-UP CONDITION



## POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0	2007	μs	10
tr	V <sub>CC</sub> Slew from 4.75V to 0V (CE at V <sub>IH</sub> )	300		μs	DS1225E
tF	V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300		μs	DS1225D
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.75V (CE at V <sub>IH</sub> )	0	-	μs	DS1225E
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0		μѕ	DS1225D
tREC	CE at VIH after Power-Up	2	125	ms	

 $(t_A = 25^{\circ}C)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10	BERODA	years	9

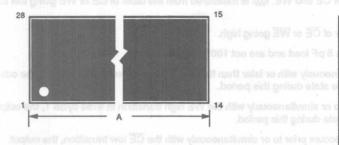
# **WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

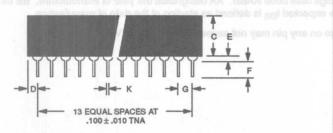
#### NOTES

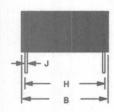
- 1. WE is high for a Read Cycle.
- 2.  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  or  $\text{V}_{\text{IL}}$ . If  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  during write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the CE high transition occurs prior to or simultaneously with the WE high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1225D/E is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- 10. In a power down condition the voltage on any pin may not exceed the voltage on Vcc.

# DS1225D/E NONVOLATILE SRAM 28-PIN 740 MIL MODULE



	PKG	28-PIN		
	DIM	MIN	MAX	
	A IN.	1.520 38.61	1.540 39.12	
	MM	0.695 17.65	0.720 18.29	
	I G IN. I	0.350 8.89	0.375 9.53	
	H BARA I	0.100 2.54	0.130 3.30	
	E IN.	0.015 0.38	0.035 0.89	
s expected t <sub>DS</sub> is defi- te on any pin may not	F IN.	0.110 2.79	0.140 3.56	
- A	G IN.	0.090 2.29	0.110 2.79	
F	H IN.	0.590 14.99	0.630 16.00	
T	J IN.	0.008 0.20	0.012 0.30	
	K IN.	0.015 0.38	0.021 0.53	





# **DALLAS**SEMICONDUCTOR

# DS1225Y 64K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EE-PROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 150ns, 170ns, or 200ns read access times
- · Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**

NC		le fon ers sem	28	VCC
A12		2 and aroni bena	27	
A7		3	26	NC
A6		4	25	A8
A5		5	24	A9
A4		6 ebom estav o	23	A11
АЗ		7 (wol) suitos e	22	OE male 10 tons
A2		8 Thrusas Talks	21	A10
A1		9	20	CE
A0		10	19	DQ7
DQ0	8	11	18	DQ6
DQ1		12	17	DQ5
DQ2		13	16	DQ4
GND		14	15	DQ3

28-Pin Encapsulated Package (720 Mil Extended)

#### PIN DESCRIPTION

A <sub>0</sub> - A <sub>12</sub>	- Address Inputs
CE	- Chip Enable
GND	- Ground
DQ <sub>0</sub> -DQ <sub>7</sub>	- Data In/Data Out
Vcc	- Power (+5V)
WE	- Write Enable
OE	- Output Enable
NC	- No Connect

#### DESCRIPTION

The DS1225Y 64K Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be

used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

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#### **OPERATION**

#### **READ MODE**

The DS1225Y executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A<sub>0</sub>-A<sub>12</sub>) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

## WRITE MODE

The DS1225Y is in the write mode whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout

the write cycle.  $\overline{\text{WE}}$  must return to the high state for a minimum recovery time ( $t_{\text{WR}}$ ) before another cycle can be initiated. The  $\overline{\text{OE}}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ( $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  active) then  $\overline{\text{WE}}$  will disable the outputs in  $t_{\text{ODW}}$  from its falling edge.

#### **DATA RETENTION MODE**

The DS1225Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1225Y constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature
O°C to +70°C; -40°C to +85°C for IND parts
-40°C to +70°C; -40°C to +85°C for IND parts
260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

(Ecolimital Para Co. El			and the same of th	75 2 2 2		0 0 10 10
PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	Colection
Input Logic 1	V <sub>IH</sub>	2.2	l a l	Vcc	-b.V.nort	NeH teglirO
Input Logic 0	V <sub>IL</sub>	0.0		+0.8	V	U.S. 1.2 82840

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

DC ELECTRICAL CHARACTERISTICS				100101	O C, VCC	= 5V I 10%
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0	101	+1.0	μА	coell ethil/
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0	ā	+1.0	μΑ	Output Add
Output Current @ 2.4V	I <sub>ОН</sub>	-1.0	08	so <sup>‡</sup>	mA	Data Setup
Output Current @ 0.4V	loL	2.0	101	Hol .	mA	Cata Hold
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5	10	mA	marin.
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>		3	5	mA	Dulgut Lond
Operating Current t <sub>CYC</sub> =200ns (Commercial)	I <sub>CCO1</sub>			75	mA	nesur zuen wehl gelmi raunt
Operating Current t <sub>CYC</sub> =200ns (Industrial)	I <sub>CCO1</sub>			85	mA	nput Pulse
Write Protection Voltage	V <sub>TP</sub>		4.25		V	10

## DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

#### AC ELECTRICAL CHARACTERISTICS

C to 70°C, Vcc=5	$.0V \pm 10\%$
------------------	----------------

AC ELECTRICAL CHA	INOTEINOT	_				-		* 00-0.0	DA T 101
national CIVII and I	TOTAL METERS	DS122	25Y-150	DS122	25Y-170	DS122	25Y-200	AND THE	no agrano
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	tRC	150	J. 90%	170		200	970	ns	Brissenso
Access Time	tACC	aolyab	150	iterago	170	ond fu	200	ns	s al aidT
OE to Output Valid	toE	on is no	70	e eiffi to	80	nother	100	ns	ni ezoni
CE to Output Valid	tco		150		170		200	ns	
OE or CE to Output Active	t <sub>COE</sub>	5	814 184	5	NG CO	5	10 00 G	ns	5
Output High Z from Deselection	a a top	5,0	35		35		35	ns	5
Output Hold from Address Change	<sup>t</sup> OH	5	3.5	5	MA.	5		ns	no Litan
Write Cycle Time	twc	150		170		200		ns	
Write Pulse Width	t <sub>WP</sub>	100		120	BONTAU	150	MAHO.	ns	3
Address Setup Time	t <sub>AW</sub>	0	1000	0	BEHNS	0	RHT	ns	
Write Recovery Time	twR	10	0.1	10	gl	10	John	ns	sell Juga
Output High Z from WE	topw		35		35		35	ns	5
Output Active from WE	toew	5		5		5		ns	5
Data Setup Time	t <sub>DS</sub>	60	0.1	70	HO	80	Va.s	ns	4
Data Hold Time	t <sub>DH</sub>	10	0.5	10	loc	10	VINC	ns	0 4 4

## **AC TEST CONDITIONS**

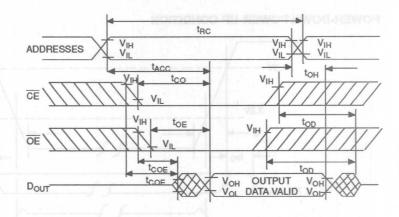
Output Load: 100pF+1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

# CAPACITANCE

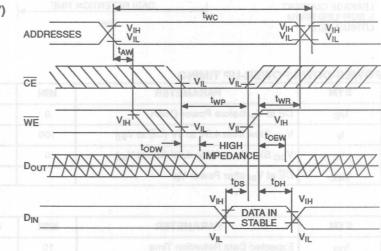
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	CIN		10	pF	DO TEST O
Input/Output Capacitance	C <sub>VO</sub>		10	pF	Tiedo Rindi

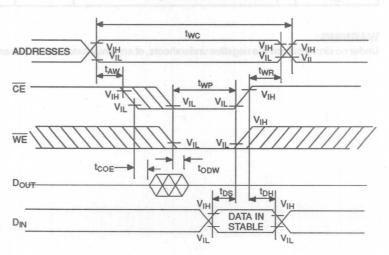




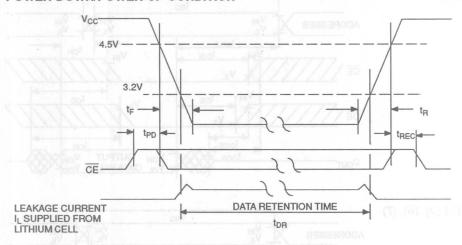
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



# POWER-DOWN/POWER-UP CONDITION



## POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES	
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0		μs	10	
t <sub>F</sub>	V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	100		μs		
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0		μs		
tREC	CE at V <sub>IH</sub> after Power-Up	AAT 1000	2	ms		

 $(t_A = 25^{\circ}C)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10		years	9

#### WARNING.

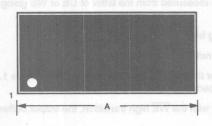
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

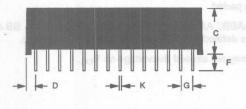
#### NOTES

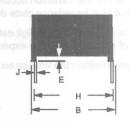
- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during a write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- 10. In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.



# DS1225Y NONVOLATILE SRAM 28-PIN 720 MIL MODULE







PKG	28-	NP
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN. MM		0.720 18.29
C IN.	0.395 10.03	0.415 10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



# DS1230Y/AB 256K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during the decrease in V<sub>CC</sub> at power loss
- Directly replaces 32K x 8 volatile static RAM or EE-PROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, 120, 150, or 200 ns read access times
- · Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



28-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

# **PIN DESCRIPTION**

 A0 - A14
 - Address Inputs

 CE
 - Chip Enable

 GND
 - Ground

 DQ0 - DQ7
 - Data In/Data Out

 V<sub>CC</sub>
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

#### DESCRIPTION

The DS1230AB and DS1230Y 256K Nonvolatile SRAMs are a 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent

garbled data. The NV SRAM can be used in place of existing 32K x 8 static RAMs directly conforming to the popular bytewide 28 pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

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#### **READ MODE**

The DS1230Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 15 address inputs ( $A_0$  -  $A_{14}$ ) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

#### WRITE MODE

The DS1230Y/AB is in the write mode whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are in the active (low) state after address inputs are stable. The later occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in  $t_{ODW}$  from its falling edge.

#### **DATA RETENTION MODE**

The DS1230AB provides full functional capability for  $V_{\rm CC}$  greater than 4.75 volts and write protects at 4.5

volts. The DS1230Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAM constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts for DS1230Y and 4.75 volts for the DS1230AB.

#### FRESHNESS SEAL AND SHIPPING

The DS1230Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V<sub>CC</sub> is first applied at a level of greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

#### **BATTERY REDUNDANCY**

Battery redundancy is provided to ensure reliability. The DS1230Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

# ABSOLUTE MAXIMUM RATINGS\*

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO 70°C, -40°C TO +85°C FOR IND PARTS -40°C TO +70°C, -40°C TO +85°C FOR IND PARTS 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES			
DS1230AB Power Supply Voltage	Vcc	4.75	5.0	5.25	won Address	skol-i tucyu			
DS1230Y Power Supply Voltage	Vcc	4.5	5.0	5.5	V	Inite Cycle			
Logic 1 an 3X	V <sub>IH</sub>	2.2	aa	Vcc	VibiV	nto Pidsel			
Logic 0	VIL	0.0	0 1	0.8	V	al eemitt			

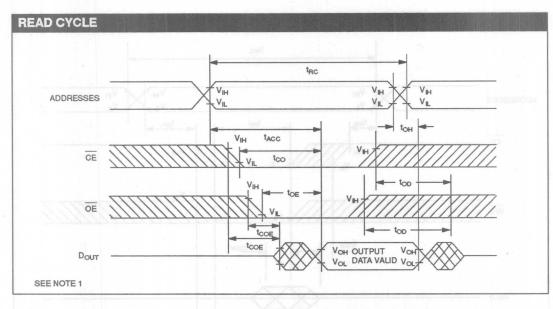
DC ELECTRICAL CHARACT	DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1230AB) (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS1230Y)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES					
Input Leakage Current	liL	-1.0		+1.0	μА						
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0	YGESTEG	+1.0	μА						
Output Current @ 2.4V	Іон	-1.0	ensa.	UNIVESTINE T CL	mA						
Output Current @ 0.4V	loL	2.0	est	ont	mA	olovO bee					
Standby Current CE = 2.2V	I <sub>CCS1</sub>	051	5.0	10.0	mA	amil' seuss					
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>	000	3.0	5.0	mA						
Operating Current	I <sub>CCO1</sub>	a	a l	85	mA	ed 3 O no 3					
Write Protection Voltage (DS1230AB)	V <sub>TP</sub>	4.50	4.62	4.75	V Z from Deser-	rigil-i tuquu					
Write Protection Voltage (DS1230Y)	V <sub>TP</sub>	4.25	4.37	4.5	seaboX mort	biol-l sucto					

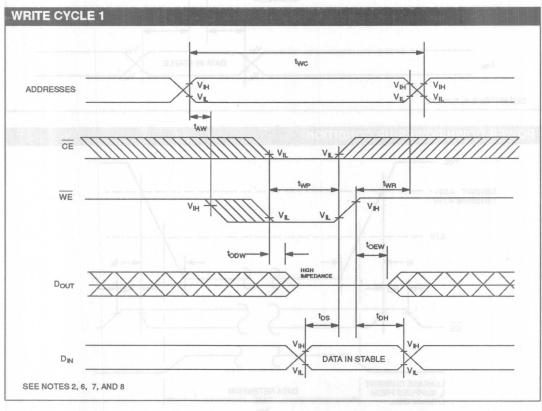
CAPACITANCE (t <sub>A</sub> = 25°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Input Capacitance	CIN	26	5	10	pF	rinii-i tuatu		
Input/Output Capacitance	C <sub>VO</sub>	8	5	10	pF	kitoA Juejei		

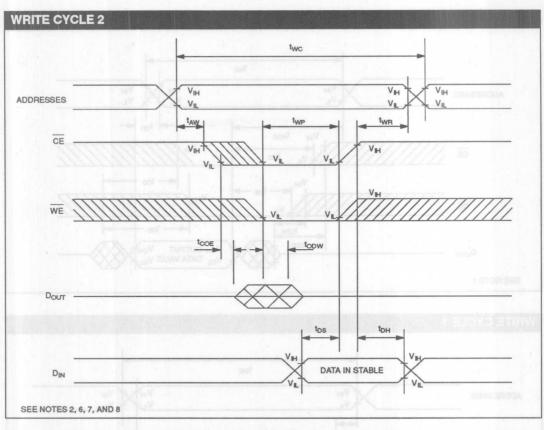
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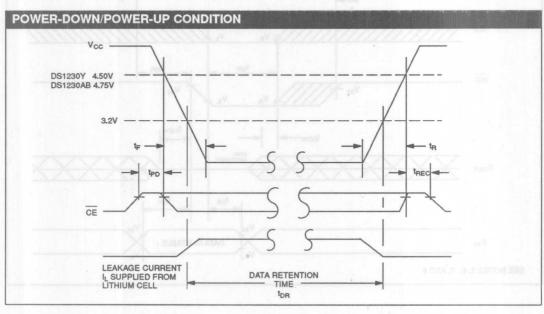
PARAMETER	SYMBOL	DS1230Y-70 DS1230AB-70		DS1230Y-85 DS1230AB-85		DS1230Y-100 DS1230AB-100		UNITS	NOTES
TATAMETER	SECONDS	MIN	MAX	MIN	MAX	MIN	MAX	HWETE	SIRBOUC
Read Cycle Time	t <sub>RC</sub>	70		85		100		ns	
Access Time	tACC	balloni	70	deolitor	85	a anoilo	100	ns	betroib
OE to Output Valid	toE		35	n toella	45	I to abo	50	ns	ancitiba
CE to Output Valid	tco		70		85	alexanticalia a	100	ns	
OE or CE to Output Active	tcoe	5		5	The State of	5		ns	5
Output High Z from Deselection	top	917	25		30		35	ns	M 5 1A
Output Hold from Address Change	tон	5		5	20	5	Árdeloc	ns	egatio
Write Cycle Time	twc	70	-8,	85	99V	100	ox Arddi	ns	A DESTIN
Write Pulse Width	t <sub>WP</sub>	55	9.	65	HIV	75		ns	3
Address Setup Time	t <sub>AW</sub>	0	0	0	.W	0		ns	D sied
Write Recovery Time	t <sub>WR</sub>	15		15		15	Pettiniano inchi	ns	
Output High Z from WE	topw		25		30		35	ns	5
Output Active from WE	toew	5		5		5		ns	5
Data Setup Time	t <sub>DS</sub>	30		35	THE COLUMN	40		ns	4
Data Hold Time from WE	t <sub>DH</sub>	15	1	15	WORLD TO	15		ns	4

PARAMETER	SYMBOL	DS1230Y-120 DS1230AB-120		DS1230Y-150 DS1230AB-150		DS1230Y-200 DS1230AB-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	de Inemi	O Meno
Read Cycle Time	t <sub>RC</sub>	120	1 0	150	Joi	200	V5.1	ns	O Judjul
Access Time	tACC	5.0	120		150		200	ns	yebest
OE to Output Valid	toE	8.0	60		70	To Visit	100	ns	Land Control
CE to Output Valid	tco		120		150		200	ns	
OE or CE to Output Active	tCOE	5	-	5	100001	5	ne self.	ns	5
Output High Z from Dese- lection	top		35		35		35	ns 🕒	5
Output Hold from Address Change	tон	5		5	414	5	th period	ns	085190
Write Cycle Time	twc	120		150		200		ns	
Write Pulse Width	t <sub>WP</sub>	90		100	Resident Control	100		ns	3
Address Setup Time	t <sub>AW</sub>	0	Tel Je	0	ngaye	0		ns	DAKADA
Write Recovery Time	twR	15		15		15		ns	
Output High Z from WE	topw	10.7	35		35		35	ns	5
Output Active from WE	toew	5		5	ONR	5	eoristic	ns	5
Data Setup Time	t <sub>DS</sub>	50		60		80		ns	4
Data Hold Time from WE	t <sub>DH</sub>	15	100	15		15		ns	4









POWER-DOWN/POWER-UP TIMING								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
CE, at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0			μѕ	12		
V <sub>CC</sub> slew from 4.75V to 0V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	t <sub>F</sub>	300			μѕ	DS1230AB		
V <sub>CC</sub> slew from 4.5V to 0V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	t <sub>F</sub>	300			μѕ	DS1230Y		
V <sub>CC</sub> slew from 0V to 4.5V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	t <sub>R</sub>	0			μѕ	DS1230Y		
V <sub>CC</sub> slew from 0V to 4.75V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	t <sub>R</sub>	0			μs	DS1230Y		
CE, at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>	2		125	ms			

(t <sub>A</sub> = 25°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Expected Data Retention Time	t <sub>DR</sub>	10			years	9, 11				

#### WARNING

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a Read Cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1230Y has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as ac-

- cumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- 11. The expected data retention time for parts designated IND meet or exceed the specified t<sub>DR</sub> at 25°C. IND parts which are continuously exposed to 85°C will have a t<sub>DR</sub> of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t<sub>DR</sub> of 7 years.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

#### DC TEST CONDITIONS

Outputs Open

Cycle = 200 ns for operating current All voltages are referenced to ground

#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V

Timing Measurement Reference Levels

Input: 1.5V Output: 1.5V

Input pulse Rise and Fall Times: 5 ns

#### DS1230Y/AB NONVOLATILE SRAM 28 PIN 740 MIL MODULE B -28-PIN PKG DIM MIN MAX A IN. 1.520 1.540 MM 39.12 38.61 B IN. 0.740 0.720 18.29 18.80 0.415 C IN. 0.395 MM 10.03 10.54 D IN. 0.100 0.130 2.54 3.30 0.030 E IN. 0.017 MM 0.43 0.76 F IN. 0.160 0.120 3.05 4.06 G IN. 0.090 0.110 2.79 H IN. 0.590 0.630 MM J IN. 0.008 0.012 0.20 0.30 0.015 0.021

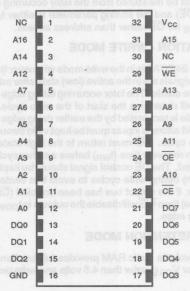
# **DALLAS**SEMICONDUCTOR

# DS1245Y/AB 1024K Nonvolatile SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM or EE-PROM
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in 70, 85, 100 or 120 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1245Y)
- Optional ±5% operating range (DS1245AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

#### **PIN DESCRIPTION**

 A0 - A16
 Address Inputs

 CE
 Chip Enable

 GND
 Ground

 DQ0 - DQ7
 Data In/Data Out

 VCC
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

 NC
 - No Connect

#### DESCRIPTION

The DS1245Y/AB 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1245Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to un-

conditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

#### OPERATION - READ MODE

The DS1245Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A $_0$  - A $_{16}$ ) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $\overline{OE}$  for  $\overline{OE}$  rather than address access.

#### **OPERATION - WRITE MODE**

The DS1245Y/AB is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topw from its falling edge.

#### **DATA RETENTION MODE**

The nonvolatile static RAM provides full functional capability for V<sub>CC</sub> greater than 4.5 volts and write protects

by 4.37 volts nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1245AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1245Y constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts (4.75 volts for the DS1245AB).

#### FRESHNESS SEAL AND SHIPPING

The DS1245Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

#### **BATTERY REDUNDANCY**

Battery redundancy is provided to ensure reliability. The DS1245Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

# **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO 70°C, -40°C TO + 85°C FOR IND PARTS -40°C TO +70°C, -40°C TO +85°C FOR IND PARTS 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

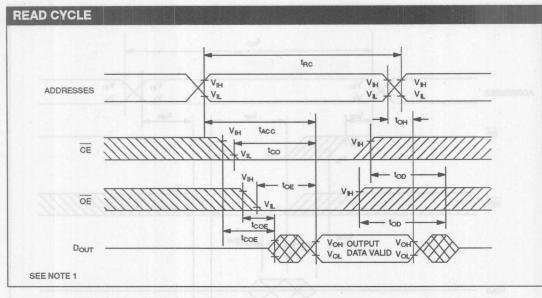
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1245Y Power Supply Voltage	Vcc	4.5	5.0	5.5	entro V non I	Pal-LuqtuC Disenge
DS1245AB Power Supply Voltage	Vcc	4.75	5.0	5.25	Vensit	Write Cycle Write Palse
Logic 1	VIH	2.2	6 1 1	V <sub>CC</sub>	VTQ	s 3 see ibb/
Logic 0	VIL	0.0	51   15	+0.8	erVT year	Appel Fact

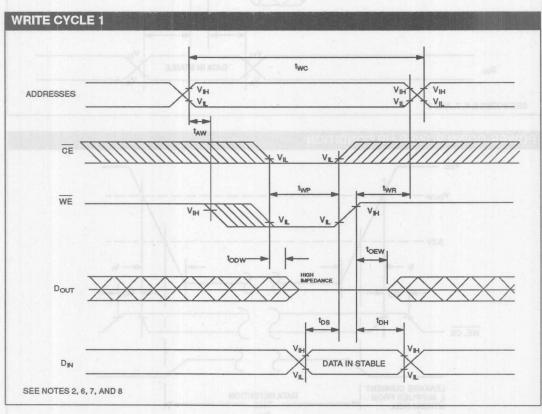
DC ELECTRICAL CHARA	CTERISTICS (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1245AB) (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS1245Y)									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μА					
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	IIO	-1.0	STEEL LOS	+1.0	μА	TEMARA9				
Output Current @ 2.4V	Іон	-1.0	4634		mA					
Output Current @ 0.4V	loL	2.0	301	912	mA	ingo bash				
Standby Current $\overline{\text{CE}}$ = 2.2V	I <sub>CCS1</sub>	001	5.0	10.0	mA	atu Orat TC				
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>	100	3.0	5.0	mA	SE to Out				
Operating Current	I <sub>CCO1</sub>	200		85	mA	edid kantat				
Write Protection Voltage (DS1245Y)	V <sub>TP</sub>	4.25	4.37	4.5	from Address	Supput Hol				
Write Protection Voltage (DS1245AB)	V <sub>TP</sub>	4.50	4.62	4.75	Vamil	Write Cycle				

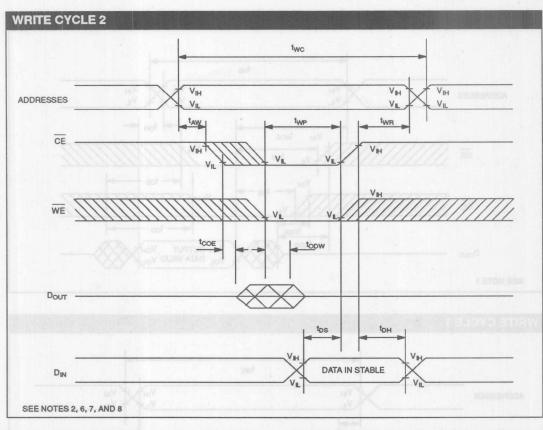
CAPACITANCE (t <sub>A</sub> = 25°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Input Capacitance	CIN		3 5 W	10	pF	Output Addit				
Input/Output Capacitance	C <sub>VO</sub>		5	10	pF	Data Setup				

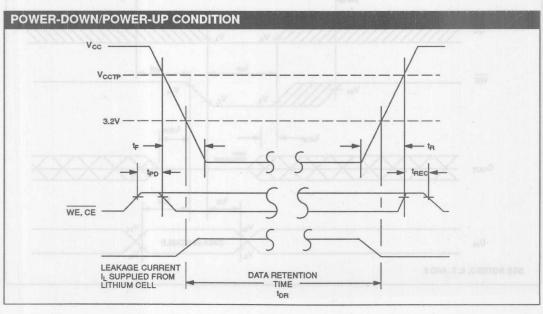
PARAMETER	SYMBOL	DS1245	//AB-70	DS1245	//AB-85	UNITS	NOTES
SON	A 10 \$500	MIN	MAX	MIN	MAX	A TEMPERA	MIREGIN
Read Cycle Time	t <sub>RC</sub>	70		85	at her sale	ns	
Access Time	t <sub>ACC</sub>	ni ton ei n	70	e sint to a	85	ns	nt betenib
OE to Output Valid	toE	- aphilipheir	35	sh emii t	45	ns	endilibre
CE to Output Valid	tco	previous.	70	ESPHITS	85	ns	
OE or CE to Output Active	t <sub>COE</sub>	5		5	SERVE YEAR	ns	5
Output High Z from Deselection	t <sub>OD</sub>	31	25	JUSINIYE	30	ns	5
Output Hold from Address Change	tон	5		5		ns	UST245Y Voltage
Write Cycle Time	twc	70	4.75	85	y y	ns	DETEASAR
Write Pulse Width	t <sub>WP</sub>	55		65		ns	3
Address Setup Time	t <sub>AW</sub>	0	22	0		ns	Logic 1
Write Recovery Time	t <sub>WR</sub>	15	0.0	15		ns	0 olgo
Output High Z from WE	topw		25		30	ns	5
Output Active from WE	toew	5		5	MATERIAL STATE	ns	5
Data Setup Time	t <sub>DS</sub>	30	0	35		ns	4
Data Hold Time	t <sub>DH</sub>	15		15		ns	4

PARAMETER	SYMBOL	DS1245	//AB-100	DS1245	//AB-120	UNITS	NOTES
Am I		MIN	MAX	MIN	MAX	74.5 (D then	uO targiuO
Read Cycle Time	t <sub>RC</sub>	100	00	120		ns	a Ortania C
Access Time	tACC		100		120	ns	
OE to Output Valid	toE	1.0	50	18001	60	ns	o francisco
CE to Output Valid	tco	3.5	100	5890	120	ns	Standoy C
OE or CE to Output Active	tcoe	5		5		ns	5
Output High Z from Deselection	top		35	TOUR!	35	ns	5
Output Hold from Address Change	tон	5		5		ns	(DB1245Y
Write Cycle Time	twc	100	55.8	120		ns	HEATH GENERAL
Write Pulse Width	t <sub>WP</sub>	75		90		ns	3
Address Setup Time	t <sub>AW</sub>	0		0	esantard consti	ns	
Write Recovery Time	t <sub>WR</sub>	15	200	15	Value of the last	ns	
Output High Z from WE	topw	YT .	35	JOHNYE	35	ns	5
Output Active from WE	toew	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	40		50		ns	4
Data Hold Time	t <sub>DH</sub>	15		15		ns	4









POWER-DOWN/POWER-UP TIMING										
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES					
t <sub>PD</sub>	$\overline{\text{CE}}, \overline{\text{WE}}$ at $\text{V}_{\text{IH}}$ before Power-Down	0		μs	12					
t <sub>F</sub>	$V_{CC}$ slew from 4.5V to 0V $(\overline{\text{CE}} \text{ at } V_{\text{IH}})$	300		μs						
t <sub>R</sub>	$V_{CC}$ slew from 0V to 4.5V ( $\overline{CE}$ at $V_{IH}$ )	0		μs						
tREC	CE, WE at V <sub>IH</sub> after Power-Up	2	125	ms						

(t <sub>A</sub> = 25°C)								
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES			
t <sub>DR</sub>	Expected Data Retention Time	10		years	9, 11			

#### WARNING

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a Read Cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- 4.  $t_{DH}$ ,  $t_{DS}$  are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1245Y has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is first applied by the user.

- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- 11. The expected data retention time for parts designated IND meet or exceed the specified t<sub>DR</sub> at 25°C. IND parts which are continuously exposed to 85°C will have a t<sub>DR</sub> of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t<sub>DR</sub> of 7 years.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

#### DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V

Timing Measurement Reference Levels

Input: 1.5V Output: 1.5V

Input pulse Rise and Fall Times: 5 ns

# DS1245Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE 32-PIN PKG MIN MAX DIM A IN. 1.720 1.740 B IN. 0.720 0.740 18.29 18.80 0.415 C IN. 0.395 10.54 D IN. 0.090 0.120 2.29 3.05 E IN. 0.017 0.030 MM 0.43 0.76 F IN. 0.120 0.160 3.05 4.06 G IN. 0.090 0.110 2.29 2.79 H IN. 0.590 0.630 J IN. 0.008 0.012 K IN. 0.015 0.021 0.53

# DALLAS

# DS1245EE 1M Write-Protected NV SRAM

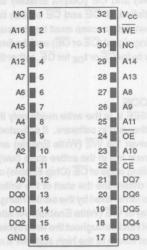
#### **FEATURES**

- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Data retention in the absence of V<sub>CC</sub>
- Directly replaces 128K x 8 EPROM, EEPROM, or FLASH
- Unlimited write cycles
- Standard 32-pin JEDEC pinout
- Available in 120 or 100 read access time
- Full ±10% operating range
- Read cycle time equals write cycle time

#### DESCRIPTION

The DS1245EE is a 1,048,576-bit fully static, nonvolatile SRAM organized as 131,072 words by 8 bits with a software controlled write inhibit function. The nonvolatile memory has a self-contained lithium energy source and control circuit which constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. Two software selectable switches are provided which are capable of inhibiting both the write enable to the RAM and the battery back-up circuitry through a pattern recognition sequence across four address lines. The first switch can

#### **PIN ASSIGNMENT**



32-Pin Encapsulated Package (740 Mil Extended)

#### **PIN DESCRIPTION**

A0-A16 Address Lines
D0-D7 Data Input/Output
OE Output Enable
CE Chip Enable
WE Write Enable
NC No Connect

inhibit the write enable to the nonvolatile SRAM. This can provide data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery back-up is not needed. The device can be used in place of existing 128K x 8 EPROM, EEPROM, or FLASH conforming to the popular bytewide 32-pin JEDEC standard. There is no limit on the number of write cycles which can be executed and no additional circuitry is required for microprocessor interface.

# **OPERATION**

#### READ MODE

The DS1245EE executes a read cycle whenever  $\overline{\text{CE}}$  (Chip Enable) is active (low) and  $\overline{\text{OE}}$  (Output Enable) is active (low). The unique address specified by the 17 address inputs (A<sub>0</sub> - A<sub>16</sub>) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within (t<sub>ACC</sub>) after the last address input signal is stable, providing that the  $\overline{\text{CE}}$  (Chip Enable) and  $\overline{\text{OE}}$  (Output Enable) access times are also satisfied. If  $\overline{\text{OE}}$  and  $\overline{\text{CE}}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{\text{CE}}$  or  $\overline{\text{OE}}$ ) and the limiting parameter is either to for  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$ , rather than address access.

#### WRITE MODE

The DS1245EE is in the write mode only if it has been enabled by the user in software. If activated, a write will occur whenever the WE (Write Enable) and CE (Chip Enable) signals are in the active state (low). The latter occurring falling edge of CE (Chip Enable) or WE (Write Enable) will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE (Chip Enable) or WE (Write Enable). All address inputs must be kept valid throughout the write cycle. WE (Write Enable) must return to the high state for a minimum recovery time (twp) before another cycle can be initiated. The OE (Output Enable) control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE enabled) then WE (Write Enable) will disable the output buffers in town from its falling edge.

#### WRITE INHIBIT MODE

The DS1245EE provides two software selectable switches for control of the write enable and nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (See Tables 1 and 2). Prior to entering the pattern recognition sequence which will define the two

switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointers. Each four-bit compare nibble is clocked into the DS1245EE in the falling edge of CE (Chip Enable). A0, A1, and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven address cycles: the last five are used to define the switch settings. The 12th address cycle defines the switch which inhibits the write enable to the device. A logic one in this location allows read/write operations. A logic zero in this location turns the device into a read-only memory device. The next four address cycles, 12 through 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010, activates the nonvolatile controller and data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation. At the completion of the sixteenth cycle, if the pattern recognition sequence is correct, the switch setting defined in cycles 11 through 15 are transferred and are active for the next memory cycle. When the DS1245EE is first installed in a system with V<sub>CC</sub> power, the device will not be in write protect mode.

#### **DATA RETENTION MODE**

The nonvolatile static RAM provides full functional capability for  $V_{\rm CC}$  greater than 4.5 volts and unconditionally write protects at 4.37 volts nominal. Data is maintained in the absence of  $V_{\rm CC}$  without any additional support circuitry. Should an out of tolerance condition be detected, the DS1245EE will automatically write protect itself and all inputs to the device become "don't care" and all outputs are high impedance. As  $V_{\rm CC}$  falls below approximately 3.0 volts, the power switching circuit can connect the lithium energy source to the RAM to retain data if enabled. During power-up, when  $V_{\rm CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{\rm CC}$  to the RAM and disconnects the lithium energy. Normal operation can resume after  $V_{\rm CC}$  exceeds 4.5 volts.

#### **ADDRESS INPUT PATTERN Table 1**

STON STR	du-	X	N.M			YCLI	NUN	/BER								
Address Inputs	0	10.	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A3 A	1	0	1	0	0	0	11	1	0	1	0		line	muO-	giola	110
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
AO	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

<sup>\*</sup> See Table 2

# **CONTROL SELECT Table 2**

	WEI	Battery C	ontrol		Operation
11	12	13	14	15	
0	X	Х	Х	Х	Read Only Operation
1	X	X	Х	X	Read/Write Operation
Χ	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

\*Any other combination turns controller off

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to 70°C -40°C to +70°C 260°C for 10 seconds

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5		
Logic 1	V <sub>IH</sub>	2.2		Vcc	V	13
Logic 0	VIL	0		+0.8	V	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

	SIMBUL	MIIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	e I <sub>IL</sub> a	-1.0	3 4 1	+1.0	μА	ul esembbA
I/O Leakage Current CE >V <sub>IH</sub> <v<sub>CC</v<sub>	I <sub>IO</sub>	-1.0	0 0	+1.0	μА	6A CA
Output Current @2.4V	Іон	-1.0	l n l n	1 1 0	mA	T <sub>A</sub>
Output Current @0.4V	loL	2.0			mA	0.6
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	
Standby Current CE = V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>		3.0	5.0	mA	WHOME BER
Operating Current t <sub>CYC</sub> = 200ns	I <sub>CC01</sub>			85	mA	TONTHO
Write Protection Voltage	V <sub>TP</sub>	4.25	4.37	4.5	V	W.

#### DC TEST CONDITIONS

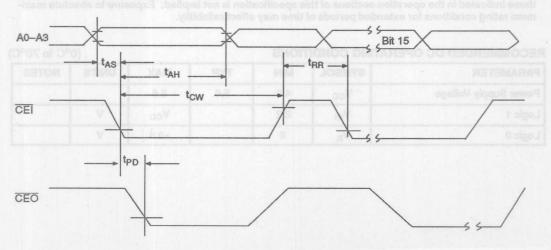
Outputs Open All Voltages Are Referenced to Ground

## **SWITCH TIMING**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CCI}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0			ns	
Address Hold	t <sub>AH</sub>	50	4	EMITASI N	ns	Limose
Read Recovery	t <sub>RR</sub>	40			ns	T prittings
CEI Pulse Width	tcw	110			ns	nell egans

# **TIMING DIAGRAM-SWITCH SETTING**



#### CAPACITANCE

(T<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	
Input/Output Capacitance	C <sub>VO</sub>	I HIV	5	10	pF	

#### AC ELECTRICAL CHARACTERISTICS

(0°C TO 70°C; V<sub>CC</sub> = 5V + 10%)

	- 10 - m	DS124	5EE100	DS124	5EE-120		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	100		120		ns	
Access Time	tACC		100		120	ns	
OE to Output Valid	toE		50	175	60	ns	o eme
CE to Output Valid	tco		100		120	ns	
OE or CE to Output Active	t <sub>COE</sub>	5	K-JK	5	80883800	ns	5
Output High Z From Deselection	t <sub>OD</sub>	77	35	777.	40	ns	5
Output Hold From Address Change	tон	5	777	5		ns	
Write Cycle Time	twc	100	V suV	120	TW .	ns	
Write Pulse Width	t <sub>WP</sub>	75		90		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		ns	
Write Recovery Time	t <sub>WR</sub>	15	( ) ( )	15		ns	
Output High Z From WE	topw		35		35	ns	5
Output Active from WE	toew	5		5	a c ave	ns	5
Data Setup Time	t <sub>DS</sub>	40		50		ns	4
Data Hold Time From WE	t <sub>DH</sub>	15	1	15	erango s	ns	4

#### AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate

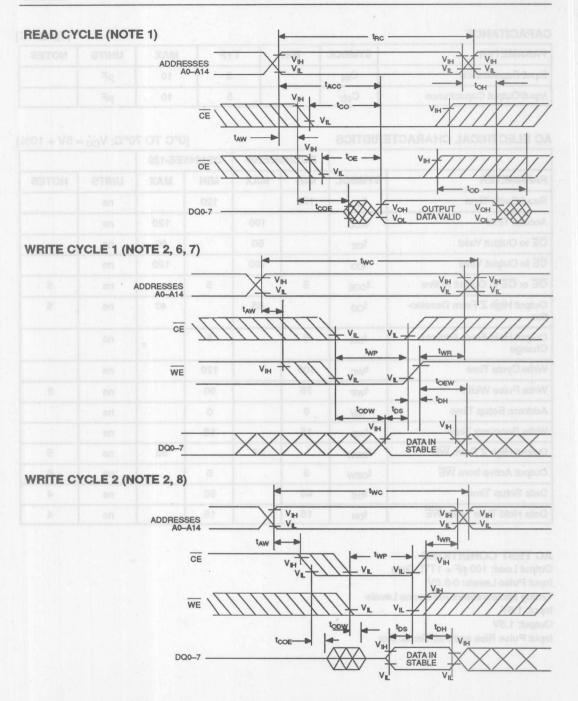
Input Pulse Levels: 0-3.0V

Timing Measurement Reference Levels

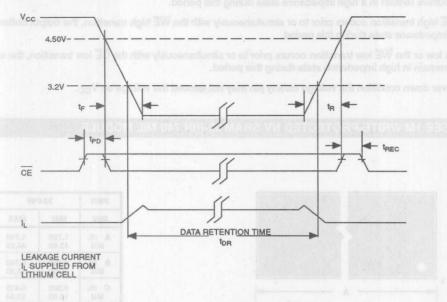
Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

4



### POWER-DOWN/POWER-UP TIMING



4

#### POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0		us	9
t <sub>F</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	100		us	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0	1 0 0 0	us	
t <sub>REC</sub>	CE at V <sub>IH</sub> after Power-Up	누러 당에는	2	ms	1

 $(t_A = 25^{\circ}C)$ 

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	5		years	9

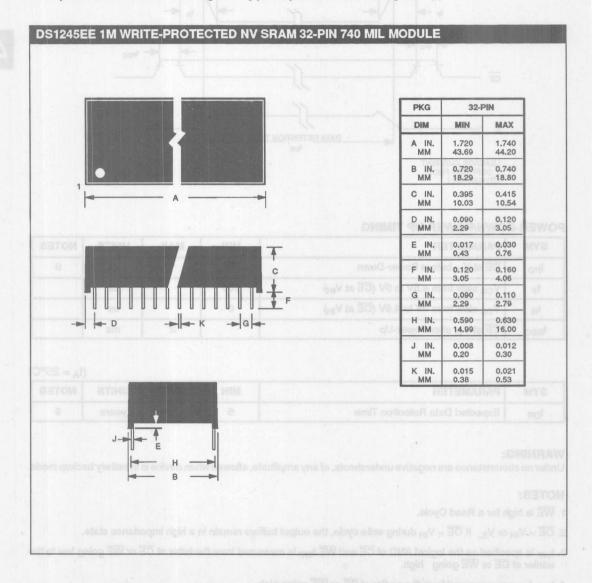
#### **WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES:

- 1. WE is high for a Read Cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ .t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.

- 6. If the CE low transition occurs simultaneously with or latter from the WE low transition in a Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition, the output buffers remain in high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in high impedance state during this period.
- 9. In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.



### DS1380, DS1380S RAMport

#### **FEATURES**

- 2K X 8 Static RAM
- 8-Bit Transparent I/O Port
- Battery connection provided for nonvolatility
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10% of power supply voltage
- Power Fail Interrupt Output
- Low Power CMOS
- 24 Pin Dip Package or optional 24 pin SOIC
- Ideally suited for microcontroller applications as add on memory

#### **PIN ASSIGNMENT**



24 PIN DIP OR 24 PIN SOIC

#### **PIN DESCRIPTION**

VBAT

PF - Power Fail Output
PI1 - PI8 - Port Inputs (μP Ports)

PO1 - PO8 - Port Outputs (External Ports)

GND - Ground

Vcc - +5 Volts

CLK - Clock

MEM - Memory Select

#### DESCRIPTION

The DS1380 is a 2K X 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1380 for use in the identical manner as previously intended. The reproduced port pins can be both inputs and outputs and will appear as exactly the same I/O structure on the attached microcontroller. The content of memory is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1380 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the

DS1380 can be made nonvolatile with direct connection of a 3 volt lithium battery. The DS1380 is controlled by only two signals; the port clock and memory select inputs.

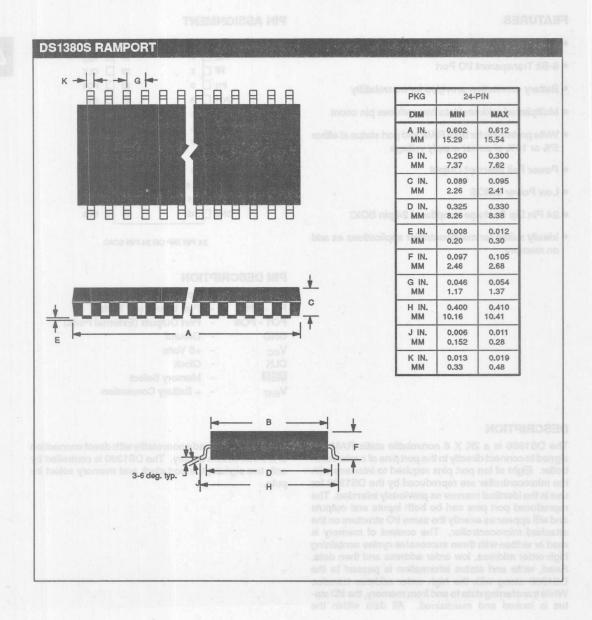
+ Battery Connection

4

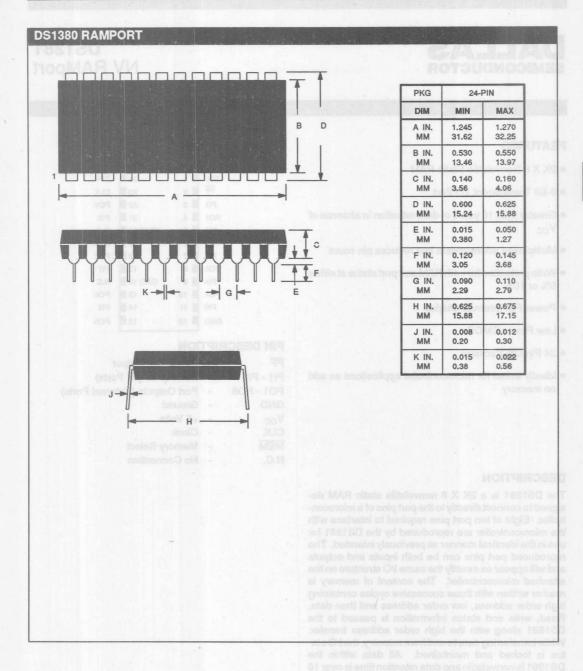
#### **OPERATION**

The DS1380 performs exactly to the specifications of the DS1381 with the exception of an external battery connection. The V<sub>BAT</sub> pin is designed for a battery input voltage between 2.7 volts and 3.5 volts and requires a current of 100 nA at 25°C and 1 uA at 60°C. If battery

backup operation is not required, the  $V_{BAT}$  input must be grounded. With the external battery connected, the DS1380 is nonvolatile and retains data in the absence of power. When the  $V_{BAT}$  input is grounded, the DS1380 is volatile and will not retain data without  $V_{CC}$ . For detailed operation and electrical specifications consult the DS1381 data sheet.









DS1381 NV RAMport

#### **FEATURES**

- 2K X 8 Nonvolatile Static RAM
- 8-Bit Transparent I/O Port
- Greater than 10 years of data retention in absence of Vcc
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10%
- Power Fail Interrupt Output
- Low Power CMOS
- 24 Pin Dip Package
- Ideally suited for microcontroller applications as add on memory

#### DESCRIPTION

The DS1381 is a 2K X 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1381 for use in the identical manner as previously intended. The reproduced port pins can be both inputs and outputs and will appear as exactly the same I/O structure on the attached microcontroller. The content of memory is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1381 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1381 is nonvolatile and data retention time is over 10 years. The DS1381 is controlled by only two signals; the port clock and memory select inputs.

#### **PIN ASSIGNMENT**

TOL	1 1	24	Vcc
PF	2	23	CLK
PI1	3	22	PO8
PO1	4	21	PI8
Pl2	5	VBAT 20	N.C.
PO2	6	19	MEM
PI3	7	18	P07
PO3	8	17	PI7
PI4	9	GND 16	N.C
PO4	10	15	PO6
PI5	11	14 🖩	PI6
GND	12	13	PO5
	Carried San		

#### PIN DESCRIPTION

PF	-	Power Fail Output
PI1 - PI8		Port Inputs (µP Ports)
PO1 - PO8	-	Port Outputs (External Ports)
GND	-	Ground

V<sub>CC</sub> - +5 Volts

CLK - Clock

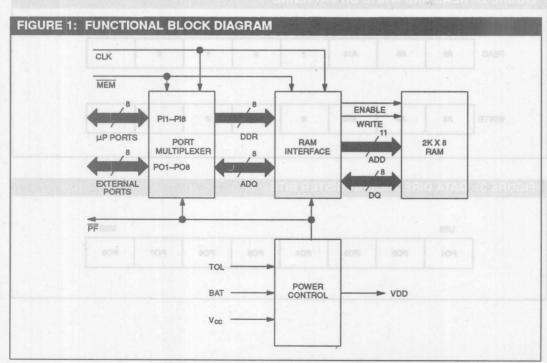
MEM - Memory Select

N.C. - No Connection

A block diagram of the DS1381 nonvolatile RAMport is shown in Figure 1. As shown, the DS1381 has four key elements: namely the port multiplexer, the RAM interface, a 2K X 8 static RAM, and a power control section. The port multiplexer is connected to eight microcontroller port pins from which address, data and port data are received. The 8 microcontroller port pins are reproduced at the multiplexer output when the MEM pin is high through transmission gates. When the MEM pin is low all output pins are latched in their high or low states and inputs go to a high impedance state. With the MEM pin low the microcontroller port pins are then free to pass address and data to and from the nonvolatile static RAM. Each read or write cycle to memory is accomplished in three separate steps involving two address transfers and one data transfer. The clock signal (CLK) is used to strobe address and data information through the port multiplexer into the RAM interface circuitry. To accomplish RAM access the high order address (A8-A10) is placed on port input pins PI1 through PI3. Pl4 through Pl8 contain bits which dictate a read of RAM or a write to RAM. If these bits do not match exactly the bit patterns as shown in Figure 2, completion of the full cycle will be allowed but no action will be taken during the data transfer portion. With the proper bit patterns placed on the port pins, the CLK input is then transitioned high to low and then high again. The clock action

allows the address and read/write information to propagate through the port multiplexer and latch the information into the RAM interface. Next the low order address (A0-A7) is placed on the port input pins (Pl1 through PI8) and the second address transfer also propagates through the port multiplexer as CLK goes low and returns high. The RAM is now ready for data transfer. If a write cycle is to occur, the microcontroller port pins must deliver the correct data to be written. As the CLK transitions high to low, data propagates through the port multiplexer and the RAM interface and finally to the RAM where data is written into RAM. The write cycle is terminated when the CLK transitions low to high. Data can then be removed from the port input pins. If during the data transfer a read cycle is to occur, the port input pins must not be driven by the microcontroller. Then as CLK transitions high to low, the RAM becomes active and data is presented on the port input pins for the microcontroller to read. A read cycle is terminated when the CLK signal is transitioned low to high and the port input pins are returned to a high impedance state.

After completing the read or write cycle another read or write cycle can be performed without pulsing the MEM pin high between cycles. After all access to the RAM is complete, the MEM pin must be returned to a high state.

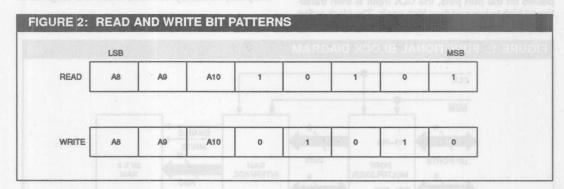


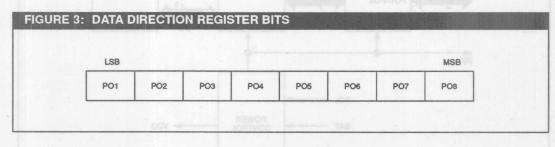
# OPERATION - WRITING THE DATA DIRECTION REGISTER

The data direction register is written with a logic one in each bit location which will have a corresponding high impedance output pin (PO1-PO8) during reading and writing of the memory of the DS1381 by the microcontroller (see Figure 3). This will avoid contention between PO1-PO8 and devices driving PO1-PO8 as inputs. To write data to the data direction register, the CLK input is driven low prior to MEM going low. With CLK low MEM is driven low which latches the port output pins and readies the DS1381 for data direction information. Data direction information is then placed on the port input pins by the microcontroller and is written into the data direction register as MEM transitions low to high. While the data direction register is being written, the output pins (PO1 through PO8) are latched to the PI1 through PI8 states with their high or low impedance condition determined by the old data direction contents. The new data direction contents will be effective the next time MEM is taken to a low state.

# OPERATION - POWER FAIL AND DATA RETENTION MODE

The DS1381 has full functional capability when Vcc is within normal limits. However, when Vcc goes to an out of tolerance level, the nonvolatile RAMport assumes a write protected status such that the memory and data direction register cannot be accessed. In addition the port output signals go to a high impedance state, the port input pins become "don't care" and the transmission gates connecting the 8 microprocessor port pins to the external ports will go to a low impedance state. The power fail pin (PF) goes to an active low level when power fail occurs and remains low until Vcc returns to nominal limits. The point at which write protection occurs depends on the level of the tolerance pin (TOL). When TOL is grounded, write protection will occur between 4.75 volts and 4.5 volts. When TOL is connected to Vcc, write protection occurs between 4.5 volts and 4.25 volts. After power fail detection has occurred and the Vcc level falls below the voltage level of the internal lithium cell the internal memory and register contents are maintained by this cell which is capable of maintaining data for over 10 years. The switch over from Vcc to the lithium cell occurs when V<sub>cc</sub> is below approximately 3 volts.





#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.5V TO 7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Supply Voltage (TOL=GND)	Vcc	4.75	5.0	5.5	Volts	Up of Mil		
Supply Voltage (TOL=V <sub>CC</sub> )	Vcc	4.5	5.0	5.5	Volts	ouo al 83		
Logic 1 Input	VIH	2.0	01	V <sub>CC</sub> + 0.3	Volts	TENZ 10 X.		
Logic 0 Input	V <sub>IL</sub>	-0.3		+0.8	Volts	ated drot		

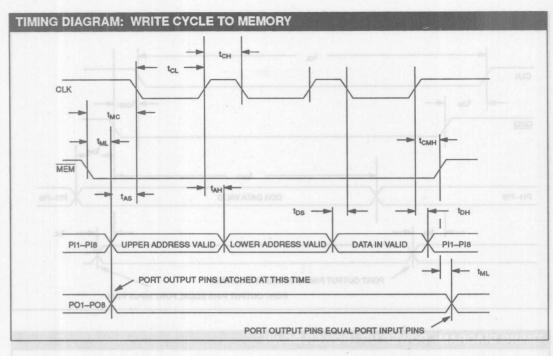
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current	ICC1		20	25	mA	2
Standby Current	ICC2		3	7	mA	3
Logic 1 Out @ 1 mA	V <sub>OH</sub>	2.4			Volts	1,6
Logic 0 Out @ 2 mA	V <sub>OL</sub>	TRAI		0.4	Volts	1,6
VCC Write Protect TOL=GND	V <sub>CCTP</sub>	4.50	4.62	4.75	Volts	1
VCC Write Protect TOL=VCC	V <sub>CCTP</sub>	4.25	4.37	4.50	Volts	1
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μА	4
Output Leakage	ILO	-1.0		+1.0	μА	5
Port Pins In to Out Impedance	Pz		75	150	Ω	7

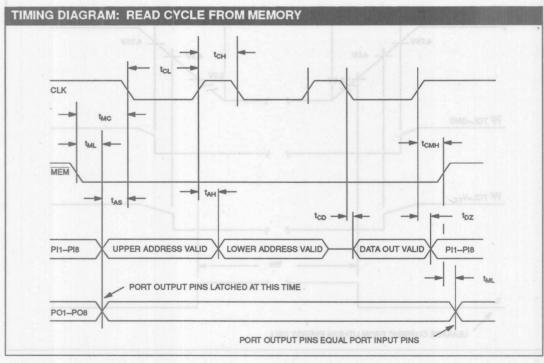
CAPACITANCE						
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	t <sub>A</sub> =25°C		10	pF	
Output Capacitance	C <sub>OUT</sub>	t <sub>A</sub> =25°C		10	pF	

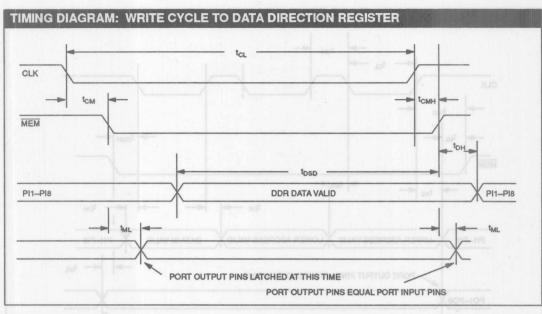
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Low	ed Morton	150		38	ns	LDERING
Clock High	t <sub>CH</sub>	50	anitasano	tendition thes	ns	arte a el el
Address Setup	t <sub>AS</sub>	20	Specificati	sections of this	no ns e	i ni batso
Address Hold	t <sub>AH</sub>	0	· ·	Man is circuit	ns	
Data Setup	t <sub>DS</sub>	20	1111111100	MATA REPRE	ns	MARONE
Data Hold	t <sub>DH</sub>	0	NEM JE	SYMBC	ns	BTBMARA
MEM to CLK Low	t <sub>MC</sub>	40	4.78	ooV (C	ns	shoV ylqqu
MEM to Output Latch	t <sub>ML</sub>	25	4.5	Ved (	ns	siloV yiqqi
CLK to MEM High	t <sub>CMH</sub>	10	0.8	HV	ns	lugal 7 sign
CLK to Data Valid	t <sub>CD</sub>		6,0-	100	ns	Jugal 0 olg
CLK to Data at High Z	t <sub>DZ</sub>			20	ns	
CLK to MEM Active	t <sub>CM</sub>	40			ns	ROTO
DDR Data Setup	t <sub>DSD</sub>	100	TOTAL ST	NATURE OF THE PARTY OF THE PART	ns	PTRIAGA
V <sub>CC</sub> Slew Rate	t <sub>R</sub> , t <sub>F</sub>	250		1001	μѕ	Lauren sade

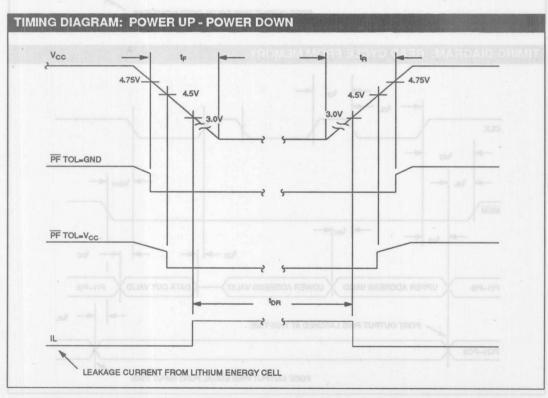
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention	10	11 614	years	







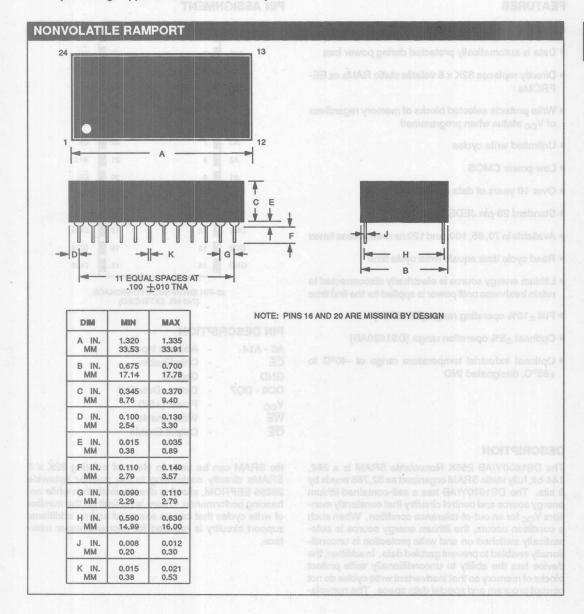




#### NOTES

- 1. All voltages are reference to ground
- Active current is defined as MEM low with CLK low and all outputs are open
- Standby current is defined as MEM high with CLK high and all outputs are open
- 4. Input leakage applies to CLK and MEM only

- 5. Output leakage applies to PF only
- Logic levels apply to PF and PO1-PO8 when these outputs are latched
- Port input to output impedance is the on resistance of the transmission gate between port inputs and port outputs with MEM high and with less than 4 mA flowing through the transmission gate.





### DS1630Y/AB Partitioned 256K NV SRAM

#### **FEATURES**

### Data retention in the absence of V<sub>CC</sub>

- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAMs or EE-PROMs
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, and 120 ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range (DS1630Y)
- Optional ±5% operation range (DS1630AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

# PIN ASSIGNMENT

A14	T <sub>1</sub> TEC	28	Vcc
A12	2	27	WE
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
АЗ	7	22	ŌE
A2	8	21	A10
A1	9	20	CE
AO	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
GND	14	15	DQ3
	Secretary and the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the second section of the second section is a second section of the sect	CONTRACTOR OF THE PERSON NAMED IN COLUMN 2 IS NOT THE PERSON NAMED	The second second

28-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

#### PIN DESCRIPTION

A0 - A14	-	Address Inputs
CE	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
Vcc	-	Power (+5V)
WE	-	Write Enable
ŌĒ	-	Output Enable

#### DESCRIPTION

The DS1630Y/AB 256K Nonvolatile SRAM is a 262, 144-bit, fully static SRAM organized as 32,768 words by 8 bits. The DS1630Y/AB has a self-contained lithium energy source and control circuitry that constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvola-

tile SRAM can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewide 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

#### **READ MODE**

The DS1630Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A<sub>0</sub> - A<sub>14</sub>) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t<sub>ACC</sub> (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access

#### WRITE MODE

The DS1630Y/AB is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in toDW from its falling edge.

#### **DATA RETENTION MODE**

The nonvolatile static RAM provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.37V nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1630AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1630Y/AB constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power

switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts (4.75 volts for the DS1630AB).

#### FRESHNESS SEAL AND SHIPPING

The DS1630Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

#### PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11 - A14. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1630Y/AB to inhibit WE internally when A14 A13 A12 A11=0101. Note that while setting the partition register. data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

TABI			No.	N-	TIL	1110	10		1	-			1110		Lai				MES					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	2
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1=	1	0	pi1u	X	X	X	>
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	>
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	)
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	)

FIRST BITS ENTERED

LAST GROUP ENTERED

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>14</sub> A <sub>13</sub> A <sub>12</sub> A <sub>11</sub> )
A11	BIT 21	PARTITION 0	0000 mg 1/1 mg
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	ov 0.5 yleder 1000 ge woled
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.5V TO 7.0V 0°C TO 70°C, -40°C TO +85°C FOR IND PARTS -40°C TO 70°C, -40°C TO +85°C FOR IND PARTS 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERA	TING COND	ITIONS (0	°C TO 70°	°C)						
PARAMETER ***	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
DS1630Y Power Supply Voltage	Vcc	4.5	5.0	5.5	V	igil-f arqtu				
DS1630AB Power Supply Voltage	Vcc	4.75	5.0	5.25	V	NOFT TURBLE				
Logic 1	V <sub>IH</sub>	2.2	bwc	V <sub>CC</sub>	V <sub>ern</sub>	nta Cycle				
Logic 0	VIL	0.0	fige	+0.8	Vubité	rita Pulse				

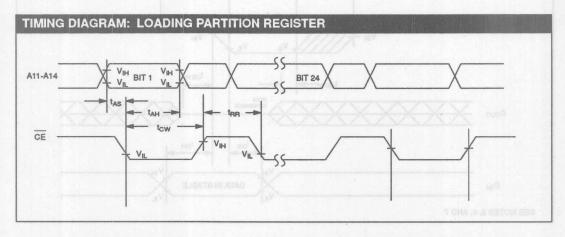
DC ELECTRICAL CHARACTE	ELECTRICAL CHARACTERISTICS			(0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10 (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5%						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Input Leakage Current	BB IIL	-1.0	eq!	+1.0	μА	Jeta Setup				
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	100 - 051	-1.0	) HGP	+1.0	μА	Pata Hold 1				
Output Current @ 2.4V	loн	-1.0	TOBMAS		mA	TEMARAS				
Output Current @ 0.4V	I loL	2.0	Sec		mA	Read Cycle				
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	emili eaecol				
Standby Current $\overline{\text{CE}} = V_{\text{CC}} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	uqiuO, et 30				
Operating Current	I <sub>CCO1</sub>		608	85	mA	CHILD OF THE				
Write Protection Voltage (DS1630Y)	V <sub>TP</sub>	4.25	4.37	4.5	v .	igiH mond				
Write Protection Voltage (DS1630AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	agnard Shange				

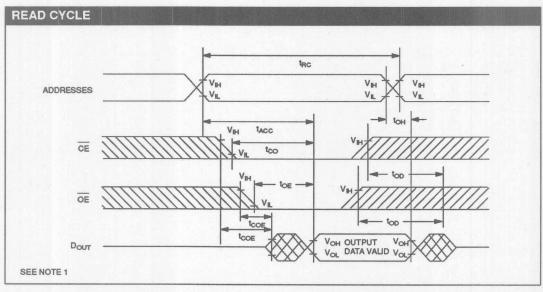
CAPACITANCE (t <sub>A</sub> = 25°C	)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	feit fugt
Input/Output Capacitance	C <sub>VO</sub>	a	5	10	pF	ritia A sugh

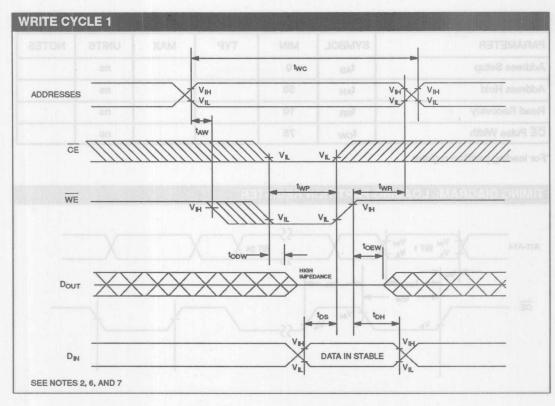
AC ELECTRICAL CHARACT	ERISTICS	(0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1630AB) (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS1630Y)								
TO 485 O FOR IND PARTS	70°C, -40°C	DS1630	Y/AB-70	DS1630	Y/AB-85	ARBAMET	BOARD			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES			
Read Cycle Time	t <sub>RC</sub>	70	noltmend	85	bris vico	ns	te a si eld			
Access Time	tACC	Jon al ne	70	BIRT TO 20	85	ns	Hogies I			
OE to Output Valid	toE		35		45	ns				
CE to Output Valid	tco	) (0) EM	70	DHITA	85	ns	Flere			
OE or CE to Output Valid	tcoe	5	101	5		ns	5			
Output High Z from Deselection	top	T a	25	W I	30	ns	5			
Output Hold from Address Change	t <sub>OH</sub>	5		5	istloV yiqq	ns	STEBOAR			
Write Cycle Time	twc	70		85		ns	ogia 1			
Write Pulse Width	t <sub>WP</sub>	55		65		ns	3			
Address Setup Time	t <sub>AW</sub>	0		0		ns				
Write Recovery Time	twR	15	25	15	MARAHE	ns	Busio			
Output High Z from WE	topw		25		30	ns	5			
Output Active from WE	toew	5	101	5		ns	5			
Data Setup Time	t <sub>DS</sub>	30		35		ns	4			
Data Hold Time	t <sub>DH</sub>	15		15		ns	4			
		DS1630	Y/AB-100	DS1630	Y/AB-120	Veo.	SWAS			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES			
Read Cycle Time	t <sub>RC</sub>	100		120	V	ns	utput Cu			
Access Time	tACC		100	pol	120	ns	tandby G			
OE to Output Valid	toE		50	ool I v	60	ns	D volonat			
CE to Output Valid	tco		100		120	ns	noltman			
OE or CE to Output Valid	t <sub>COE</sub>	5		5	- Interpretation of	ns	5			
Output High Z from Deselection	top		35		35	ns	5			
Output Hold from Address Change	фОН	5		5	eg	ns	Inte Prote			
Write Cycle Time	twc	100		120		ns				
Write Pulse Width	t <sub>WP</sub>	75		90		ns	3			
Address Setup Time	t <sub>AW</sub>	0	17.55	0		ns				
Write Recovery Time	t <sub>WR</sub>	15	130	15		ns	JEN PERSON			
Output High Z from WE	topw		35	9	35	ns	5			
Output Active from WE	toew	5		5	eon	ns	5			
Data Setup Time	t <sub>DS</sub>	40		50		ns	4			
Data Hold Time	t <sub>DH</sub>	15		15		ns	4			

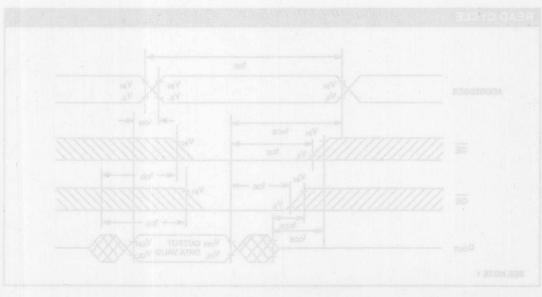
AC ELECTRICAL CHA	CAL CHARACTERISTICS (0°C TO 70°C, V <sub>CCI</sub> = 4.50V TO 5.50V)*					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0			ns	
Address Hold	t <sub>AH</sub>	50	es.V	X	ns	E E E E E E E E E E E
Read Recovery	t <sub>RR</sub>	10	Land		ns	
CE Pulse Width	tcw	75	150		ns	

<sup>\*</sup>For loading partition register

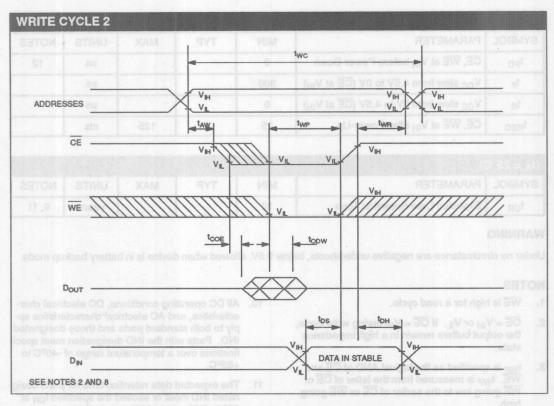


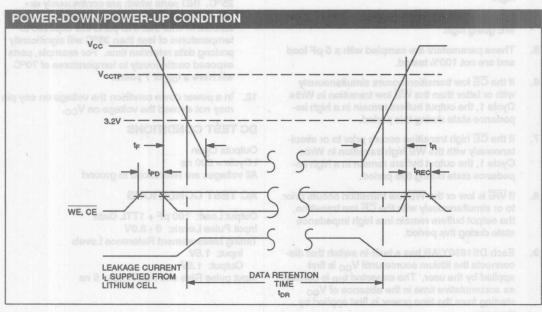












POWER-	DOWN/POWER-UP TIMING					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>PD</sub>	CE, WE at VIH before Power-Down	0			μs	12
t <sub>F</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300			μs	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0			μs	ADDRES
tREC	CE, WE at VIH after Power-Up	25	All the second	125	ms	

(t <sub>A</sub> = 25°C)								
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES		
t <sub>DR</sub>	Expected Data Retention Time	10	35/1999	9999	years	9, 11		

#### WARNING

Under no circumstance are negative undershoots, below 0.5V, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a read cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
- 4.  $\underline{t_{DH}}$ ,  $t_{DS}$  are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in Write
  Cycle 1, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1630Y/AB has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is first applied by the user.

- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- 11. The expected data retention time for parts designated IND meet or exceed the specified t<sub>DR</sub> at 25°C. IND parts which are continuously exposed to 85°C will have a t<sub>DR</sub> of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t<sub>DR</sub> of 7 years.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

#### DC TEST CONDITIONS

Outputs Open t Cycle = 200 ns All voltages are referenced to ground

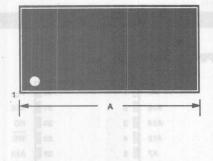
#### **AC TEST CONDITIONS**

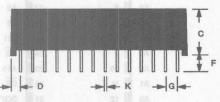
Output Load: 100 pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V Timing Measurement Reference Levels Input: 1.5V

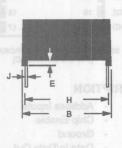
Output: 1.5V

Input pulse Rise and Fall Times: 5 ns

#### DS1630Y/AB NONVOLATILE SRAM 28 PIN 740 MIL MODULE







PKG	28-F	PIN	
DIM	MIN	MAX	
A IN.	1.520	1.540	
MM	38.61	39.12	
B IN.	0.720	0.740	
MM	18.29	18.80	
C IN.	0.395	0.415	
MM	10.03	10.54	
D IN.	0.100	0.130	
MM	2.54	3.30	
E IN. MM	0.017 0.43	0.030 0.76 0.160 4.06	
F IN. MM	0.120 3.05		
G IN.	0.090	0.110	
MM	2.29	2.79	
H IN.	0.590 14.99	0.630 16.00	
J IN.	0.008	0.012	
MM	0.20	0.30	
K IN.	0.015 0.38	0.021	

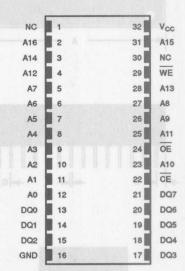


# DS1645Y/AB Partitioned 1024K NV SRAM

#### **FEATURES**

- Data retention in the absence of Vcc.
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM or EE-PROM
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, 100 or 120 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1645Y)
- Optional ±5% operating range (DS1645AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



32-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

#### PIN DESCRIPTION

 A0 - A16
 - Address Inputs

 CE
 - Chip Enable

 GND
 - Ground

 DQ0 - DQ7
 - Data In/Data Out

 V<sub>CC</sub>
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

#### DESCRIPTION

The DS1645Y/AB 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1645Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to un-

conditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

- No Connect

NC

#### **OPERATION - READ MODE**

The DS1645Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A $_0$  - A $_{16}$ ) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $\overline{OE}$  for  $\overline{OE}$  rather than address access.

#### **OPERATION - WRITE MODE**

The DS1645Y is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topw from its falling edge.

#### **DATA RETENTION MODE**

The nonvolatile static RAM provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.37 volts nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1645AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1645Y constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can re-

sume after V<sub>CC</sub> exceeds 4.5 volts (4.75 volts for the DS1645AB).

#### FRESHNESS SEAL AND SHIPPING

The DS1645Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

#### **BATTERY REDUNDANCY**

Battery redundancy is provided to ensure reliability. The DS1645Y contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

#### PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A13 - A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 128K/16 or 8K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1645Y/AB to inhibit WE internally when A16 A15 A14 A13=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

ABLE 2:	PARTITION REG	ISTER MAPPING	
Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>16</sub> A <sub>15</sub> A <sub>14</sub> A <sub>13</sub> )
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	5 bas MAR 1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.5V TO +7.0V 0°C TO 70°C, -40°C TO +85°C FOR IND PARTS -40°C TO +70°C, -40°C TO +85°C FOR IND PARTS 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERA	TING COND	ITIONS (0	°C TO 70°	C)		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1645Y Power Supply Voltage	Vcc	4.5	5.0	5.5	V	lold turning
DS1645AB Power Supply Voltage	Vcc	4.75	5.0	5.25	V	hange
Logic 1	VIH	2.2	J. SWA	Vcc	V	abyO ethi
Logic 0	VIL	0.0	- SWI	+0.8	V	AND THE PARTY OF T

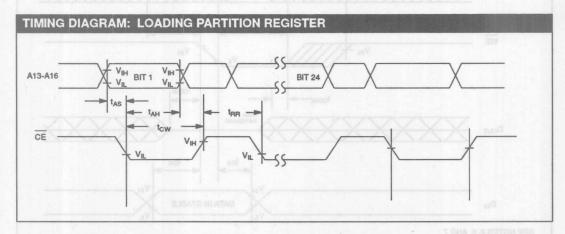
DC ELECTRICAL CHARACTE	(0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1645 (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS164					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0	Luci	+1.0	μА	blold eta0
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	l <sub>IO</sub>	-1.0	Ton Ave	+1.0	μА	TO A A CLASS
Output Current @ 2.4V	Іон	-1.0			mA	dayen haref
Output Current @ 0.4V	loL	2.0	nou)		mA	Access Yie
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	nguO of IC
Standby Current $\overline{\text{CE}} = V_{\text{CC}} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	igkuO of EC
Operating Current	I <sub>CCO1</sub>	8	300	85	mA	/ 30 to 30
Write Protection Voltage (DS1645Y)	V <sub>TP</sub>	4.25	4.37	4.5	V	i giri xiqibç NoH iuqibÇ
Write Protection Voltage (DS1645AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	Vinte Cycle

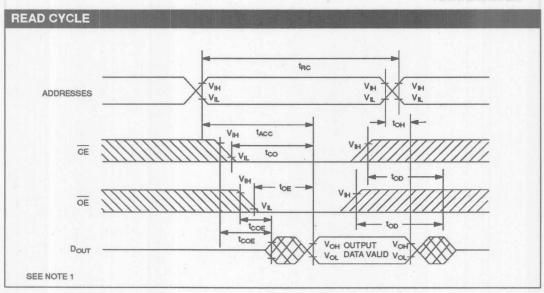
CAPACITANCE (t <sub>A</sub> = 25°C	)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	2	5	10	pF	Mrs.A. Screens
Input/Output Capacitance	C <sub>VO</sub>	0.0	5	10	pF	ata Satus

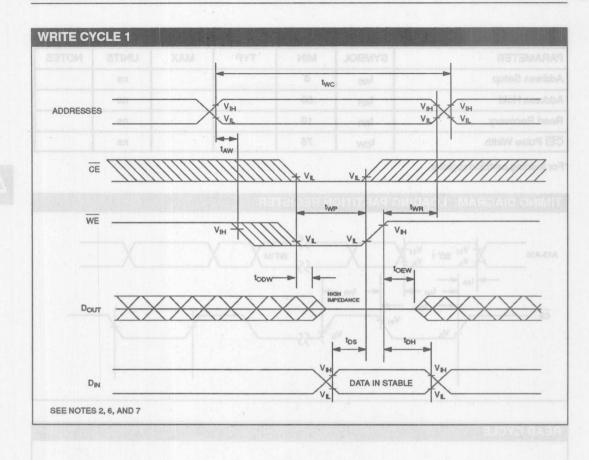
AC ELECTRICAL CHARACT	ERISTICS		°C TO 70°				
TO 183°C FOR IND PARTS	70°C, -40°C		SY/AB-70		Y/AB-85	G TENN'E TEMPERA	PEROUNA TORAGE
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	70	operation	85	only and	ns	te a ai aid'
Access Time	tACC	ion al noi	70	eidt to and	85	ns	dicated
OE to Output Valid	toE	Anniemina	35	O CERCIO INC.	45	ns	ationimi
CE to Output Valid	tco	10.15	70	is divas	85	ns	Violett
OE or CE to Output Valid	tcoe	5	100	5		ns	5
Output High Z from Deselection	top		25		30	ns	5
Output Hold from Address Change	tон	5	1	5	gasov vog pply Volta	ns	Assaras
Write Cycle Time	twc	70		85		ns	1 sipo.
Write Pulse Width	t <sub>WP</sub>	55		65		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		ns	
Write Recovery Time	twR	15	mesta respect	15		ns	
Output High Z from WE	topw		25		30	ns	5
Output Active from WE	toew	5	ES -yallia	5	Mark Library	ns	5
Data Setup Time	t <sub>DS</sub>	30	-	35		ns	4
Data Hold Time from WE	t <sub>DH</sub>	15		15	- 11	ns	4
Aq   0.14		DS1645	Y/AB-100	DS1645	Y/AB-120	e Cumant	O Leakap
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	100		120		ns	
Access Time	tACC	1 V-	100	2	120	ns	- Aurilian
OE to Output Valid	toE		50	101	60	ns	Account.
CE to Output Valid	tco		100	pol V	120	ns	tandby D
OE or CE to Output Valid	tcoe	5	10	5		ns	5
Output High Z from Deselection	top	ac	35	N	35	ns	5
Output Hold from Address Change	tон	5		5		ns	DS1645
Write Cycle Time	twc	100		120		ns (8	0816454
Write Pulse Width	t <sub>WP</sub>	75	1	90		ns	3
Address Setup Time	t <sub>AW</sub>	0	THE WAY	0	25 C	ns	OARA
Write Recovery Time	twR	15	Tion	15		ns	TELLA SER
Output High Z from WE	topw		35		35	ns	5
Output Active from WE	toew	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	40	0	50	eon	ns	4
Data Hold Time from WE	t <sub>DH</sub>	15		15		ns	4

AC ELECTRICAL CHARACT	TERISTICS (0	°C TO 70°	C, V <sub>CCI</sub> = 4.	50V TO 5.	50V)*	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0			ns	
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	10			ns	
CEI Pulse Width	t <sub>CW</sub>	75	-d-00		ns	

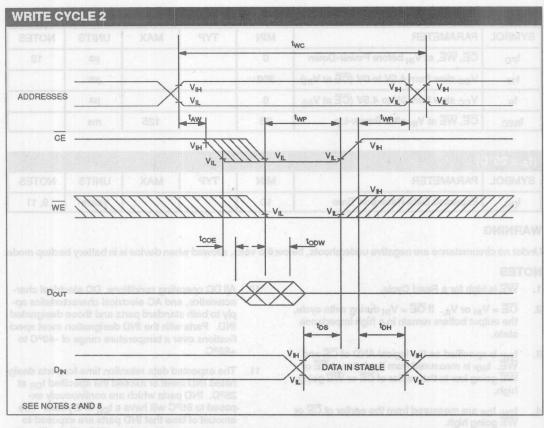
<sup>\*</sup>For loading partition register

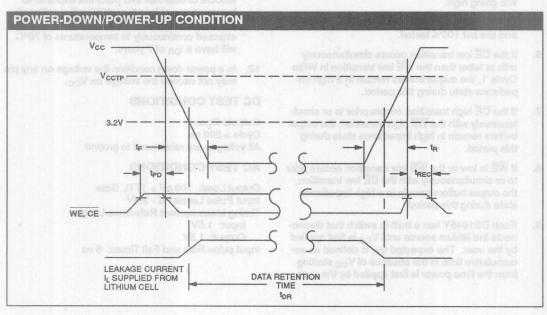












POWER-	DOWN/POWER-UP TIMING					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>PD</sub>	CE, WE, at VIH before Power-Down	0			μs	12
t <sub>TF</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300	V		μs	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH)</sub>	0	.V.		μs	ADDRESSE
tREC	CE, WE at VIH after Power-Up	25	- And	125	ms	

$(t_A = 25^{\circ})$	<b>(2)</b>					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10	(20/11)	7/1//	years	9, 11

#### WARNING

Under no circumstance are negative undershoots, below 0.5 volts, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a Read Cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high
- t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of <del>CE</del> or <del>WE</del> going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1645Y has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is first applied by the user.

- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- 11. The expected data retention time for parts designated IND meet or exceed the specified t<sub>DR</sub> at 25°C. IND parts which are continuously exposed to 85°C will have a t<sub>DR</sub> of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t<sub>DR</sub> of 7 years.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

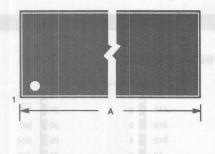
#### DC TEST CONDITIONS

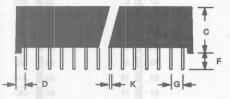
Outputs Open Cycle = 200 ns All voltages are referenced to ground

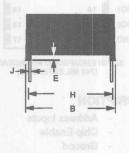
#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V Timing Measurement Reference Levels Input: 1.5V Output: 1.5V Input pulse Rise and Fall Times: 5 ns

### DS1645Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE







PKG	32-F	PIN	
DIM	MIN	MAX	
A IN. MM	1.720 43.69	1.740 44.20	
B IN. MM	0.720 18.29	0.740 18.80	
C IN.	0.395 10.03	0.415 10.54	
D IN. MM	0.090 2.29	0.120 3.05	
E IN. MM	0.017 0.43	0.030 0.76	
F IN. MM	0.120 3.05	0.160 4.06 0.110 2.79	
G IN.	0.090 2.29		
H IN. MM	0.590 14.99	0.630 16.00	
J IN. MM	0.008 0.20	0.012	
K IN.	0.015 0.38	0.021 0.53	

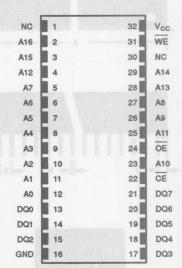


### DS1645EE Partitioned 1024K NV SRAM

#### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 128K x 8 EPROM, EEPROM, or FLASH
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, or 100 ns read access times
- · Read cycle time equals write cycle time
- Full ±10% operating range
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

#### **PIN ASSIGNMENT**



32-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

#### **PIN DESCRIPTION**

 A0 - A16
 - Address Inputs

 CE
 - Chip Enable

 GND
 - Ground

 DQ0 - DQ7
 - Data In/Data Out

 VCC
 - Power (+5V)

WE - Write Enable
OE - Output Enable
NC - No Connect

#### DESCRIPTION

The DS1645EE 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1645EE has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadver-

tent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 EPROM, EEPROM or FLASH conforming to the popular bytewide 32 pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface. This part is functionally equivalent to the DS1645Y and differs only in pinout. See the DS1645Y/AB 1024K NV SRAM data sheet for technical details.

# 4

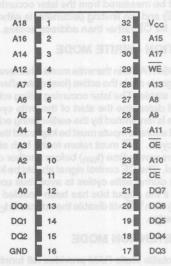
# **DALLAS**SEMICONDUCTOR

### DS1650Y/AB Partitioned 4096K NV SRAM

### **FEATURES**

- Data retention in the absence of V<sub>CC</sub>
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM or EE-PROM
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1650Y)
- Optional ±5% operating range (DS1650AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

### **PIN ASSIGNMENT**



32-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

### PIN DESCRIPTION

 A0 - A18
 - Address Inputs

 CE
 - Chip Enable

 GND
 - Ground

 DQ0 - DQ7
 - Data In/Data Out

 V<sub>CC</sub>
 - Power (+5V)

 WE
 - Write Enable

 OE
 - Output Enable

 NC
 - No Connect

### DESCRIPTION

The DS1650Y/AB 4096K Nonvolatile SRAM is a 4,194,304 bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. The DS1650Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to un-

conditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 512K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

### **OPERATION - READ MODE**

The DS1650Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 19 address inputs ( $A_0$  -  $A_{18}$ ) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

### **OPERATION - WRITE MODE**

The DS1650Y/AB is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in toDW from its falling edge.

### **DATA RETENTION MODE**

The nonvolatile static RAM provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.37 volts nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1650AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1650Y/AB constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can

resume after  $V_{CC}$  exceeds 4.5 volts (4.75 volts for the DS1650AB).

### FRESHNESS SEAL AND SHIPPING

The DS1650Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

### **BATTERY REDUNDANCY**

Battery redundancy is provided to ensure reliability. The DS1650Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

### **PARTITION PROGRAMMING MODE**

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1650Y/AB to inhibit WE internally when A18 A17 A16 A15=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

4

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	Х	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	110	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>18</sub> A <sub>17</sub> A <sub>16</sub> A <sub>15</sub> )
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	Va.o - 0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111 day no
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101 80/18
A17	BIT 24	PARTITION 14	1110 fongs
A18	BIT 24	PARTITION 15	1111

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.5V TO +7.0V 0°C TO 70°C, -40°C TO +85°C FOR IND PARTS -40°C TO +70°C, -40°C TO +85°C FOR IND PARTS 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
DS1650Y Power Supply Voltage	Vcc	4.5	5.0	5.5	V			
DS1650AB Power Supply Voltage	Vcc	4.75	5.0	5.25	V			
Logic 1	V <sub>IH</sub>	2.2		Vcc	V			
Logic 0	VIL	0.0		+0.8	V			

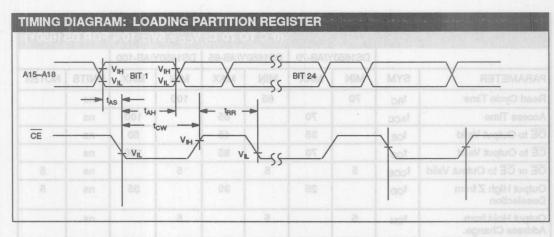
DC ELECTRICAL CHARACTE	ERISTICS	(0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1650AB (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS1650Y						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Input Leakage Current	IIL	-1.0		+1.0	μА			
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	110	-1.0		+1.0	μА			
Output Current @ 2.4V	ІОН	-1.0		ts Tie	mA			
Output Current @ 0.4V	loL	2.0		IS TIE	mA			
Standby Current CE = 2.2V	I <sub>CCS1</sub>	ARTITION -	5.0	10.0	mA			
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I <sub>CCS2</sub>	HOITITRA	3.0	5.0	mA			
Operating Current	I <sub>CCO1</sub>	MATTITION		85	mA			
Write Protection Voltage (DS1650Y)	V <sub>TP</sub>	4.25	4.37	4.5	VIA			
Write Protection Voltage (DS1650AB)	V <sub>TP</sub>	4.50	4.62	4.75	VIA			

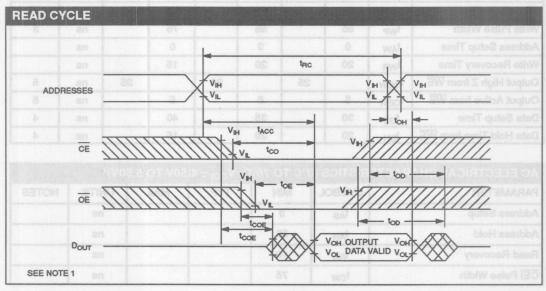
CAPACITANCE (t <sub>A</sub> = 25°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Input Capacitance	CIN	NOTTEN	5	10	pFIA			
Input/Output Capacitance	C <sub>I/O</sub>	HOITITHA	5	10	pFIA			

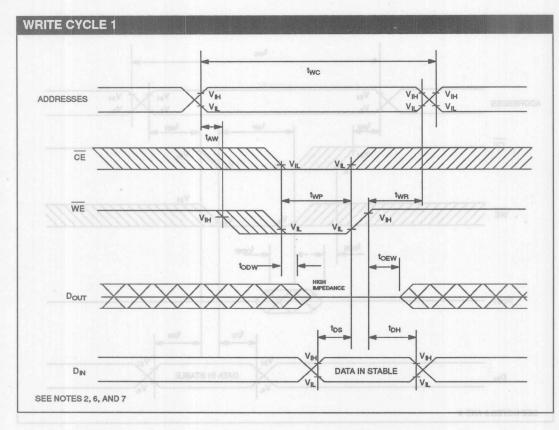
AC ELECTRICAL CHA	AC ELECTRICAL CHARACTERISTICS						(0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 5% FOR DS1650AB) (0°C TO 70°C; $V_{CC}$ = 5V $\pm$ 10% FOR DS1650Y)						
		DS1650	Y/AB-70	DS1650	Y/AB-85	DS1650	Y/AB-100	N/					
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES				
Read Cycle Time	tRC	70		85		100		ns					
Access Time	tACC		70	1	85		100	ns					
OE to Output Valid	toE		35		45	E and	50	ns	- 50				
CE to Output Valid	tco		70	100 ×	85	1	100	ns					
OE or CE to Output Valid	tcoe	5		5		5		ns	5				
Output High Z from Deselection	top		25		30		35	ns	5				
Output Hold from Address Change	tон	5		5		5		ns					
Write Cycle Time	twc	70		85		100		ns	ever le				
Write Pulse Width	t <sub>WP</sub>	55		65	The state of the s	75		ns	3				
Address Setup Time	t <sub>AW</sub>	0		0		0		ns					
Write Recovery Time	twR	20	. onl	20		15	40	ns					
Output High Z from WE	topw		25		20	1	35	ns	5				
Output Active from WE	toew	5		5	37	5		ns	5				
Data Setup Time	t <sub>DS</sub>	30	-	35		40		ns	4				
Data Hold Time from WE	tDH	20		20	1000	15	17777	ns	- 4				

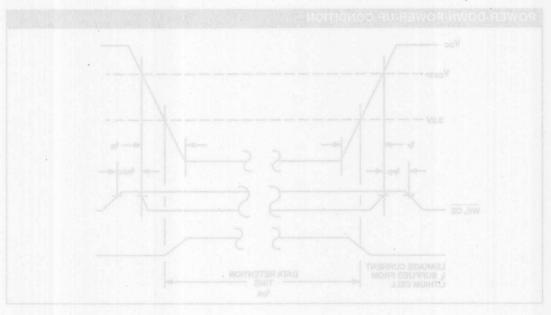
AC ELECTRICAL CHA	RACTERISTICS (0	°C TO 70°	°C, V <sub>CCI</sub> = 4	.50V TO 5.	50V)*	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0	6- T	CLLCCC.	ns	
Address Hold	t <sub>AH</sub>	50	pol Pol		ns	
Read Recovery	t <sub>RR</sub>	10			ns	
CEI Pulse Width	tcw	75			ns	STOW SEA

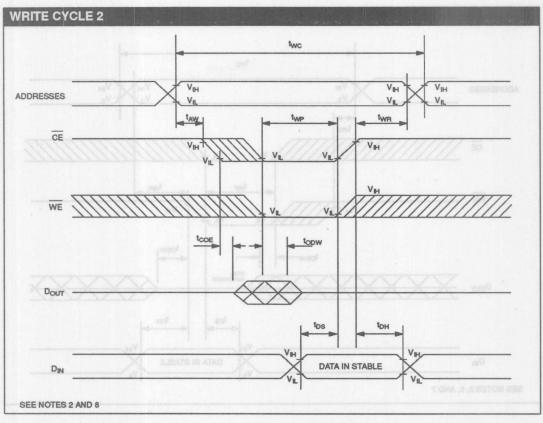
<sup>\*</sup>For loading partition register

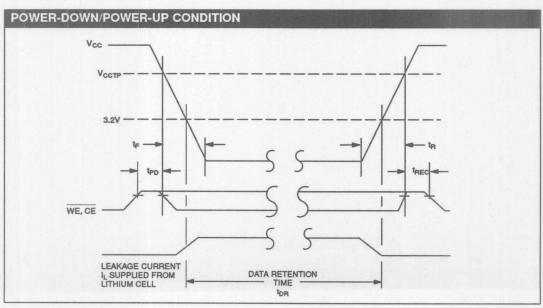












POWER-	DOWN/POWER-UP TIMING					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>PD</sub>	CE, WE, at VIH before Power-Down	0			μs	12
t <sub>TF</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	300			μs	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH)</sub>	0			μs	
tREC	CE, WE at V <sub>IH</sub> after Power-Up	25		125	ms	

$(t_A = 25^{\circ})$						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10			years	9, 11

### WARNING

Under no circumstance are negative undershoots, below 0.5 volts, allowed when device is in battery backup mode.

### NOTES

- 1. WE is high for a Read Cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- 4.  $t_{DH}$ ,  $t_{DS}$  are measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- Each DS1650Y/AB has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is first applied by the user.

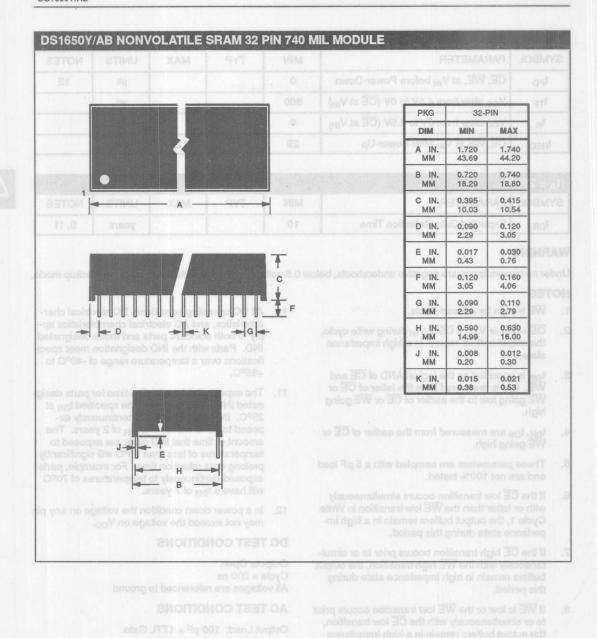
- All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
- 11. The expected data retention time for parts designated IND meet or exceed the specified t<sub>DR</sub> at 25°C. IND parts which are continuously exposed to 85°C will have a t<sub>DR</sub> of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t<sub>DR</sub> of 7 years.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.

### DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V Timing Measurement Reference Levels Input: 1.5V Output: 1.5V Input pulse Rise and Fall Times: 5 ns



# **DALLAS**SEMICONDUCTOR

## DS2016, DS2016S 2K x 8 3V Operation Static RAM

### **FEATURES**

### PIN ASSIGNMENT

- Low power CMOS design
- Standby current

50 nA max at	t <sub>A</sub> = 25°C	$V_{CC} = 3.0V$
100 nA max at		
1 μA max at	$t_A = 60^{\circ}C$	$V_{CC} = 5.5V$

- Full operation for V<sub>CC</sub> = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 150 ns at 5.0V and 250 ns at 3.0V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 24 pin DIP and 24 pin SOIC packages
- Suitable for both battery operate and battery backup applications

A7 🗆	1	24	□ V <sub>cc</sub>
A6 🗆	2	23	_ A8
A5 🗌	3	22	_ A9
A4 [	4	21	WE
A3 🗌	5	20	OE
A2 [	6	19	A10
A1 🗆	7	18	CE
A0	8	17	DQ7
DQ0	9	16	DQ6
DQ1	10	15	DQ5
DQ2	11	14	DQ4
GND [	12	13	DQ3

24 PIN DIP OR 24 PIN SOIC

### PIN DESCRIPTION

A0 - A10		Address Inputs
WE	141	Write Enable Input
OE	OND	Output Enable Input
CE	-	Chip Enable Input
DQ0 - DQ7	-	Data Input/Output
Vcc	-	+5 Volts
GND	-	Ground

### DESCRIPTION

The DS2016 is a 16384 bit low power, fully static random access memory organized as 2048 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ( $\overline{\text{CE}}$ ) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 150 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 250 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2016 is most suitable for low power applications where battery operation or

battery backup for nonvolatility are required. The DS2016 is JEDEC pin compatible with ROM and EPROM of similar density and can be interchanged in the same socket providing flexibility of application in microcomputer systems.

PERATION MODE						
MODE	CE	ŌĒ	WE	A0 - A10	DQ - DQ7	POWER
READ	and Abelen	Q X NZ	Н	STABLE	DATA OUT	Icco
WRITE	L	X	L	STABLE	DATA IN	Icco
DESELECT	L	Н	Н	X	HIGH-Z	Icco
STANDBY	THE BUILDING	X	X	X	HIGH-Z	lccs

SYMBOL	PARAMETER	RATING
Vcc 35 [ 68 3	Power Supply Voltage	-0.3V to +7.0V
V <sub>IN</sub> , V <sub>I/O</sub>	Input, Input/Output Voltage	-0.3 to V <sub>CC</sub> + 0.3V
T <sub>STG</sub>	Storage Temperature	-55°C to +125°C
T <sub>OPR</sub>	Operating Temperature	-40°C to +85°C
T <sub>SOLDER</sub>	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t <sub>A</sub> = 25°	C)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	A - OA	5	10	pF	bož nielašu
Input/Output Capacitance	C <sub>VO</sub>	30	5	12	pF	enolisoliqq

# 4

### +5 VOLT OPERATION

PARAMETER TO THE PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V emiT	lrite Cycle
Input High Voltage	VIH	2.0	120	V <sub>CC</sub> + 0.3	ViduliV	hite Pulse
Input Low Voltage	VIL	-0.3	0	0.8	ViiT qu	el aserbb
Data Retention Voltage	V <sub>DR</sub>	2.0	07	5.5	V	coeff athi

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	IIL	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	1907	±0.1	μА	
I/O Leakage Current	ILO	CE=V <sub>IH</sub> , 0V≤V <sub>IO≤</sub> V <sub>CC</sub>		±0.5	μА	
Output High Current	ГОН	V <sub>OH</sub> = 2.4V	-1.0		mA	IN ATA 6
Output Low Current	X M loL	V <sub>OL</sub> = 0.4V	4.0		mA	PARAMET
Standby Current	I <sub>CCS1</sub>	CE = 2.0V	ngV	0.3	mA	Oata Rota
Standby Current	I <sub>CCS2</sub>	CE <sub>≥</sub> V <sub>CC</sub> -0.5V t <sub>A</sub> =60°C	recol	V8.4 is to	μА	Cata Relo
Standby Current	I <sub>CCS2</sub>	CE <sub>≥</sub> V <sub>CC</sub> -0.5V t <sub>A</sub> =25°C	snoof	V 100	nA	Data Reta
Operating Current	Icco	CE=0.8V min cycle	RGO <sup>3</sup>	55	mA	seeC cirio

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	150			ns	
Access Time	tACC			150	ns	
OE to Output Valid	toE			70	ns	
CE to Output Valid	tco			150	ns	
CE or OE to Output Active	tcoe	5			ns	
Output High-Z from Deselection	top	10		60	ns	
Output Hold from Address Change	t <sub>ОН</sub>	10			ns	

PARAMETER 277/4	SYMBOL	MIN	AM TYP JOS	MAX	UNITS	NOTES
Write Cycle Time	twc	. 150	8.8	Vol	ns ov vi	ower Supp
Write Pulse Width	o t <sub>WP</sub>	120	0.3	ηV I	ns	nput Hilgh V
Address Setup Time	t <sub>AW</sub>	0	1.0-	gV	ns	/ wo.l tuqr
Write Recovery Time	t <sub>WR</sub>	10	0.8	aV .	eg ns V noi	ata Retent
Output High-Z from WE	topw			70	ns	
Output Active from WE	t <sub>OEW</sub>	5			ns	
Data Setup Time	t <sub>DS</sub>	60		AND	ns	BIOLES HOLD
Data Hold Time	t <sub>DH</sub>	0	MOO LIVE	MTS	ns	Talviaria

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V <sub>DR</sub>	2.0	5	mool 5.5	V men	landby Ou
Data Retention Current at 5.5V	I <sub>CCR1</sub>	-0.6V t <sub>A</sub> =60	0.1*	stool 1	μΑ	Randby Gu
Data Retention Current at 2.0V	I <sub>CCR2</sub>	es <sub>ma</sub> r Vē.o-	50*	750	nA inem	tandby Ou
Chip Deselect to Data Retention	tcdr	Van On Val	0=30	dool	μs	Sperading C
Recovery Time	t <sub>R</sub>	2			ms	

### +3 VOLT OPERATION

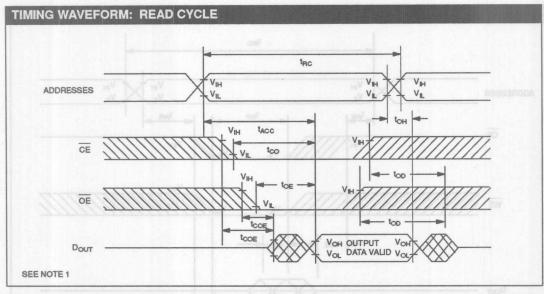
PARAMETER COMMON	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	2.7	3.0	3.5	V emil	rite Cycle
Input High Voltage	V <sub>IH</sub>	2.0	190	V <sub>CC</sub> + 0.3	V drbiVi	rite Pulse
Input Low Voltage	VIL	-0.3	0	0.6	VniT qu	e3 esenbb
Data Retention Voltage	V <sub>DR</sub>	2.0	25	3.5	Village	rite Recov

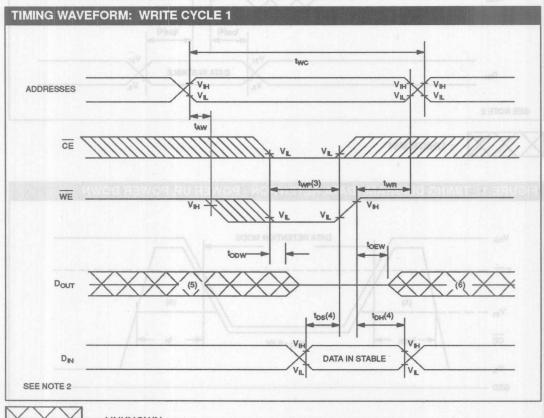
DC CHARACTERISTICS	$t_A = -40^{\circ}C$	10 +85°C, V <sub>CC</sub> = 2.7V	10 3.5	V)		
PARAMETER	SYMBOL CONDITIONS MIN		MIN	MAX	UNITS	NOTES
Input Leakage Current	IIL	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	PSCP	±0.1	μА	
I/O Leakage Current	ILO	CE=VIH, 0V≤VIO≤VCC		±0.5	μА	
Output High Current	loh	V <sub>OH</sub> = 2.2V	-0.5	CHARA	mA	BH ATAC
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0		mA	PARAMET
Standby Current	I <sub>CCS1</sub>	<u>CE</u> = 2.0V	RGV ·	0.1	mA	Onta Rejer
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =60°C	leon	500	nA of	Jain Retn
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =25°C	loonz	50	nA	Oata Flater
Operating Current	Icco	CE=0.6V min cycle	RODI	25	mA	Onip Dese

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	250			ns	
Access Time	tACC			250	ns	
OE to Output Valid	toE			120	ns	
CE to Output Valid	tco	7		250	ns	
CE or OE to Output Active	tcoe	15			ns	
Output High-Z from Deselection	t <sub>OD</sub>	5		100	ns	
Output Hold from Address Change	t <sub>OH</sub>	15			ns	

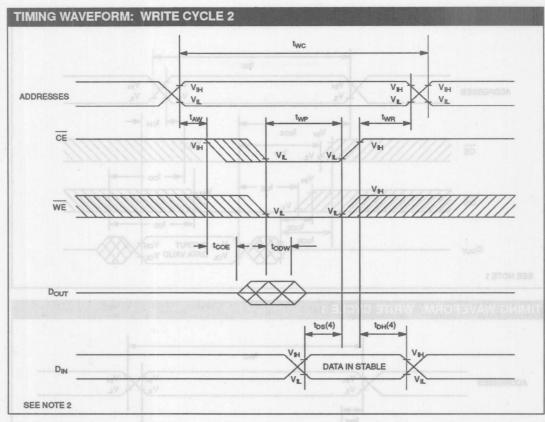
PARAMETER CTIVIL	SYMBOL	MIN	TYP LO	MAX	UNITS	NOTES
Write Cycle Time	t <sub>WC</sub>	250	2.7	Ver	ns	ower Supp
Write Pulse Width	twp	190	0.0	aV	ns	V rigit high V
Address Setup Time	t <sub>AW</sub>	0	8.0-	aV V	ns	V wo.I tuo
Write Recovery Time	t <sub>WR</sub>	25	2.0	sgV .	ns / no	InstaR stanf
Output High-Z from WE	topw			90	ns	
Output Active from WE	toew	5			ns	
Data Setup Time	t <sub>DS</sub>	100		HASE VAS	ns	
Data Hold Time	t <sub>DH</sub>	0	JHOO DO	INTE	ns	S C SHIPLING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V <sub>DR</sub>	2.0	5	3.5		uO ydbna
Data Retention Current at 3.5V	I <sub>CCR1</sub>	03-At V8.0-	50*	1000	nA inst	andby Cu
Data Retention Current at 2.0V	I <sub>CCR2</sub>	es- <sub>A</sub> r ve.o-	50*	750	nA iner	andby Out
Chip Deselect to Data Retention	t <sub>CDR</sub>	W m0 cycle	0-35	dool	μѕ	serating C
Recovery Time	t <sub>R</sub>	2			ms	



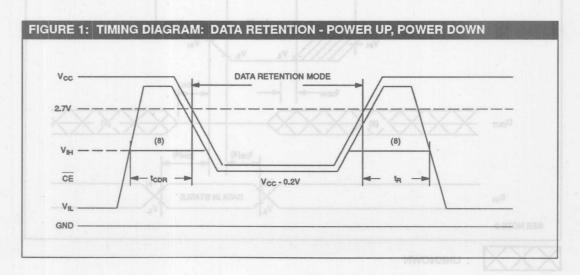


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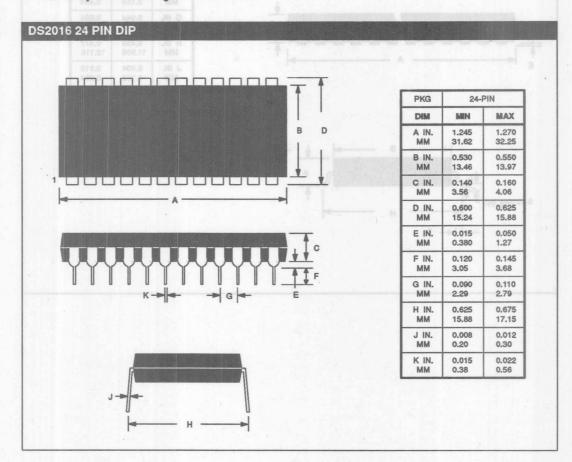
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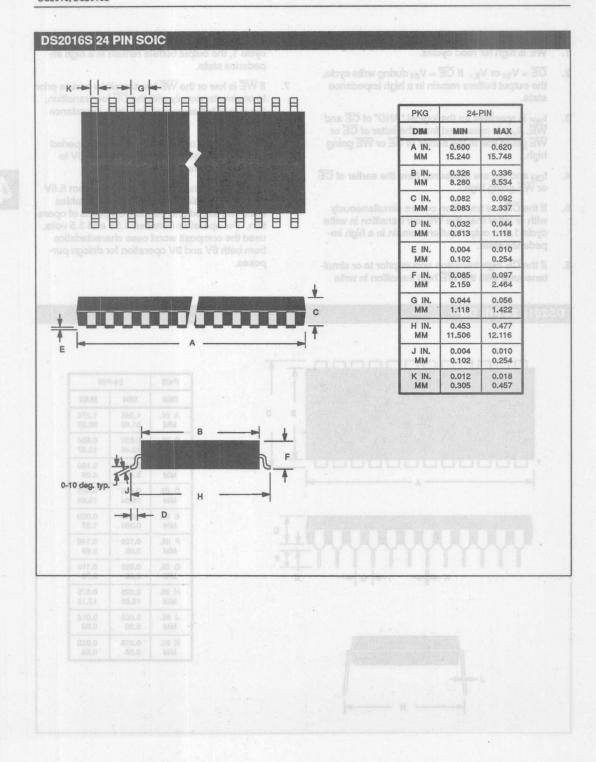


### NOTES

- 1. WE is high for read cycles.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical "AND" of CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
- t<sub>DH</sub> and t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in write cycle 1, the output buffers remain in a high impedance state.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in write

- cycle 1, the output buffers remain in a high impedance state.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state.
- If the V<sub>IH</sub> level of <del>CE</del> is 2.0V during the period that V<sub>CC</sub> voltage is going down from 4.5V to 2.7V l<sub>CCS1</sub> current flows.
- The DS2016 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composit worst case characteristics from both 5V and 3V operation for deisgn purposes.





# DALLAS

## DS2064, DS2064S 8K x 8 3V Operation Static RAM

1 000   Zerte/II		H				15/3	Inlend
FEATURES			PIN ASSIGNI	MEN.	н		
01400	4. X						
Low power CMOS de	esign		NC E	1	28	b vcc	
Standby current			A12 [		27	F WE	
50 nA max at t <sub>A</sub> =	250C Van = 3 0V		A7 [		26	G CE2	
100 nA max at t <sub>A</sub> =			A6 [		25	□ A8	
1 μA max at t <sub>A</sub> =			A5	5	24	□ A9	
F. II A: 4 V	F F\/ 4= 0.7\/		A4 [	6	23	☐ A11	
Full operation for V <sub>C</sub>	C = 5.5V to 2.7V		A3 [	7	22	OE	
Data Retention Volta	age = 5.5V to 2.0V		Othon Jun A2	8	21	A10	
			A1 [	9	20	CE1	
Access time equals 1	50 ns at 5.0V and 3	00 ns at 3.0V	A0 [	10	19	DQ7	
Operating temperatu	re range of -40°C t	DQ0 [	11	18	DQ6		
- who were the set the	ence		DQ1 [	12	17	DQ5	
Full static operation			DQ2 [	13	16	DQ4	
TTL compatible inprange of 5.5V to 2.7	The state of the s	over voltage	GND [	14 28 PIN	DIP OR 28 PIN S	OIC DQ3	
Available in 28 pin D	IP and 28 pin SOIC	packages					
actions emile	II MASE	ave.	PIN DESCRI	PTIO	N		
Suitable for both batt applications	ery operated and ba	attery backup	A0 - A12 WE		ldress Inputs rite Enable Inc		
			ŌĒ	- 0	tput Enable I	nput	
			CE1, CE2	- Ch	nip Enable Inp	uts	
			DQ0 - DQ7	- Da	ata Input/Outp	ut	
			Vcc	- Po	wer Supply Ir	put 2.7V	- 5.5V
			GND	-	round		
			NC	- No	Connection		

### DESCRIPTION

The DS2064 is a 65536 bit low power, fully static random access memory organized as 8192 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ( $\overline{\text{CE}}$ ) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 150 ns when operated from a 5 volt power supply input, and also pro-

vides relatively good performance of 300 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2064 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2064 is JEDEC pin compatible with ROM and EPROM of similar density and can be interchanged in the same socket providing flexibility of application in microcomputer systems.

OPERATION MODE									
MODE	CE1	CE2	ŌĒ	WE	A0 - A12	DQ - DQ7	POWER		
READ	изапрп з	ACH AS	O N. VI	Н	STABLE	DATA OUT	Icco		
WRITE	L	Н	X	L	STABLE	DATA IN	Icco		
DESELECT	L	Н	Н	Н	X	HIGH-Z	Icco		
STANDBY	Н	X	X	X	X	HIGH-Z	Iccs		
STANDBY	X	L	X	X	X	HIGH-Z	Iccs		

ABSOLUTE MAXIMUM R	ATINGS	
SYMBOL	PARAMETER	RATING
Vcc	Power Supply Voltage	-0.3V to +7.0V
VIN, VI/O	Input, Input/Output Voltage	-0.3 to V <sub>CC</sub> + 0.3V
T <sub>STG</sub>	Storage Temperature	-55°C to +125°C
T <sub>OPR</sub> and [ at	Operating Temperature	-40°C to +85°C
T <sub>SOLDER</sub>	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t <sub>A</sub> = 25°C	C)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	A - UA	5	10	pF	inottsollqq
Input/Output Capacitance	CVO	30	5	12	pF	

RECOMMENDED DC OPERATING CONDITIONS (t <sub>A</sub> = -40°C TO +85°C)								
PARAMETER	SYMBOL	MIN	03 TYP	MAX	UNITS	NOTES		
Power Supply Voltage	Vcc	4.5	5.0	5.5	V rittely	feeluse h		
Input High Voltage	V <sub>IH</sub>	2.0	0	V <sub>CC</sub> + 0.3	Vmi q	idness Seh		
Input Low Voltage	V <sub>IL</sub>	-0.3	10	0.8	ry Tin <b>y</b>	evoceFl eth		
Data Retention Voltage	V <sub>DR</sub>	2.0		5.5	EVV nort 3	-rigit High		

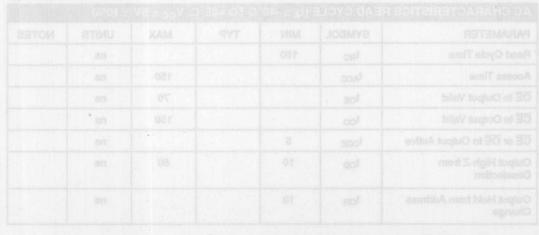
DC CHARACTERISTICS	6 (t <sub>A</sub> = -40°C 1	FO +85°C, $V_{CC}$ = 5V $\pm$	10%)			
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	IIL	$0V \le V_{IN} \le V_{CC}$		±0.1	μА	1 13
I/O Leakage Current	ILO	CE=VIH, OVSVIOSVCC	TERET	±0.5	μА	ATA RE
Output High Current	AM I <sub>OH</sub>	V <sub>OH</sub> = 2.4V	-1.0		mA =	ARAMET
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0	Vokage	mA	eta Relen
Standby Current	I <sub>CCS1</sub>	*1.0 CE = 2.0V	legan	0.3	mA	ata Reten
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.5V t <sub>A</sub> =60°C	snool	vat 2p0V	μА	ata Reten
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.5V t <sub>A</sub> =25°C	наоз	100	nA	hip Desel
Operating Current	Icco	CE=0.8V min cycle		55	mA	10

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	tRC	150			ns	
Access Time	tACC			150	ns	
OE to Output Valid	toE			70	ns	
CE to Output Valid	tco			150	ns	
CE or OE to Output Active	tcoe	5			ns	
Output High-Z from Deselection	top	10		60	ns	
Output Hold from Address Change	tон	10			ns	

PARAMETER	SYMBOL	MIN	TYP	MAX	ŲNITS	NOTES
Write Cycle Time	twc	150	ини Ц	OBMYS -	ns	STEMARIE
Write Pulse Width	a.a t <sub>WP</sub>	120	a.a. I.	ooV Voc	ns	weir Supp
Address Setup Time	t <sub>AW</sub>	0	2.0	HIV	ns	out High V
Write Recovery Time	e.o t <sub>WR</sub>	10	5.0-	J <sub>E</sub> V	ns	West too
Output High-Z from WE	topw		0.8	ng V 70	ns	itaste <b>7</b> i st
Output Active from WE	toew	5			ns	7
Data Setup Time	t <sub>DS</sub>	60			ns	
Data Hold Time	t <sub>DH</sub>	0			ns	

DATA RETENTION CHARACTERISTICS (t <sub>A</sub> = -40°C TO +85°C)									
PARAMETER Am	SYMBOL	MIN	ov TYP	MAX	UNITS	NOTES			
Data Retention Supply Voltage	V <sub>DR</sub>	2.0	oV.	5.5	Vnemut	wo.l tuqtu			
Data Retention Current at 5.5V	I <sub>CCR1</sub>	V0.5 =	0.1*	appl 1	μΑ	landby Cur			
Data Retention Current at 2.0V	I <sub>CCR2</sub>	0.5V ( <sub>A</sub> =60°	50*	750	nA men	bandby Cur			
Chip Deselect to Data Retention	t <sub>CDR</sub>	0.6V 0,	00Vs375	leool	μs	iandby Cur			
Recovery Time	t <sub>R</sub>	2	.0-20	300	ms	A Primary			

<sup>\*</sup> Typical values are at 25°C



## +3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t <sub>A</sub> = -40°C TO +85°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Power Supply Voltage	Vcc	2.7	3.0	3.5	V ribiV	ite Pulse		
Input High Voltage	V <sub>IH</sub>	2.0	0	V <sub>CC</sub> + 0.3	V mT qu	idness Set		
Input Low Voltage	V <sub>IL</sub>	-0.3	25	0.6	vy Tiry	voccit eth		
Data Retention Voltage	V <sub>DR</sub>	2.0		3.5	E front S	riput High		

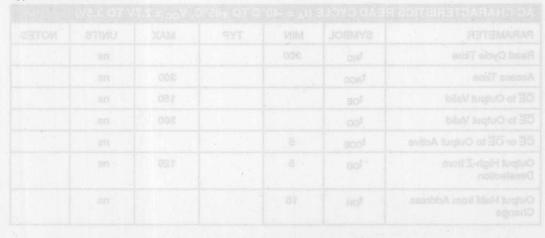
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I	$0V \le V_{IN} \le V_{CC}$		±0.1	μА	
I/O Leakage Current	lo	CE=VIH, 0V≤VIO≤VCC	CHER	±0.5	μА	TE ATA
Output High Current	MAM IOH	V <sub>OH</sub> = 2.2V	-0.5		mA	THIMARA
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0	Voltage	mA	ata Reter
Standby Current	I <sub>CCS1</sub>	CE = 2.0V	POCEL	0.1	mA	ata Retar
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =60°C	loons	500	nA	eta Reter
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =25°C	нао*	50	nA	hip Desel
Operating Current	Icco	CE=0.6V min cycle		25	mA	

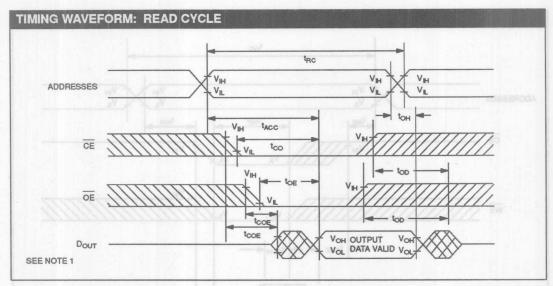
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	300			ns	
Access Time	tACC			300	ns	
OE to Output Valid	toE			150	ns	
CE to Output Valid	tco			300	ns	
CE or OE to Output Active	tcoe	5			ns	
Output High-Z from Deselection	top	5		120	ns	
Output Hold from Address Change	tон	15			ns	

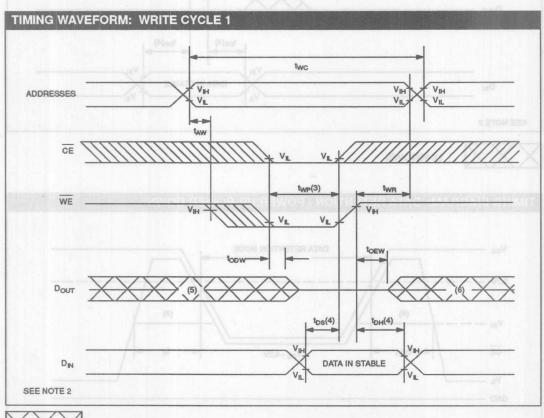
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	twc	300	MIM JO	BMY8	ns	BTBMAR
Write Pulse Width	a.e. t <sub>WP</sub>	225	2.7	Voc	ns	мег Ѕчрр
Address Setup Time	t <sub>AW</sub>	0	2.0	euV Visi	ns	out-High Ve
Write Recovery Time	a twn	25	8,0-	VIL	ns	ov woulder
Output High-Z from WE	topw		2.0	100	e ns V	Ineta7) at
Output Active from WE	toew	5			ns	7
Data Setup Time	t <sub>DS</sub>	150			ns	
Data Hold Time	t <sub>DH</sub>	0	1084-01-0	Um = All 6	ns	THE SE

DATA RETENTION CHARA	CTERISTIC	S (t <sub>A</sub> = -4	0°C TO +8	5°C)		
PARAMETER	SYMBOL	MIN	V TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V <sub>DR</sub>	2.0	ρV	3.5	Vienus	wo.l tuqtu
Data Retention Current at 3.5V	I <sub>CCR1</sub>	V0.5 ==	50*	1000	nA free	tandby Cur
Data Retention Current at 2.0V	I <sub>CCR2</sub>	0.3V 1 <sub>A</sub> =60°	50*	750	nA ins	tandby Curr
Chip Deselect to Data Retention	tcdr	0.3V0	OE <sub>2</sub> V <sub>CC</sub>	locet	μs	tandby Cun
Recovery Time	t <sub>R</sub>	2	0.0220	300*	ms	A Sunsend

<sup>\*</sup> Typical values are at 25°C

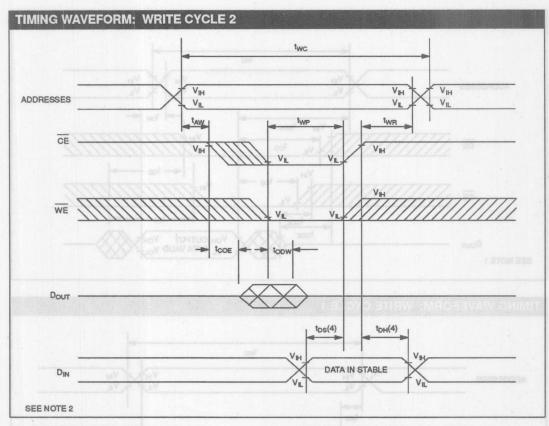






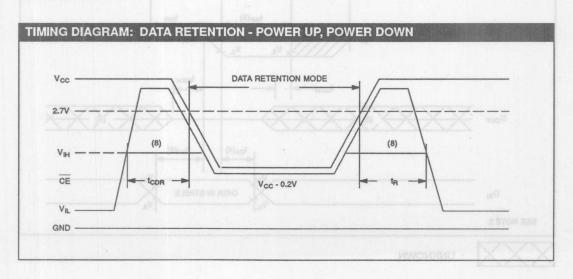
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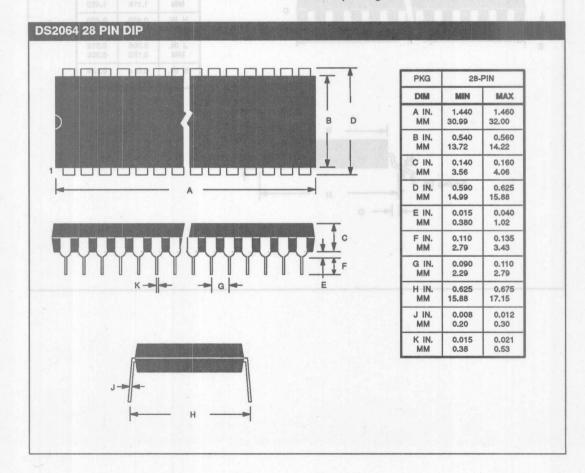
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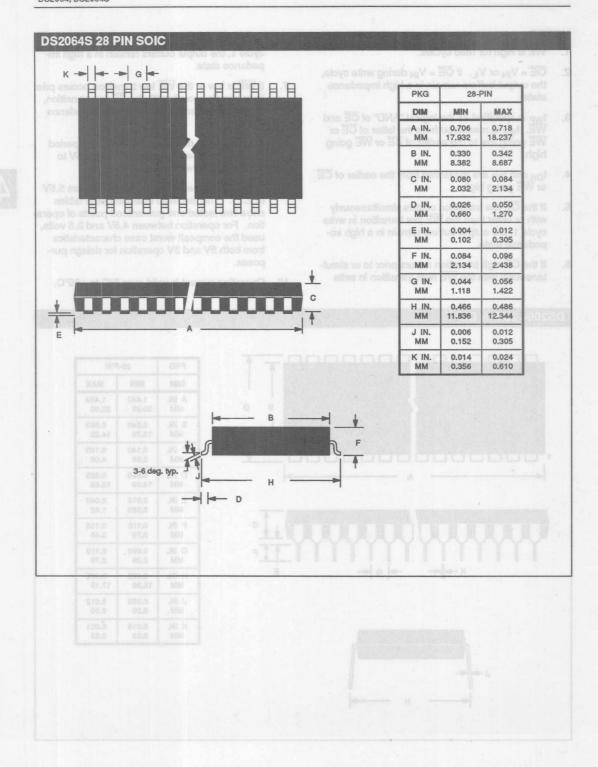


#### NOTES

- 1. WE is high for read cycles.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical "AND" of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- t<sub>DH</sub> and t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in write cycle 1, the output buffers remain in a high impedance state.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in write

- cycle 1, the output buffers remain in a high impedance state.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state.
- If the V<sub>IH</sub> level of CE is 2.0V during the period that V<sub>CC</sub> voltage is going down from 4.5V to 2.7V I<sub>CCS1</sub> current flows.
- The DS2064 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composit worst case characteristics from both 5V and 3V operation for deisgn purposes.
- 10. Operating current is valid over 0°C to +85°C.



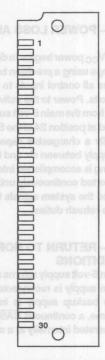


## **FEATURES**

# Nonvolatile DRAM Stik 1M x 9

- · Maintains data in the absence of system power
- Compatible with existing DRAM SIMM applications
- Normal operating mode completely unaffected
- Nonvolatile circuitry transparent and independent from host system
- Conforms to popular JEDEC standard
- 30-position SIMM DRAM module
- Accommodates any 6- to 10-volt primary energy cell or rechargeable energy source
- Memory array available as 1024K bytes with parity bit
- RAS access time of 120 ns or 150 ns
- Power-fail detection at 10% supply ertT .ylqqua gurbad erit to notibno

### **PIN ASSIGNMENT**



30-Pin SIP Stik

### DESCRIPTION

The DS2219 Nonvolatile DRAM Stik 1M x 9 provides all necessary timing, refresh generation, and power-down/ power-up sequencing necessary to maintain data integrity during system power failure. A primary or a rechargeable energy source can be used to support data retention. Available in 1,048,576 bytes, the memory

module conforms to the standard 30-position SIMM pin configuration. The self-contained memory maintenance circuitry resides transparently to the host system, eliminating the need for any additional components. Normal 5-volt operation is completely unaffected as nonvolatile circuitry is transparent to DRAM.

# OPERATION - NORMAL POWER CONDITIONS

Under normal 5-volt operating conditions, the DS2219 Nonvolatile DRAM Stik behaves exactly like a standard 1024K x 9 DRAM SIMM such as the Hitachi HB56A19B. The  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  inputs to the Stik are directed through the DS1237 directly to the individual DRAM circuits. The DS2219 will operate in this mode until the 5-volt supply at  $V_{CC}$  decays to 4.5 volts during loss of power.

### OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt  $V_{\rm CC}$  power begins to drop, the DS1237 senses this change using a precision band gap comparator and isolates all control inputs to the Stik as  $V_{\rm CC}$  falls below 4.5 volts. Power to the individual DRAM circuits is switched from the main 5-volt supply to a backup supply connected at position 24 of the Stik. This backup supply is typically a chargeable capacitor or battery; however, any supply between six and ten volts is suitable. All refreshing is accomplished internally within the Stik and is supported continuously until  $V_{\rm CC}$  returns to normal levels and the system signals the Stik that it is ready to assume refresh duties.

# OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the system 5-volt supply returns and exceeds 4.5 volts, the system supply is reconnected to the DRAM circuits and the backup supply is internally disconnected. At this time, a continuous CAS before RAS refresh is also generated internally at a cycle time of 350

ns maximum. Refreshing continues without interruption until the system signals the Stik that it is ready to assume refresh responsibility for the DRAMs. Refresh duties are shifted from the Stik to the system when a software-controlled switch is set by sending a specific pattern on address lines A5, A6, and A7 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. This address pattern is clocked into the DS1237 DRAM Nonvolatizer Chip resident on the Stik on the falling edge of  $\overline{CAS}$  provided that setup and hold times are met. When the 24th cycle is correctly entered, the system will have full access to RAM and must handle refresh requirements. RAM read and write cycles can then resume without restriction.

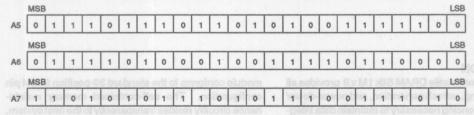
### CONSERVATION OF BACKUP SUPPLY

Another software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. The bit patterns shown in Figure 2 turn on or off this switch which disconnects or connects the backup supply.

### **BACKUP CONDITION**

The DS2219 contains two features which provide information about the condition of the backup supply. The  $\overline{BC}$  (Battery Condition) pin at location 19 of the Stik provides the output for the backup supply information. If this feature is to be used, please review the "Backup Condition" section of the DS1237 DRAM Nonvolatizer Chip data sheet.

### SOFTWARE SWITCH FOR PROCESSOR CONTROL POWER-UP Figure 1



### SOFTWARE CONTROLLED SWITCH FOR CONSERVATION OF BACKUP SUPPLY Figure 2

	MSB					14			174	BAT	TER	Y BA	СКИ	PON	De	evi	isle	SI et	uqn Jose	l yns	tini Let	i iqs	KOK.	LSB
	0	1	1	1	0	1	1	1	0	1	10	0	1	0	1	0	0	1	1	1	1	1	0	0
	MSB							P G	11+1	al U	-86													LSB
	0	1	1	1	1	0	1	0	0	0	1	0	0	1	1	1	1	0	1	1	0	0	0	0
	MSB	eju	ose	is o	ST	16.0	qel	lb	oller	mi de	m a	noi	tao	The	qa r	ild	lo a	noti	003	noi	lene	qo e	arti	LSB
7	1	1	0	1	0	1	0	1	1	1	0	1	0	1	1	1	0	0	1	1	1	0	1	0
	MSB	0	90)							BAT	TER	Y BA	CKUI	OF	ioi	TIO	ио	01	MI	TAF	199	o:	90	LSB
	1	1	1	1	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	1	1	0	0
	MSB			1		I		i A			0.8		I		in dealer			J.V			of the same		vio	LSB
	0	1	1	1,	1	0	1	0	0	0	1	0	0	1	1	1	1	0	1	1	0	0	0	0
	MSB																							LSB
	INIOD					_	-	-	-	-	-	-	-	-	-	-	-	-	_	_	-	-	_	_

NOTE: ABOVE SEQUENCES ENTERED LSB FIRST.

### PIN DESCRIPTION Table 1

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1 Am	Vcc	16	DQ4
8 2 V	CAS	4.25 71 4.37	A8
3 A	DQ0	18	A9
4	AO	19	BC
5 0000	10°0\ A1	20	DQ5
6	DQ1	21	WE
7	A2	22	GND
8	A3	23	DQ6
9	GND	24	V <sub>BAT</sub>
10 2114	DQ2	25	DQ7
11 Ag	A4	26	PQ
12	A5	27	RAS
8 of 13	DQ3	28	PCAS
14	A6	29	PD
15	A7	30	Vcc

### ABSOLUTE MAXIMUM RATINGS\* MOTTAN RESIDED ROT HOTHWA DE MOSTINOS ESPANTROS

Voltage on Any Pin Except Battery Inputs Relative to Ground
-0.3V to +7V
Voltage on Any Pin Relative to Ground
-0.3V to +72V
-0.3V to +12V
Operating Temperature
0°C to +75°C
Storage Temperature
-55°C to +125°C

### **RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Voltage Input Logic 1	V <sub>IH</sub>	2.0	10 11 10	V <sub>CC</sub> +0.3	V	1
Voltage Input Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1
Backup Supply	BKUP	6.0	8.0	10.0	V	2,3

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	lcc	la la		15	mA	1
Power-Fail Detect	○V <sub>TP</sub>	4.25	4.37	4.5	V	2 5
Input Leakage	@A <sub>IIL</sub>	-1.0		1.0	μА	8

(0°C to 70°C, V<sub>CC</sub> < V<sub>TP</sub>)

Data Retention Current	I <sub>DR</sub>	7	15	mA	4
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### CAPACITANCE

(tA =25°C)

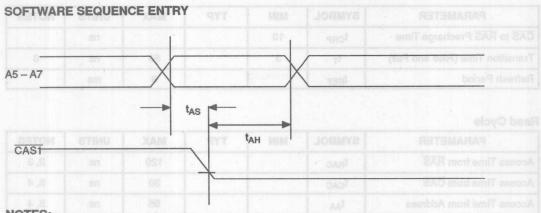
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	0	5	7	pF	13

### **AC ELECTRICAL CHARACTERISTICS**

(0°C to 70°C, V<sub>CC</sub>=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	tas	0			ns	
Address Hold Time	t <sub>AH</sub>	20			ns	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.



### NOTES:

- 1. All voltages are referenced to ground.
- The BC pin will be driven active whenever V<sub>CC</sub> is within nominal limits and the backup supply is below V<sub>CC</sub>.
- 3. Backup input voltage is internally regulated within the DS2219 such that V<sub>CC</sub> to the DRAMs is never below 4.5 volts, for a backup input voltage of 6.0 volts minimum.
- 4. This is the average current from the backup supply to maintain memory for the Stik.
- 5. V<sub>TP</sub> is the trip point where the internal switching circuit disconnects V<sub>CC</sub> and connects the internally regulated backup supply to the DRAMs. Rapid refresh is also initiated at this time.

### **AC ELECTRICAL CHARACTERISTICS**

 $(t_A = 0 \text{ to+} 70^{\circ}\text{C}, V_{CC} = 5\text{V} \pm 10\%)$ 

### **Test Conditions**

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Random Read or Write Cycle Time	t <sub>RC</sub>	220	How	em	ns	Write Com
RAS Precharge Time	t <sub>RP</sub>	90	3397	THE ST	ns	DEAD COME
RAS Pulse Width	t <sub>RAS</sub>	120	49014*	10000	ns	HINN COLLEGE
CAS Pulse Width	tcas	30	3450	10000	ns	THOU BENE
Row Address Setup Time	t <sub>ASR</sub>	0	801		ns	SO INCUSING
Row Address Hold Time	tRAH	15	1 1404		ns	277 137-131155
Column Address Setup Time	tasc	0			ns	
Column Address Hold Time	tCAH	25	T variable	- Wind	ns	10/11-016
RAS to CAS Delay Time	t <sub>RCD</sub>	25	1.000010	90	ns	7
RAS to Column Address Delay Time	t <sub>RAD</sub>	20	- dwa <sup>‡</sup>	65	ns	10
RAS Hold Time	t <sub>RSH</sub>	30	towo!		ns	W of SAS
CAS Hold Time	t <sub>CSH</sub>	120	dwal	Jelay Time	ns	Solumn Ast

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CAS to RAS Precharge Time	t <sub>CRP</sub>	10		1	ns	
Transition Time (Rise and Fall)	t <sub>T</sub>	3		50	ns	6
Refresh Period	t <sub>REF</sub>	1		8	ms	TA-

Read Cycle

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Access Time from RAS	tRAC		/	120	ns	2,3
Access Time from CAS	tcac			30	ns	3, 4
Access Time from Address	t <sub>AA</sub>			55	ns	3, 4
Read Command Setup Time	t <sub>RCS</sub>	0	b	suono et bec	ns	annilos IIA
Read Command Hold Time Referenced to CAS	tRCH	mon Pirthw	anever V <sub>CC</sub>	n áctive wh	ns	This BC pt
Read Command Hold Time Referenced to RAS	t <sub>RRH</sub>	10	leim allov 0.	meannaunt voltage of t	ns	sadkup m rolls, for a
Column Address to RAS Lead	t <sub>RAL</sub>	55	que quiosa poidolive las	ent non me ne the inter	ns	This is the Vip is the
Output Buffer Turn-Off Delay	toff	DESTRUCTION OF	a mener b	30	ns	5

Write Cycle

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Command Setup Time	twcs	0	Tograss		ns	8
Write Command Hold Time	twcH	25	i oni	Sycle	ns	Filmotanaf
Write Command Pulse Width	t <sub>WP</sub>	20	-		ns	Sound DAY
Write Command to RAS Lead Time	t <sub>RWL</sub>	30			ns	anh G SAS
Write Command to CAS Lead Time	t <sub>CWL</sub>	30			ns	and SA
Data-In Setup Time	t <sub>DS</sub>	0			ns	9
Data-In Hold Time	t <sub>DH</sub>	25			ns	9

Read-Modify-Write Cycle

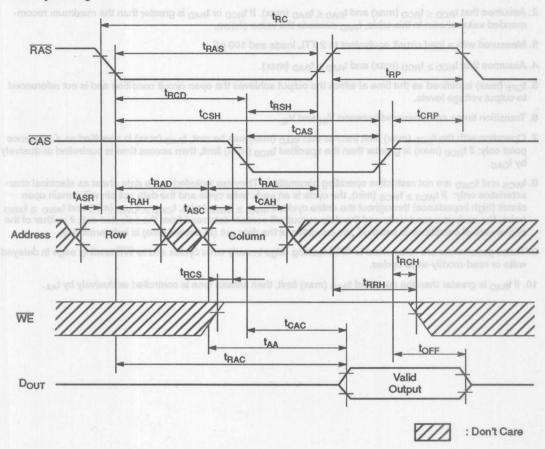
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read-Write Cycle Time	t <sub>RWC</sub>	245	Taken to the same of the same		ns	D == 57.0
RAS to WE Delay Time	t <sub>RWD</sub>	110.			ns	8
CAS to WE Delay Time	tcwD	30	HBB		ns	bol 8
Column Address to WE Delay Time	t <sub>AWD</sub>	55	test		ns	b 8 A

# 4

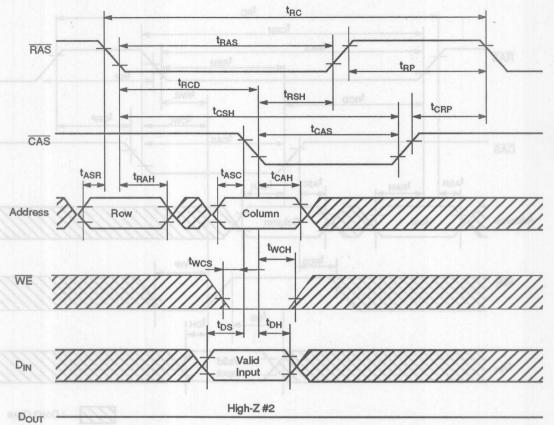
#### NOTES:

- 1. AC measurements assume  $t_T = 5$  ns.
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max) and t<sub>RAD</sub> ≤ t<sub>RAD</sub> (max). If t<sub>RCD</sub> or t<sub>RAD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> exceeds the value shown.
- 3. Measured with a load cirucit equivalent to 2 TTL loads and 100 pF.
- 4. Assumes that  $t_{RCD} \ge t_{RCD}$  (max) and  $t_{RAD} \le t_{RAD}$  (max).
- t<sub>OFF</sub> (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 6. Transition times are measured between VIH and VIL.
- 7. Operation with the t<sub>RCD</sub> (max) limit insures that t<sub>RAC</sub> (max) can be met, t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> (max) is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
- 8. t<sub>WCS</sub> and t<sub>CWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min), t<sub>CWD</sub> ≥ t<sub>CWD</sub> (min) and t<sub>AWD</sub> ≥ t<sub>AWD</sub> (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
- 10. If t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (max) limit, then access time is controlled exclusively by t<sub>AA</sub>.

# TIMING WAVEFORMS Read Cycle Figure 3



#### Early Write Cycle Figure 4

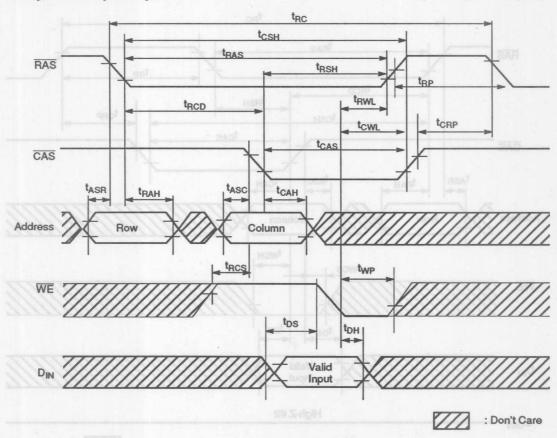


Notes: 1.

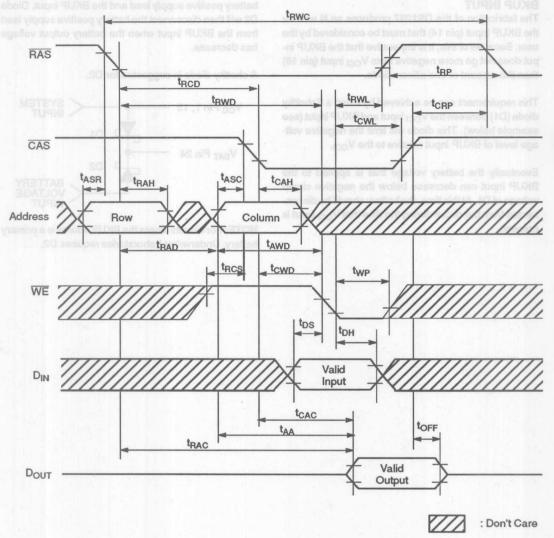
: Don't Care

2. twcs ≥ twcs (min)

#### **Delayed Write Cycle** Figure 5



#### Read-Modify-Write Cycle Figure 6



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## APPLICATION NOTE: DIODE CONTROL OF BKUP INPUT

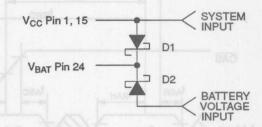
The fabrication of the DS1237 produces an N well for the BKUP Input (pin 14) that must be considered by the user. Because of this, it is imperative that the BKUP input does not go more negative from V<sub>CCI</sub> input (pin 16) than the amount of one silicon diode.

This requirement can be achieved by using a Schottky diode (D1) between the  $V_{\rm CCI}$  input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the  $V_{\rm CCI}$ .

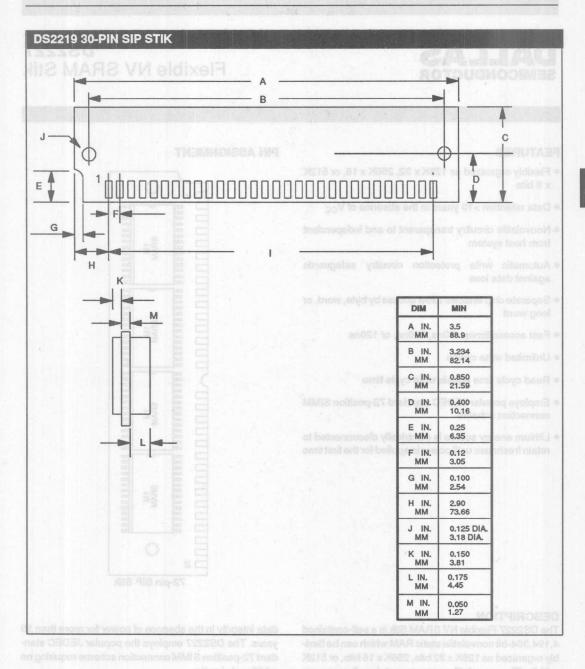
Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V<sub>CCI</sub> input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive supply lead from the BKUP input when the battery output voltage has decrease.

A shottky diode is suggested for D2.



**NOTE:** For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.





#### DS2227 Flexible NV SRAM Stik

#### **FEATURES**

- Flexibly organized as 128K x 32, 256K x 16, or 512K x 8 bits
- Data retention >10 years in the absence of V<sub>CC</sub>
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate chip enables allow access by byte, word, or long word
- Fast access times: 70ns, 100ns, or 120ns
- Unlimited write cycles
- · Read cycle time equals write cycle time
- Employs popular JEDEC standard 72-position SIMM connection scheme
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

# HERRERERER REPRESENTATION OF THE PRESENTATION OF THE PRESENTATION

PIN ASSIGNMENT

#### 72-pin SIP Stik

0

72

#### DESCRIPTION

The DS2227 Flexible NV SRAM Stik is a self-contained 4,194,304-bit nonvolatile static RAM which can be flexibly organized as 128K x 32 bits, 256K x 16 bits, or 512K x 8 bits. The nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain

data integrity in the absence of power for more than 10 years. The DS2227 employs the popular JEDEC standard 72-position SIMM connection scheme requiring no additional circuitry.

#### OPERATION of botoeles of apation teached and rife

The DS2227 Flexible NV SRAM Stik is used like any standard static RAM. All the nonvolatile circuitry resides transparently to the user. The flexibility of the part is achieved by providing separate read, write, and chip select pins for each of the four banks of onboard memories (see Figure 1). For operation as a 512K x 8 NV SRAM Stik, tie all data lines from each bank together (i.e., all D0s together, all D1s together, etc.). Read enables and write enables are also tied together. For operation as a 256K x 16 NV SRAM Stik, tie the data lines from two banks together. Chip enables, read enables, and write enables from these banks are also tied together. Connection to the DS2227 is made by using an industry-standard, 72-position SIMM socket DS9072-72V (AMP part number 821824-8). These SIMM sockets are also available in perpendicular, inclined, or parallel mount, depending on the height available. See the DS907x SipStik<sup>TM</sup> connectors available from Dallas Semiconductor.

#### **READ MODE**

The DS2227 executes a read cycle whenever  $\overline{WE}$  is inactive (high) and  $\overline{CE}$  is active (low). The unique address specified by the 17 address inputs (A<sub>0</sub> - A<sub>16</sub>) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within  $t_{ACC}$  (access time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access. Read cycles can only occur when  $V_{CC}$  is greater than 4.5 volts. When  $V_{CC}$  is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

#### WRITE MODE

The DS2227 is in the write mode whenever both WE and CE signals are in the active (low) state after address

inputs are stable. The latter occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) during write cycles to avoid bus contention. However, if the output bus has been enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs to  $t_{ODW}$  from its falling edge. Write cycles can occur only when  $V_{CC}$  is greater than 4.5 volts. When  $V_{CC}$  is less than 4.5 volts, the memory is write-protected.

#### **DATA RETENTION MODE**

The DS2227 provides full functional capability for  $V_{CC}$  greater than 4.5 volts and guarantees write protection for  $V_{CC}$  less than 4.5 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS2227 constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects the external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

The DS2227 checks lithium status to warn of potential data loss. Each time that  $V_{\rm CC}$  power is restored to the DS2227 the lithium is checked with a precision comparator. If the lithium supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications data integrity is paramount. The DS2227 provides lithium cell redundancy and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the lithium with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user.

#### PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME	
Vrite cycl	V <sub>CC</sub> Power	ghuo ent 38 is seld	together, all D1s together, etc. 00-4 denal	200
2	a A ruf 1-D0 sarp al op V nerwythe v.	39 39	tanago 4-D1 entregot belt cels ens soldane e	
3	less than 4.5 volts, thet d-thocy i	40	4-D2 of of Ala MARE VA BLX X	
4	1-D2	betset 41 my br	4-D3 del seldene qui D dellegel ax	
5	1-D3	42	4-D4 als era alred ceast mort sold	
6	1-D4	43	40D5	
7/ 40/ 40/	1-D5	44	4-D6	
8	1-D6 out bos after 8.4 mark	rens are.	4-D7	
99	es than 4.5 volts. Data 70-1 intain	W	NC	
10	gous NC libbs yns tuediw 55V I	7 TOTAL BEST	4-Chip Enable	
11 orli blu	1-Chip Enable	The second secon	4-Output Enable	
12		49	4-Write Enable	
13	1-Write Enable	50	Ground	
14		0.8 VI 51	V <sub>CC</sub> Power	
15		52	AO AO E DE LE COMPANIE DE LE COMPANI	
16	2-D2	53	eupinu A1 (low) evide (low). The unique	
17	2-D3	54	A2	
18	2-D4	55	A2	
19	2-D5	EG	AS and Od stab from on deal	
20	2-D6	57	A5 A5 A S A S A S A S A S A S A S A S A	
21		58	A6 believes for less semil 30 time	
22		59 1016		
23	2-Chip Enable		and the limiting parameter is eliAA Loo for	
24	2-Output Enable	di notes 61 conto	for OE rather than address scote QA and by	
25	2-Write Enable	62	A10 of setsoig al goV deriv succe	
26	3-D0	63		
27	3-D1 ni nobasol yas of c	64	A12 berongi eta sedes	
28	3-D2	65	A13	
29	3-D3	66	A14 Enow Emi	
30	3-D4	67	DS2227 is in the write mode 21A ever i	
31	3-D5	68	CE signals are in the active (low A16 a after	
32	3-D6	69	NC	
33	3-D7	70	NC	
34	NC	71	NC	
35	3-Chip Enable	72	Ground	
36	3-Output Enable	12	Citatio	
37	3-Write Enable			

NOTE: Leave all pins marked as NC unconnected.

4

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground

Operating Temperature

O°C to 70°C

Storage Temperature

-0.3V to +7.0V

O°C to 70°C

-40° to +85°C

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN OT	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	٧	er 25 to 3
Input High Voltage	V <sub>IH</sub>	2.2		Vcc	V	BOPT RAUGH
Input Low Voltage	V <sub>IL</sub>	0		+0.8	V	diput nugiti

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	IIL I	-1.0	ae	+1.0	μА	agin Pulge
I/O Leakage Current	ILO	-5.0	101	+5.0	μА	dines Se
Output Current @ 2.4V	Іон	-1.0	1 68 1	RWI	mA	opeR eth
Output Current @ 0.4V	loL	2.0	3.0	Wrgo <sup>1</sup>	mA	Bild tridin
Operating Current	loc	8 1	60	280	mA	ADA JUGAL

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		20	40	pF	
Output Capacitance	C <sub>OUT</sub>		5	10	pF	

#### POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE at V <sub>IH</sub> Before Power-down	t <sub>PD</sub>	0			μѕ	
V <sub>CC</sub> Slew from 4.5V to 4.25V (CE at V <sub>IH</sub> )	t <sub>F</sub>	300			μѕ	
V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	t <sub>R</sub>	0			μѕ	
CE at V <sub>IH</sub> after Power-up	tREC	2	80	125	ms	

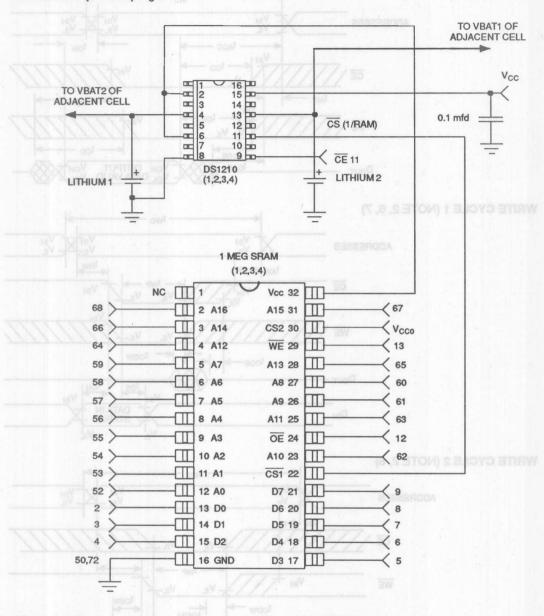
 $(t_A = 25^{\circ}C)$ 

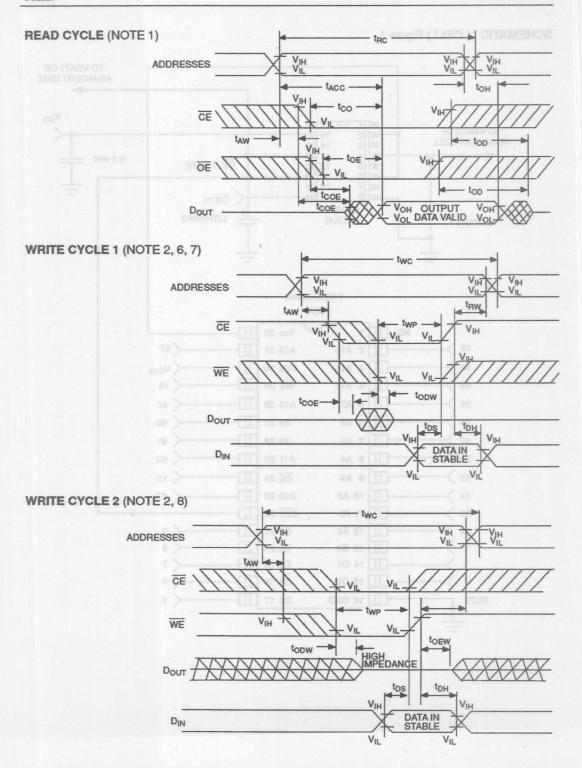
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t <sub>DR</sub>	. 10			Years	

#### AC ELECTRICAL CHARACTERISTICS

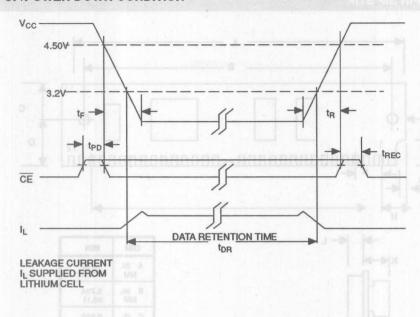
		DS22	27-70	DS22	27-100	DS22	27-120	utereqme	perating
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	70	oificatio	100	o anolto	120	ne open	ns	10
Access Time	tACC	310170	70	DELIE TO	100	Granten A	120	ns	10
OE to Output Valid	toE		35	MOITIO	50	HTAR:	60	ns	10
CE to Output Valid	tco	TYP	70	M	100		120	ns	10
OE or CE to Output Active	t <sub>COE</sub>	5		5	y Vec	5	. 0	ns	10
Output High Z from Deselection	top		25		35		40	ns	10
Output Hold from Address Change	фон	5		5	encs	5	CHARA	ns	10
Write Cycle Time	twc	70	1/1	100	OBMYS	120	Ra	ns	10
Write Pulse Width	t <sub>WP</sub>	55	0	75	T pl	90	In	ns	3,10
Address Setup Time	taw	0	0	0	o.l	0		ns	10
Write Recovery Time	t <sub>WR</sub>	20	0	20	und	20	Va	ns	10
Output High Z from WE	topw	0.8	25	2	35	1	40	ns	10
Output Active from WE	toew	5		5	nol	5		ns	8,10
Data Setup Time	t <sub>DS</sub>	30		40		50		ns	4,10
Data Hold Time from WE	t <sub>DH</sub>	20		20		20		ns	4,5,10







#### POWER-UP/POWER-DOWN CONDITION



#### NOTES:

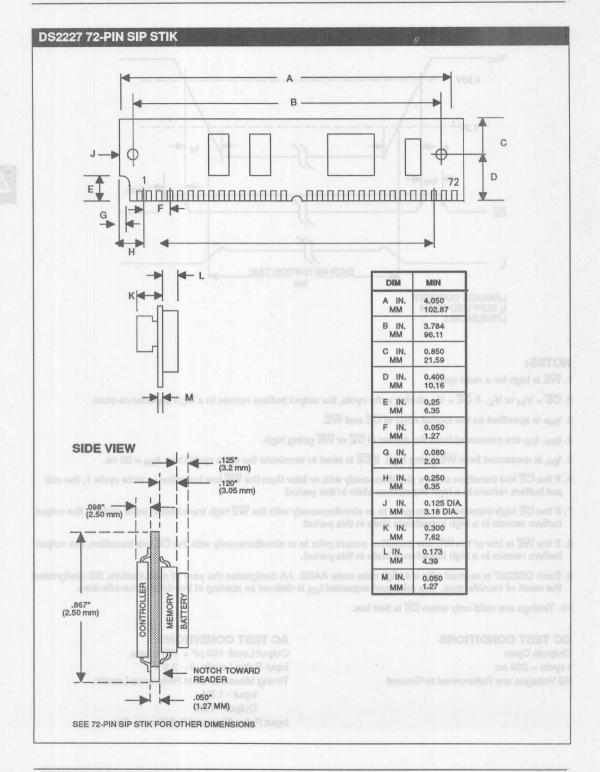
- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- 3. twp is specified as the logical AND of CE and WE.
- 4. tDH, tDS are measured from the earlier of CE or WE going high.
- 5.  $t_{DH}$  is measured from WE going high. If  $\overline{CE}$  is used to terminate the write cycle then  $t_{DH} = 20$  ns.
- 6. If the CE low transition occurs simultaneously with or later than the WE low transition in write cycle 1, the output buffers remain in a high impedance state in this period.
- 7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition in write cycle 1, the output buffers remain in a high impedance state in this period.
- 8. If the WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state in this period.
- Each DS2227 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates
  the week of manufacture. The minimum expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- 10. Timings are valid only when CE is tied low.

#### DC TEST CONDITIONS

Outputs Open t cycle = 200 ns All Voltages are Referenced to Ground

#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL gate
Input Pulse Levels: 0 – 3.0 V
Timing Measurements Reference Levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5ns





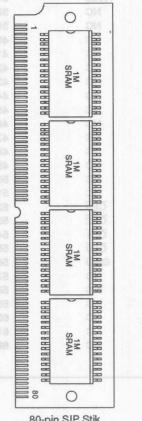


#### **DS2229** Word-Wide 8 Meg SRAM Stik

#### **FEATURES**

- Organized as a high density 512K x 16 bit Stik<sup>TM</sup>
- Fast access times 85ns, 100ns, 120ns
- Unlimited write cycles
- Employs popular JEDEC standard 80-position SIMM connector
- Full ± 10% operating range
- · Read cycle time equals write cycle time
- Ultra-low standby current < 20 μA</li>
- Suitable for battery-backed applications

#### PIN ASSIGNMENT



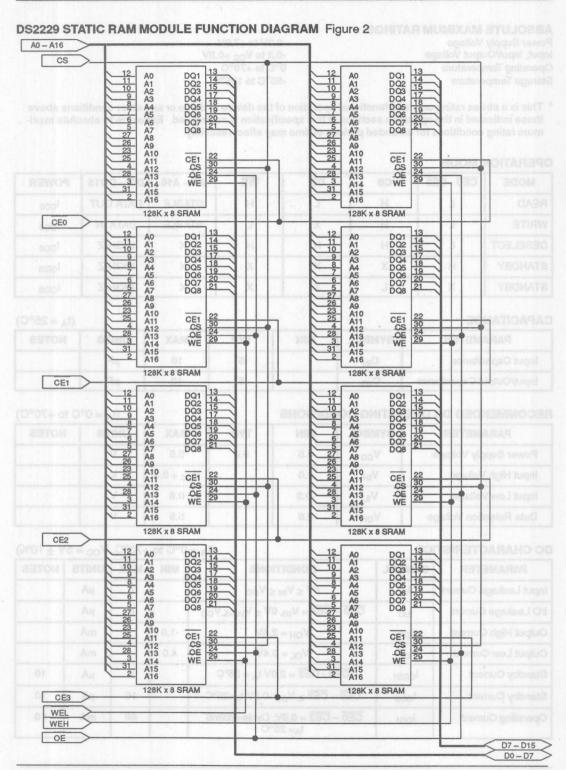
80-pin SIP Stik

#### DESCRIPTION

The DS2229 is a 8,388,608-bit low-power fully static Random Access Memory organized as a 524,888 word by 16 bits using CMOS technology. The device employs the popular JEDEC standard 80-pin SIMM connection scheme with no additional circuitry required. The device operates from a single power supply with a voltage input of 4.5 to 5.5 volts. The Chip Enable inputs (CEO, CE1, CE2, CE3) are used for device selection and can be used in order to achieve the minimum standby current mode which facilitates battery backup. The device provides a fast access time of 85nS. The DS2229 maintains TTL levels over input voltage range 4.5V to 5.5V. The DS2229 is JEDEC pin compatible (see Figure 1) with flash EEPROM memory SIMM boards of similar density.

#### **PIN DESCRIPTION** Figure 1

PIN#	PIN NAME	PIN#	PIN NAME	PIN# PI	N NAME
1	GND	32	NC	63	DQ <sub>7</sub>
2	Vcc	33	NC	64	DQ <sub>6</sub>
3	NC	34	NC	65	DQ <sub>5</sub>
4	OE	35	CS	66	DQ <sub>4</sub>
5	WEH	36	A <sub>16</sub>	67	DQ <sub>3</sub>
6	WEL	37	A <sub>15</sub>	68	DQ <sub>2</sub>
7	NC _	38	A <sub>14</sub>	69	DQ <sub>1</sub>
8	NC	39	A <sub>13</sub>	70	DQ <sub>0</sub>
9	NC	40	A <sub>12</sub>	71	NC
10	NC	41	A <sub>11</sub>	72	V <sub>CC</sub>
- 11	NC	42	A <sub>10</sub>	73	NC
12	NC	43	A <sub>9</sub>	74	GND
13	NC	44	A <sub>8</sub>	75	NC
14	NC	45	A <sub>7</sub>	76	GND
15	NC	46	A <sub>6</sub>	77	GND
16	NC	47	A <sub>5</sub>	78	
17	NC	48	A <sub>4</sub>	79	
18	NC	49	A <sub>3</sub>	80	GND
19	NC	50	A <sub>2</sub>		
20	NC	51	A <sub>1</sub>		
21	CE3	52	A <sub>0</sub>	PIN NAME	DESCRIPTION
22	CE2	53	GND	A <sub>0</sub> - A <sub>16</sub>	Address Input
23	CE1	54	GND	WEL	Write Enable Input Low
24	CE0	55	DQ <sub>15</sub>	WEH	Write Enable Input High
25	GND	56	DQ <sub>14</sub>	ŌĒ	Output Enable Input
26	NC	57	DQ <sub>13</sub>	NC	No Connect
27	NC	58	DQ <sub>12</sub>	CEO - CE3	Chip Enable Input
28	NC	59	DQ <sub>11</sub>	CS	Chip Select
29	NC	60	DQ <sub>10</sub>	DQ0 - DQ15	Data Input/Output
30	NC	61	DQ <sub>9</sub>	Vcc	+5 Volts
31	NC	62	DQ <sub>8</sub>	GND	Ground



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#### ABSOLUTE MAXIMUM RATINGS\*

Power Supply Voltage Input, Input/Output Voltage Operating Temperature Storage Temperature -0.3V to +7.0V -0.3 to V<sub>CC</sub> +0.3V 0°C to +70°C -55°C to 125°C

#### **OPERATION MODE**

MODE	CEO - CE3	CS	OE	WE	A0 - A16	DQ - DQ15	POWER
READ	L	H 917	J	Н	STABLE	DATA OUT	Icco
WRITE	L	Н	X	L	STABLE	DATA IN	Icco
DESELECT	L	200H 1	Н	Н	×	HIGH-Z	Icco
STANDBY	н	X	X	X	X	HIGH-Z	Iccs
STANDBY	X	700 L 8	X	X	X	HIGH-Z	Iccs

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	110120
Input/Output Capacitance	C <sub>VO</sub>		5	12	pF	130

#### RECOMMENDED DC OPERATING CONDITIONS

 $(t_A = 0^{\circ}C t_{0} + 70^{\circ}C)$ 

TOOMINE HAPED DO OF	LITATING COL	DITION			(1A -0 0 10 +10 0	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Input High Voltage	VIH	2.0		V <sub>CC</sub> + 0.3	V	
Input Low Voltage	VIL	-0.3	H	0.8	V	
Data Retention Voltage	V <sub>DR</sub>	2.0		5.5	V	

#### DC CHARACTERISTICS

 $(t_A = 0^{\circ}C \text{ to } +70^{\circ}C, V_{CC} = 5V \pm 10\%)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	$0V \le V_{IN} \le V_{CC}$		8	μА	
I/O Leakage Current	ILO	$\overline{CE0} - \overline{CE3} = V_{IH}, 0V \le V_{I/O} \le V_{CC}$		8	μА	
Output High Current	ОН	V <sub>OH</sub> = 2.4V	-1.0		mA	
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0	A RE	mA	
Standby Current	I <sub>CCS1</sub>	CE0 - CE3 = 2.0V t <sub>A</sub> = 25°C		8	μА	10
Standby Current	Iccs	CE0 - CE3 ≥ V <sub>CC</sub> -0.3V t <sub>A</sub> =25°C	PR 6 x MB	10	μА	10
Operating Current	I <sub>CC1</sub>	CE0 - CE3 = 0.8V; Cycle=200nS t <sub>A</sub> = 25°C		60	mA	10

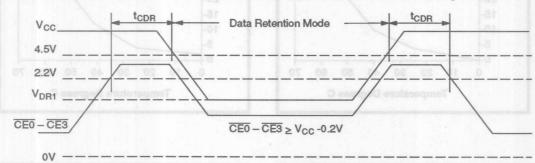
<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### LOW VCC DATA RETENTION CHARACTERISTICS

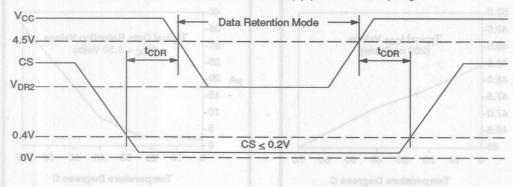
ĺ	t A	_	0	to	+7	0	0	C	١
١	(A	-	v	CO	TI	v	-	0	ì

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION		
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	2.0	pedance	ne high in	V	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		
Data Retention Current	ICCDR	-	1	8	μ <b>Α</b>	$\begin{split} &V_{CC} = 3.0 \text{V, } V_{\text{IN}} \geq 0 \text{V } \overline{\text{CE0}} \\ &- \overline{\text{CE3}} \geq V_{CC} \text{-0.2V, } \text{CS} \geq \\ &V_{CC} \text{-0.2V or} \\ &0 \text{V} \leq \text{CS} \leq 0.2 \text{V } t_{\text{A}} \text{=} 25 ^{\circ} \text{C} \end{split}$		
Chip Deselect to Data Retention Time	tcDR	0	-	-	ns	See Retention Waveform		
Operation Recovery Time	t <sub>R</sub>	5	-	1-	ms	J. Hericalt 20		

#### LOW VCC DATA RETENTION TIMING WAVEFORM (1) (CEO - CE3 Controlled) Figure 3



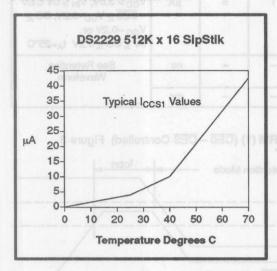
#### LOW VCC DATA RETENTION TIMING WAVEFORM (2) (CS Controlled) Figure 4

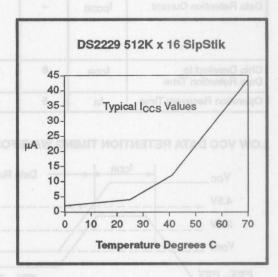


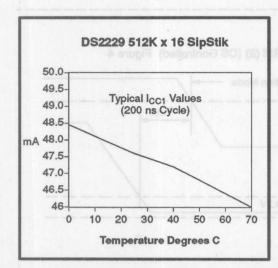
#### NOTES:

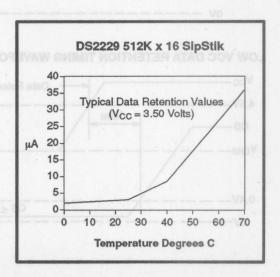
1. CS controls address buffer, WE buffer, CE0 – CE3 buffer and OE buffer and D<sub>IN</sub> buffer. If CS controls data retention mode, V<sub>IN</sub> levels (address, WE, OE, CE0 – CE3, I/O) can be in the high impedance state. If CE0 – CE3 controls data retention mode, CS must be CS ≥ V<sub>CC</sub> -0.2V or 0V ≤ CS ≤ 0.2V. The other input levels (address, WE, OE, I/O) can be in the high impedance state.

#### PRODUCT CHARACTERISTICS









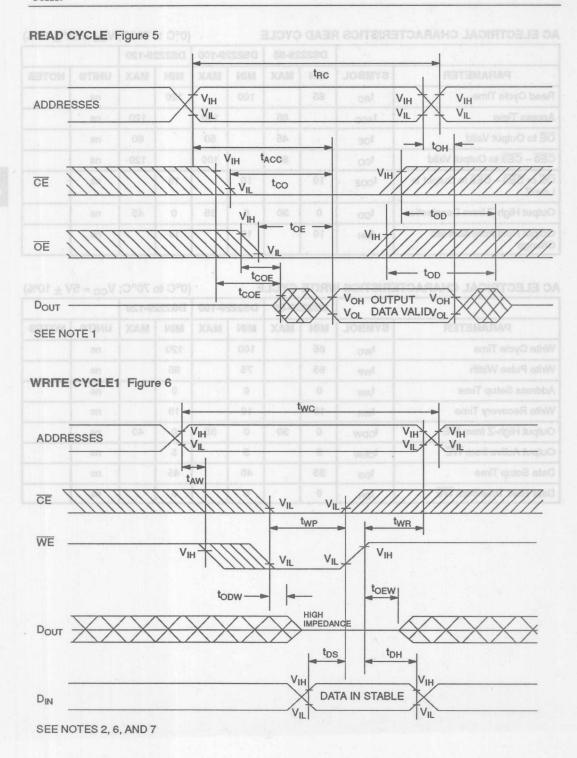
#### AC ELECTRICAL CHARACTERISTICS READ CYCLE

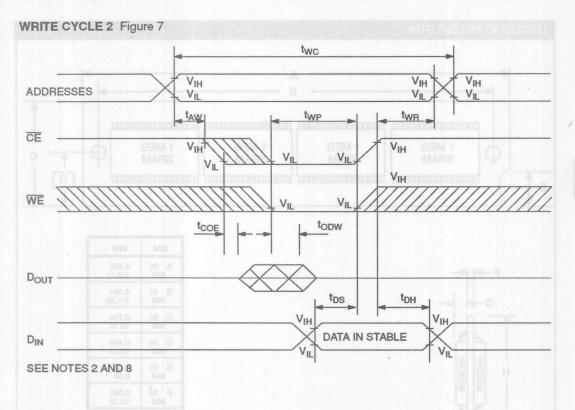
		DS22	29-85	DS22	29-100	DS22	29-120		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	85		100	FBV S	120		ns	negga
Access Time	tACC		85		100	1	120	ns	
OE to Output Valid	toE	L	45		50		60	ns	
CE0 - CE3 to Output Valid	tco		85	161	100		120	ns	
OE or CE0 - CE3 to Output In Low-Z	tcoe	10	001	10	4/1	10		ns	30
Output High-Z from Deselection	top	0	30	0	35	0	45	ns	
Output Hold from Address Change	фон	10	Di aV	10	1//	10		ns	30

#### AC ELECTRICAL CHARACTERISTICS WRITE CYCLE

- 1	O°C	to	700	C. V	1	_	5V	4	10%	12
- 1	0	CO	10	U. V	CC	-	JV	+	10%	5}

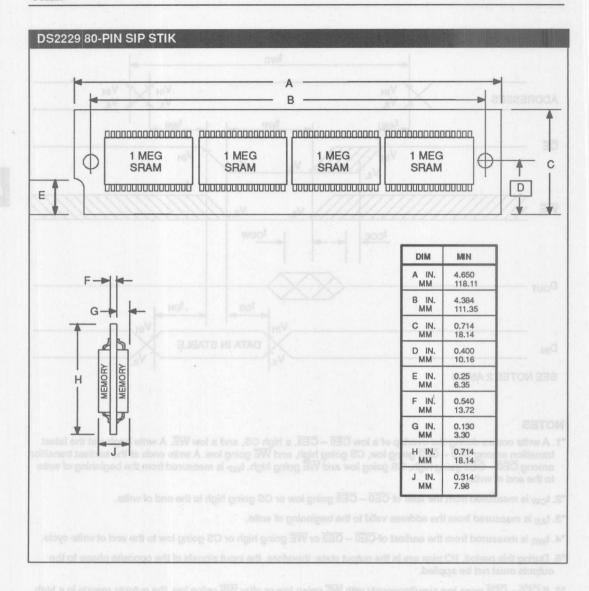
	AV ATAG MY	DS2229-85		DS2229-100		DS2229-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write Cycle Time	twc	85		100		120		ns	
Write Pulse Width	t <sub>WP</sub>	65		75		85		ns	
Address Setup Time	t <sub>AW</sub>	0		0		0	Maryle 1	ns	20 1 17 1 19
Write Recovery Time	t <sub>WR</sub>	10		10		15		ns	
Output High-Z from WE	topw	0	30	0	35	0	40	ns	BOOA
Output Active from WE	toew	5		5		5		ns	
Data Setup Time	t <sub>DS</sub>	35		40		45		ns	
Data Hold Time from WE	t <sub>DH</sub>	0		0	777	0	777	ns	7 38





#### **NOTES**

- \*1. A write occurs during the overlap of a low  $\overline{CE0} \overline{CE3}$ , a high CS, and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE0} \overline{CE3}$  going low, CS going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CE0} \overline{CE3}$  going high, CS going low and  $\overline{WE}$  going high. two is measured from the beginning of write to the end of write.
- \*2. t<sub>CW</sub> is measured from the later of CE0 CE3 going low or CS going high to the end of write.
- \*3. t<sub>AS</sub> is measured from the address valid to the beginning of write.
- \*4. t<sub>WR</sub> is measured from the earliest of CE0 CE3 or WE going high or CS going low to the end of write cycle.
- \*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
- \*6. If CEO CE3 goes low simultaneously with WE going low or after WE going low, the outputs remain in a high impedance state.
- \*7. If  $\overline{\text{CE0}} \overline{\text{CE3}}$  is low and CS is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
- \*8. This parameter is sampled and not 100% tested.
- \*9. This value is measured from CS going low to the end of write cycle.
- \*10. Only one CE active during any read or write cycle.



011592 10/10

# DALLAS

### DS2257, DS2257S 32K x 8 3V Operation Static RAM

EATURES	HGH-Z			PIN	ASSIC	BNM	ENT			
Low power	CMOS desi	gn			Н		0	<u>.</u>		
Standby cu	ırrent				A14	1	2			
					A12	2	2		WE	
		$^{\circ}$ C $V_{CC} = 3.5$			A7 🗆	3		6	A13 A8	
		$^{\circ}$ C $V_{CC} = 5.5$ $^{\circ}$ C $V_{CC} = 5.5$			A5 I	5	2	5	A9	
		$^{\circ}$ C $V_{CC} = 5.5$								
	1 0	56"C to 41259			A4	6	mons I	3	A11 OE	
Full operati	ion for V <sub>CC</sub> =	= 5.5V to 2.7V			A3   A2	8	1900 2			
Data Roter	ation Voltage	= 5.5V to 2.0	V		A1	9		0	CE	
Data Heter	ition voitage	- 0.04 to 2.0			AO H	10	blog	9 =	DQ7	
Access tim	e equals 70	ns at 5.0V and	150 ns at 2.7	/	DQ0	11		8		
Operating	tomporaturo	range of -40°	C to . 959C		DQ1	12		7	DQ5	
Operating i	temperature	Tarige or -40	0 10 +85-0		DQ2	13		6	DQ4	
Full static of	peration				GND [	14		5	DQ3	
		s and output	s over voltag	9	2	8 PIN [	DIP OR 28 PIN	SOIC	eens	
range of 5.	5V to 2.7 vo	lts.		DIN	DESC	PIP	TION			
Available in	28 pin DIP	and 28 pin SC	OIC packages			rur				
0 11 11 6			SAFYET A	AO-A	114		Address I Write Ena			
		y operate and	battery backu	OE			Output Éi			
application	S			CE			Chip Ena			
					-DQ7		Data Inpu			
				Vcc	I SUCKER	214				2.7V - 5.5V
				GNE		٧ -	Ground	1.1.3	geticV s	Former Suppl
				NC		7 -	No Conne	ectio	n open	

#### DESCRIPTION

The DS2257 is a 262,144 bit low power, fully static random access memory organized as 32768 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input  $(\overline{\text{CE}})$  is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applica-

tions. The device provides fast access time of 70 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 150 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7 to 5.5 volts. The DS2257 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required.

OPERATION MOD	OPERATION MODE										
MODE	CE	ŌĒ	WE	A0 - A14	DQ - DQ7	POWER					
READ	Opplant	ACTOX	NZ4H	STABLE	DATA OUT	Icco					
WRITE	L	X	L	STABLE	DATA IN	Icco					
DESELECT	L	Н	Н	X	HIGH-Z	Icco					
STANDBY	Н	Х	X	X	HIGH-Z	Iccs					

ABSOLUTE MAXIMU	M RATINGS	
SYMBOL	PARAMETER	RATING
V <sub>CC</sub>	Power Supply Voltage	-0.3V to +7.0V
V <sub>IN</sub> , V <sub>I/O</sub>	Input, Input/Output Voltage	-0.3 to +7.0V
T <sub>STG</sub>	Storage Temperature	-55°C to +125°C
TOPR DEA C 15	Operating Temperature	-40°C to +85°C
T <sub>SOLDER</sub>	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t <sub>A</sub> = 25°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Input Capacitance	CIN	90	dev 5 vo s	10	pF di	gmoo JTT				
Input/Output Capacitance	C <sub>VO</sub>	MIS .	5	10	pF	o to agris				

#### +5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t <sub>A</sub> = -40°C TO +85°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V					
Input High Voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	٧					
Input Low Voltage	V <sub>IL</sub>	-0.3		0.8	٧					
Data Retention Voltage	V <sub>DR</sub>	2.0		5.5	٧					

#### +5 VOLT OPERATION - CONTINUED

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	55 VIIL	$0V \le V_{IN} \le V_{CC}$	/	±0.1	μА	dgil-l tuq
I/O Leakage Current	ILO	CE=VIH, 0V≤VIO≤VCC		±0.5	μА	Wo.J tug
Output High Current	Іон	V <sub>OH</sub> = 2.4V	-1.0	(9)	mA	ata Rete
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0		mA	
Standby Current	I <sub>CCS1</sub>	<u>CE</u> = 2.2V	01 /	1.0	mA	AHO O
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =85°C	SYMBO	10	μА	TEMARA
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =60°C		4	μА	iput Leak
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =25°C	ou!	500	nA	ps/sel/ O
Operating Current	Icco	CE=0.8V min cycle	HO	60	mA	al-i sugto

PARAMETER	SYMBOL	DS2257-70 DS2257S-70		UNITS	NOTES
	D908=A2 V8.0-00.V	MIN	MAX		emuo yabn
Read Cycle Time	t <sub>RC</sub>	70	1800	ns	BHIAN YOUN
Access Time	tACC	10	70	ns	kun-s dustese
OE to Output Valid	t <sub>OE</sub>		35	ns	un inue
CE to Output Valid	tco	Marie M	70	ns	
OE or CE to Output Active	tcoe	5		ns	5
Output High Z from Deselection	t <sub>OD</sub>	Un	25	ns	5
Output Hold from Address Change	tон	5		ns	Manual Con-
Write Cycle Time	twc	70		ns	
Write Pulse Width	t <sub>WP</sub>	55		ns	3
Address Setup Time	t <sub>AW</sub>	0		ns	
Write Recovery Time	t <sub>WR</sub>	10		ns	
Output High Z from WE	topw	, AL	25	ns	5
Output Active from WE	toew	5		ns	5
Data Setup Time	t <sub>DS</sub>	30		ns	4
Data Hold Time	t <sub>DH</sub>	10		ns	4

#### +3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t <sub>A</sub> = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	2.7	3.0	3.5	V	DTBMARA
Input High Voltage	V <sub>IH</sub>	2.0	10	V <sub>CC</sub> + 0.3	ine <b>V</b> O e	out Leaka
Input Low Voltage	V <sub>IL</sub>	-0.3	/=35	0.6	V	apulsa.J 3
Data Retention Voltage	V <sub>DR</sub>	2.0		3.5	V	rigiH Juqtu

DC CHARACTERISTICS (	t <sub>A</sub> = -40°C <sup>-</sup>	TO +85°C, V <sub>CC</sub> = 2.7V T	O 3.5V)			
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	loosa	±0.1	μА	Handby C
I/O Leakage Current	ILO	CE=V <sub>IH</sub> , 0V≤V <sub>IO</sub> ≤V <sub>CC</sub>	10032	±0.5	μА	D yelbrati
Output High Current	Іон	V <sub>OH</sub> = 2.2V	-0.5		mA	antistic qu
Output Low Current	loL	V <sub>OL</sub> = 0.4V	4.0		mA	
Standby Current	I <sub>CCS1</sub>	CE = 2.0V	7 0 01	0.5	mA	
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> - 0.3V t <sub>A</sub> =85°C		4	μА	
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =60°C		1	μА	-1815-8-197
Standby Current	I <sub>CCS2</sub>	CE≥V <sub>CC</sub> -0.3V t <sub>A</sub> =25°C		400	nA	hu'il bend
Operating Current	Icco	CE=0.6V min cycle		40	mA	T sames

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	150			ns	
Access Time	tACC	1 00		150	ns	The second
OE to Output Valid	toE	HO		75	ns	NOT LINCOLD
CE to Output Valid	tco	OW		150	ns	and and
CE or OE to Output Active	tcoe	5			ns	060 100
Output High-Z from Deselection	top	9,000		75	ns	70 200 100
Output Hold from Address Change	tон	15			ns	laifi tustu

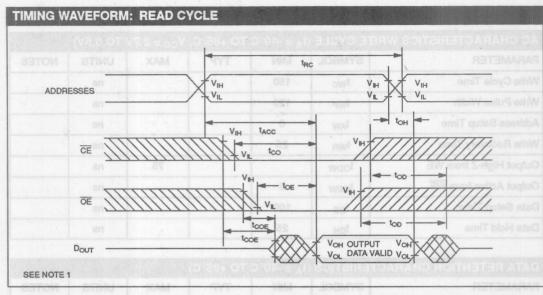
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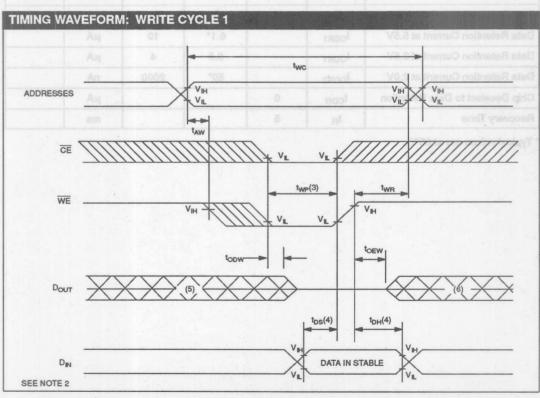
#### +3 VOLT OPERATION - CONTINUED

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	twc	150	HV		ns	innas.
Write Pulse Width	t <sub>WP</sub>	120			ns	
Address Setup Time	t <sub>AW</sub>	0	wV S		ns	
Write Recovery Time	t <sub>WR</sub>	25	: 1777		ns	
Output High-Z from WE	topw			75	ns	
Output Active from WE	toew	5	1	77777	ns	
Data Setup Time	t <sub>DS</sub>	100	4411		ns	
Data Hold Time	t <sub>DH</sub>	25			ns	

DATA RETENTION CHARACTERISTICS (t <sub>A</sub> = -40°C TO +85°C)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Data Retention Supply Voltage	V <sub>DR</sub>	2.0		5.5	1910 V = 1/A	7 SMM	
Data Retention Current at 5.5V	Iccn1		0.1*	10	μА		
Data Retention Current at 3.5V	IccR1		0.5	4	μА		
Data Retention Current at 2.0V	I <sub>CCR2</sub>		50*	2000	nA		
Chip Deselect to Data Retention	tcdr	0		K	μА	BREADUA	
Recovery Time	t <sub>R</sub>	5	140-05		ms		

<sup>\*</sup> Typical values are at 25°C

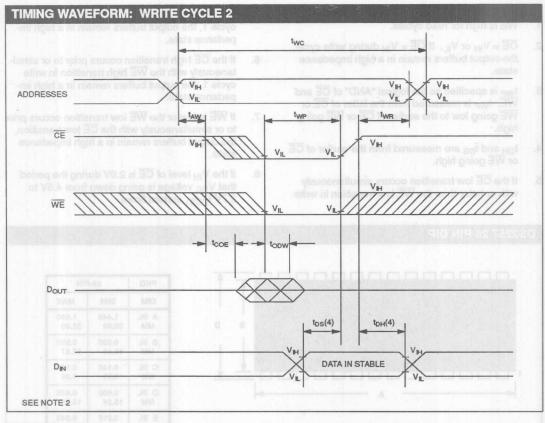




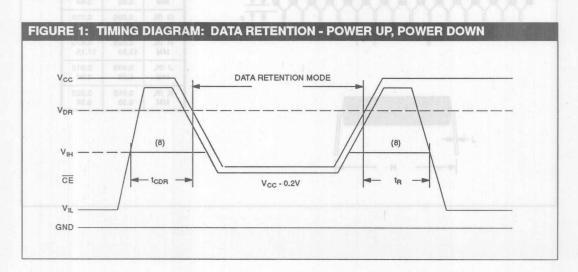
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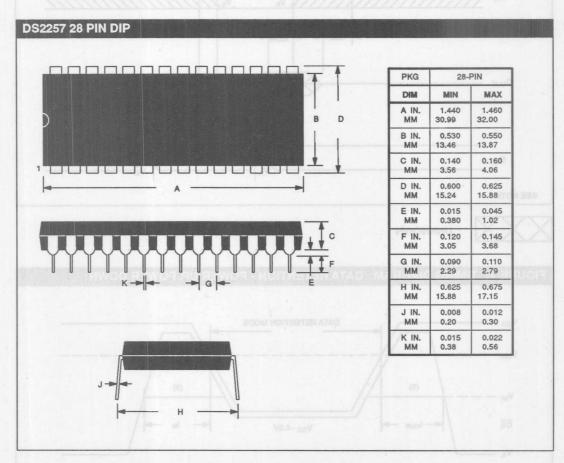




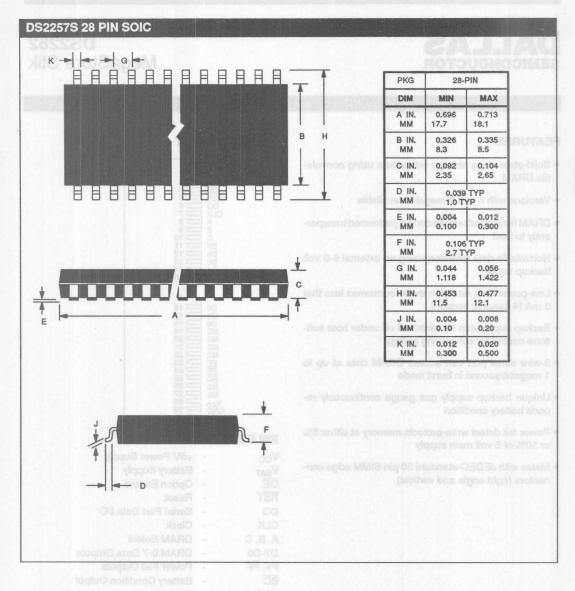
#### NOTES

- 1. WE is high for read cycles.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical "AND" of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- t<sub>DH</sub> and t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- If the CE low transition occurs simultaneously with or latter than the WE low transition in write

- cycle 1, the output buffers remain in a high impedance state.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in write cycle 1, the output buffers remain in a high impedance state.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state.
- If the V<sub>IH</sub> level of CE is 2.0V during the period that V<sub>CC</sub> voltage is going down from 4.5V to 2.7V I<sub>CCS1</sub> current flows.







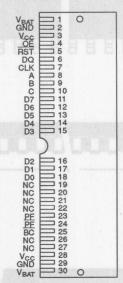


DS2262 MegaStore Stik

#### **FEATURES**

- Solid-state mass storage subsystem using nonvolatile DRAM
- Versions with 4 and 8 megabits available
- DRAM timing and refresh control performed transparently to host
- Nonvolatile data retention using an external 6-9 volt backup supply
- Low-power data retention mode consumes less that 3 mA (4 megabit version)
- Backup supply can be switched off under host software control for conserving energy
- 3-wire serial port can access DRAM data at up to 1 megabit/second in burst mode
- Unique backup supply gas gauge continuously reports battery condition
- Power fail detect write-protects memory at either 5% or 10% of 5 volt main supply
- Mates with JEDEC-standard 30 pin SIMM edge connectors (right angle and vertical)

#### **PIN ASSIGNMENT**



#### **PIN DESCRIPTION**

Vcc	_	+5V Power Supp
VBAT	-	Battery Supply
OE	-	Option Enable
RST	-	Reset

DQ - Serial Port Data I/O

CLK - Clock A, B, C - DRAM Select

D7-D0 - DRAM 0-7 Data Outputs
PF, PF - Power Fail Outputs

BC - Battery Condition Output

GND - Ground

#### DESCRIPTION

The DS2262 MegaStore Stik is an extremely compact solid-state mass storage device that provides up to 8 megabits of nonvolatile DRAM for data storage. The DRAM and internal control functions are accessed using a 3-wire serial interface (CLK, D/Q, RST) which can hook directly to the serial port of popular microprocessor/microcontroller devices such as the DS5000T/2250T Time Microcontroller family. All nec-

essary DRAM timing and refresh duties are performed automatically.

An external backup supply such as a 6-volt battery can be attached to enable DRAM data retention, creating in effect a solid state disk drive. An internal circuit monitors the main +5V supply. Upon its failure, the DRAM is write-protected and the backup supply switched on. With an inexpensive 1300 mA/Hr lithium battery, a DS2262 with 4 megabits can provide up to 3 weeks of continuous nonvolatile operation. If the failure of the main supply is relatively infrequent, the DS2262 can extend its nonvolatile operation for years, especially if the backup source is a rechargeable battery. A unique gas gauge circuit continuously monitors and reports the backup supply condition, warning the host of impending battery failure.

#### **OPERATION - OE (PIN 4) HIGH**

The main elements of the DS2262 are shown in Figure 1. Six signals control sending or retrieval of data using the address converter circuit. The signals CLK, RST, and DQ comprise the DS2262 serial port. The signals A, B, and C control which DRAM data is written to. To transfer data into the DS2262, RST is first driven high while CLK is low. After sufficient setup time from RST, one bit of data is placed onto the DQ line. With valid data on DQ, the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred to the DS2262. If data is to be written to or read from one of the DRAMs, that DRAM must be selected on the A, B, and C pins when RST is brought high, and must remain selected until RST is brought low again to reset the serial port (see Table 2).

Information is written to the serial port in the form of a 24 bit address field followed by an 8 bit function code. 24 address bits are required regardless of the density of Stick used. Function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from a DRAM or the control registers. Data is read from the control registers by driving CLK low while RST is high. Data becomes valid on the DQ line after sufficient time is allowed for access. Reading from a DRAM selected by the A, B and C pins will place the correct data on the corresponding data line (D0-D7) after time is allowed for access, as well as on the DQ line. A read cycle is terminated when RST is returned low.

#### OPERATION - OE (PIN 4) LOW

When the  $\overline{OE}$  pin is tied low, the A, B and C pins are replaced with a serial interface controlled by  $\overline{RST}$ , CLK, and DQ. To load the DRAM to be written, the  $\overline{RST}$  pin is brought low and the DRAM select signals are clocked in, in the order C, B then A on DQ on the rising edge of the CLK pin.  $\overline{RST}$  is then brought high to enable the entry of addresses and function codes into the control registers as described above. When the DS2262 is to be used with the  $\overline{OE}$  pin low, the A, B and C pins should be left unconnected.

#### **BURST MODE**

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst

write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. Burst mode is terminated when RST is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers.

# OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt V<sub>CCI</sub> power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V<sub>CCI</sub> falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF,PF) are driven active at this time and will remain active until Vccı is restored to a normal condition. When the data retention mode begins, the DS2262 isolates the 3-wire serial port. If an active DRAM read/write cycle is in progress when power loss occurs, the DS2262 will complete this cycle properly before isolating the 3-wire serial port (RST. CLK, D/Q). The V<sub>CCI</sub> input is then disconnected from the V<sub>CCO</sub> output and the backup supply connected to the V<sub>BAT</sub> pin is switched in. The V<sub>BAT</sub> input is normally connected to either a rechargeable battery or super capacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be tied to the V<sub>CCI</sub>pin; do not tie this pin low when not using the battery-backup function.

#### **BATTERY GAS GAUGE**

The DS2262 contains two features that provide information about the condition of the backup supply. First, the DS2262 monitors the backup supply input condition. If this input is below  $V_{\rm CCl}$  the backup condition output pin  $(\overline{\rm BC})$  is driven active low and remains in this state until the backup supply voltage is restored to a level above  $V_{\rm CCl}$ . This feature is active only while  $V_{\rm CCl}$  is applied within nominal limits. Whenever the backup supply is providing power, the  $\overline{\rm BC}$  pin remains in a high impedance state.

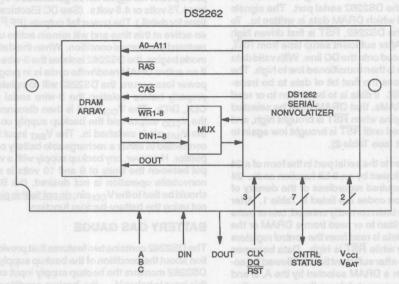
The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while V<sub>CCI</sub> is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field, followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field followed by the correct function code. Information in the address field is automatically entered into the battery condition counter when RST is brought low to end the

cycle. The battery condition counter value can only be entered when  $V_{\text{CCI}}$  is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V<sub>CCI</sub> is within normal limits. No other action will take

place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply will be discharged. When the counter reaches zero, the  $\overline{\rm BC}$  pin will be driven low as soon as  $V_{\rm CCI}$  is within normal limits. The  $\overline{\rm BC}$  pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

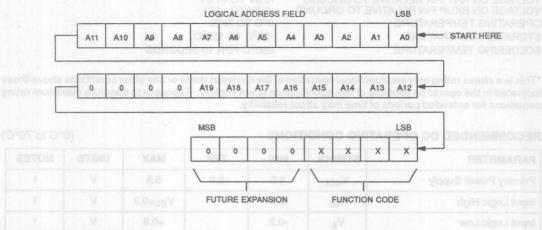
#### **FUNCTIONAL DIAGRAM** Figure 1



#### **DRAM SELECTION Table 1**

	INPUTS		DRAM SELECTED
A	B .eisis e	C	DRAM SELECTED
noo ed o madinar	rol amin o brooss	0	0
atribnodaz i isbe	nemeroel 0 feet retre	0 000	ie DRAM telectelgnet are
0	dmsm s cal w besilation	0	e mod moe 2 medi si
e of the oquitter is	omal limits. The value	0	3
oltonial Outribinoo	red by a 0 rite batter	lol thorisa	pin low, 4 e4, 8 and 0 pin
no acu ere ruiw obbs erb to SCM	0	of 1	5
molal o co noto	nd to more one of the	vol 1	6
is bringht lov	dition cou <b>h</b> ter when	or but to	beer triud MA70 on mo

#### **SERIAL PORT PROTOCOL Figure 2**



#### FUNCTION CODES Table 2

FUNCTION NAME	FUNCTION CODE (HEX)		
BURST READ DRAM DATA READ DRAM DATA	MIN	IOBINYS	00 01 RETEMARA
READ BKUP COUNTER WRITE BKUP COUNTER	-1.0	13	02 03
BACKUP SUPPLY ENABLED BACKUP SUPPLY DISABLED	0.14	но	OC OD 2 O treated butter
WRITE DRAM DATA BURST WRITE DRAM DATA	2.0	101	OE OF MANUS MIGHT

 PARAMETER
 SYMBOL
 MIN
 TYP
 MAX
 UNITS
 NOTES

 Imput Capacitance
 C<sub>IN</sub>
 C<sub>A</sub>=28°C
 5
 7
 pF

 Output Capacitance
 Court
 C<sub>A</sub>=28°C
 7
 10
 pF

 VO Capacitance
 C<sub>VO</sub>
 C<sub>A</sub>=28°C
 7
 10
 pF

#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND VOLTAGE ON BKUP PIN RELATIVE TO GROUND

OPERATING TEMPERATURE STORAGE TEMPERATURE

SOLDERING TEMPERATURE

-0.3V TO +7.0V -0.3V TO +12V 0°C TO 70°C -55°C TO 125°C

260°C FOR 10 SECONDS

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Input Logic High	OO WOOD VIH	2.0	a anunun	V <sub>CC</sub> +0.3	V	1
Input Logic Low	V <sub>IL</sub>	-0.3		+0.8	V	1
Backup Supply	V <sub>BAT</sub>	5.5	8.0	10.0	V	1,2

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CCI</sub>=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage SO	I <sub>IL</sub>	-1.0		+1.0	оч µА	BR .
DQ Leakage	ILO	-1.0		+1.0	μА	100
Output Current @ 2.4V	Іон	-1.0	d	LY DISABILE	mA	AS
Output Current @ 0.4V	loL	2.0		ATA	mA	W.
Input Supply Current	Icci		3.0	7.0	mA	D8
TOL Pin = V <sub>CCO</sub>	V <sub>TP</sub>	4.50	4.62	4.75	V	
TOL Pin = GND	T <sub>TP</sub>	4.25	4.37	4.50	V	
Backup Supply Leakage	I <sub>BKUPL</sub>		2	4	μА	
Backup Supply Quiescent	I <sub>BKUPQ</sub>		2.0		MA	

#### CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	t <sub>A</sub> =25°C	5	7	pF	
Output Capacitance	C <sub>OUT</sub>	t <sub>A</sub> =25°C	7	10	pF	
I/O Capacitance	C <sub>VO</sub>	t <sub>A</sub> =25°C	7	10	pF	

<sup>\*</sup>This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

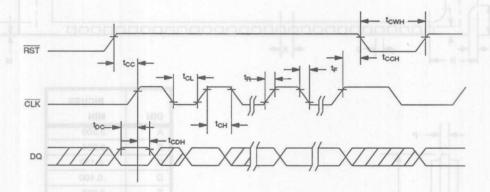
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#### AC ELECTRICAL CHARACTERISTICS

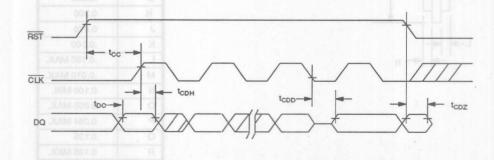
 $(t_A=25^{\circ}C, V_{CC}=5V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DQ to CLK Setup	t <sub>DC</sub>	100	okup supply	its and the br	ns	is within
CLK to DQ Delay	tcdd			200	ns	/ WOISO
CLK Low Time	t <sub>CL</sub>	500		High	ns	Load ca
CLK High Time	as V or to to to	500	E HIN - 100	puis upert,	ns	W.
CLK Frequency	tclk	DC	rnal switchin	otni eril eriori	MHz	V <sub>TP</sub> is to
CLK Rise and Fall	t <sub>R</sub> , t <sub>F</sub>	3	10	20	ns	circuits o
RST to CLK Setup	tcc	1			μs	
CLK to RST Hold	tссн	200		STILK	ns	2252 14
RST Inactive Time	tcwH	1-4-			μѕ	
RST to DQ in High Z	t <sub>CDZ</sub>	8		100	ns	40 -

### WRITE DATA TRANSFER FROM SERIAL PORT



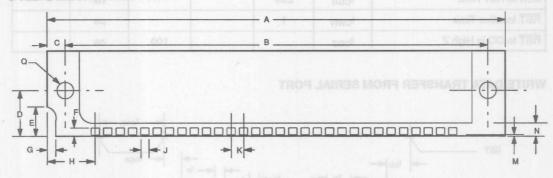
#### **READ DATA TRANSFER FROM SERIAL PORT**

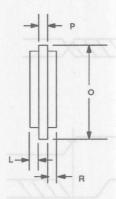


#### NOTES

- 1. All voltages are referenced to ground.
- The BC pin will be driven active whenever V<sub>CCI</sub> is within nominal limits and the backup supply is below V<sub>CCI</sub>.
- 3. Load capacity is 100 pF.
- Measured with all outputs open, V<sub>CCI</sub> = V<sub>IH</sub> = 5.5
   V.
- V<sub>TP</sub> is the trip point where the internal switching circuits disconnects V<sub>CCI</sub> and connects the internally regulated backup supply to the DRAMs.
- Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS2262 is in the data retention mode (V<sub>CCI</sub>=0V).
- Backup quiescent current is the current consumed by the DS2262 when in the data retention mode and the backup supply is enabled. Total current into the V<sub>BAT</sub> pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

#### **DS2262 MEGASTORE STIK**



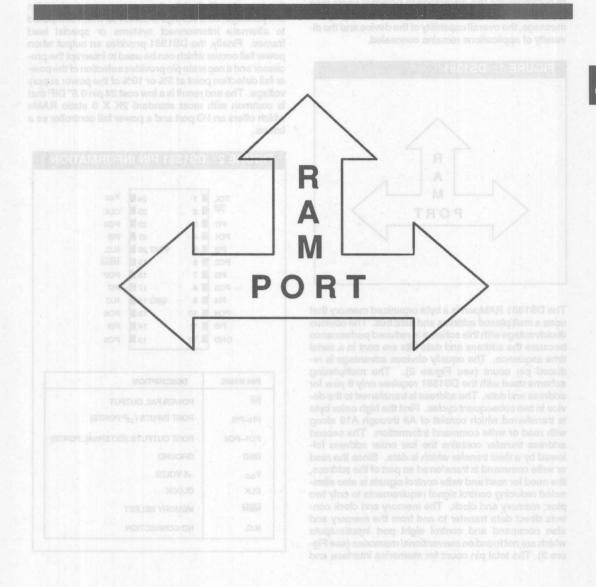


DIM	INCHES
William Control of the Control of th	
A	3.500
В	3.234
C	.0.133
D	.0.400
E	0.250
FMOR	0.070 MIN.
G	.0.080
Н	0.300
J	0.070
K	.0.100
L	.0.185 MAX.
М	.0.010 MAX.
N	0.100 MIN.
0	0.855 MAX.
P	0.054 MAX.
Q	0.125
R	0.185 MAX.

# DALLAS

## RAMport Application Note – 61

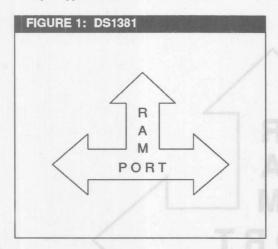
RAMBORT -- 2K X 8 NV SRAMAND MORE



4

### RAMport - 2K X 8 NV SRAM AND MORE

The RAMport memory developed by Dallas Semiconductor was designed to be connected to microcontrollers without robbing the device of valuable port pins. The name "RAMport" was chosen for the DS1381 to try to communicate this advantage to potential users (see Figure 1). Even if the name is effective in conveying this message, the overall capability of the device and the diversity of applications remains concealed.

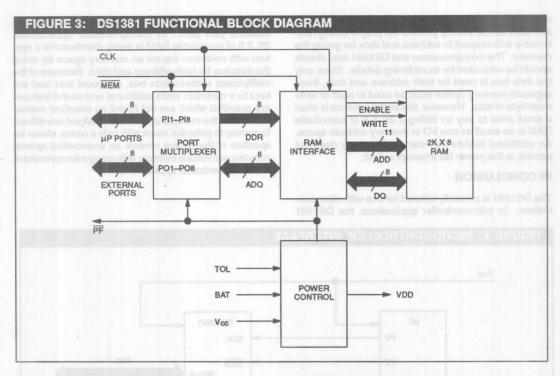


The DS1381 RAMport is a byte organized memory that uses a multiplexed address and data bus. The obvious disadvantage with this scheme is reduced performance because the address and data bits are sent in a serial time sequence. The equally obvious advantage is reduced pin count (see Figure 2). The multiplexing scheme used with the DS1381 requires only 8 pins for address and data. The address is transferred to the device in two subsequent cycles. First the high order byte is transferred which consist of A8 through A10 along with read or write command information. The second address transfer contains the low order address followed by a third transfer which is data. Since the read or write command is transferred as part of the address, the need for read and write control signals is also eliminated reducing control signal requirements to only two pins; memory and clock. The memory and clock controls direct data transfer to and from the memory and also command and control eight port input/outputs which are not found on conventional memories (see Figure 3). The total pin count for memories interface and

port input/output plus V<sub>CC</sub> and ground amounts to 20 pins. This leaves four pins for the special purpose of providing nonvolatility. Two pins provide for a direct connection to a data retention energy cell. These pins do not go outside the package, but are internally connected to a button style energy cell. Since this connection is made with 2 of the 24 pins on a standard dual in line package, cost savings is achieved when compared to alternate interconnect systems or special lead frames. Finally, the DS1381 provides an output when power fail occurs which can be used to interrupt the processor and a separate pin provides selection of the power fail detection point at 5% or 10% of the power supply voltage. The end result is a low cost 24 pin 0.6" DIP that is common with most standard 2K X 8 static RAMs which offers an I/O port and a power fail controller as a

#### FIGURE 2: DS1381 PIN INFORMATION Vcc TOL 1 24 PF 23 CLK Pl1 3 22 PO8 PO1 4 21 PI8 PI2 5 VBAT 20 N.C. MEN P02 19 PI3 18 P07 PO3 8 17 PI7 PI4 9 GND 16 N.C PO4 10 PO6 15 PI5 11 14 PI6 GND 12 13 PO5

PIN NAME	DESCRIPTION
PF	POWER FAIL OUTPUT
PI1-PI8	PORT INPUTS (µP PORTS)
PO1-PO8	PORT OUTPUTS (EXTERNAL PORTS)
GND	GROUND
V <sub>CC</sub>	+5 VOLTS
CLK	CLOCK
MEM	MEMORY SELECT
N.C.	NO CONNECTION



# REDUCING TO PRACTICAL – MICROCONTROLLER INTERFACE

As mentioned, the DS1381 was designed to offer the microcontroller user some external nonvolatile memory that does not consume all of the valuable port pins. When using the DS1381 with a microcontroller, the interconnect system is simple and straight forward. Eight port pins of the microcontroller connect directly to the eight input port pins (PI1 - PI8) of the DS1381 (see Figure 3). These port pins are reproduced at the port output pins (PO1 - PO8). During operation when no memory transfer is taking place, the DS1381 port output pins look exactly like the eight microprocessor port pins with the only addition of a small series impedance. Two other port pins of the microprocessor are required to control the DS1381; namely CLOCK and MEMORY. Since these port pins must be dedicated to control, they are not reproduced the the DS1381. The MEMORY and CLOCK signals must be generated using software within the microcontroller to establish the proper signal levels and timing relationships. The function of these two controls is to direct data to and from memory or to the data direction register within the DS1381. When data is being transferred to and from the DS1381, the port outputs are latched or become high impedance depending on their assigned function. More detailed information on the control signals is furnished in the DS1381 data sheet.

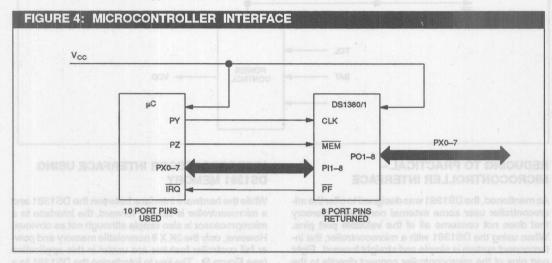
# MICROPROCESSOR INTERFACE USING DS1381 MEMORY

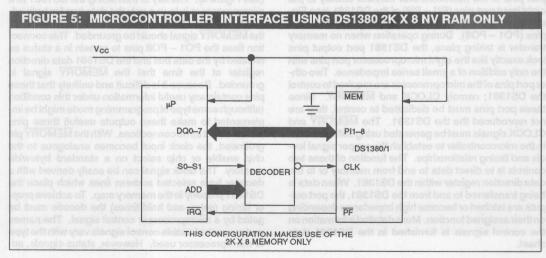
While the hardware interface between the DS1381 and a microcontroller is straight forward, the interface to a microprocessor is also simple although not as obvious. However, only the 2K X 8 nonvolatile memory and power fail controller features are useful in this application (see Figure 5). The key to interfacing the DS1381 to a microprocessor is to use only the data bus for both address and data. Since only the memory is to be used, the MEMORY signal should be grounded. This connection fixes the PO1 - PO8 pins to remain in a status as dictated by the data bus and the DS1381 data direction register at the time that the MEMORY signal is grounded. Because it is difficult and unlikely that these pins contain any useful information under this condition (although some type of programming mode might be implemented to make these outputs useful) these pins should be left as no connections. With the MEMORY pin grounded, the clock input becomes analogous to the chip enable or chip select on a standard bytewide memory. The clock signal can be easily derived with a decoder from selected address lines which place the DS1381 properly in the memory map. To achieve proper timing (setup and hold times) the decode must be gated by a microprocessor control signal. The names and purpose of usable control signals vary with the type of microprocessor used. However, status signals, address latch enable, memory request, address strobe, and data strobe usually provide the proper timing relationship with respect to address and data for gating the decoder. The microprocessor and DS1381 data sheets should be consulted for exact timing details. Since only the data bus is used for both address and data, three separate memory cycles must be used to read or write each byte of data. However, this inconvenience is often a small price to pay for hiding a 2K X 8 of nonvolatile RAM in as small as one I/O or memory address space. An additional feature that standard memory does not provide is the power fail interrupt output.

#### IN CONCLUSION

The DS1381 is primarily tailored for use with microcontrollers. In microcontroller applications, the DS1381

provides an inexpensive nonvolatile RAM without using valuable port pins. In microprocessor applications, 2K X 8 of nonvolatile RAM is easily interfaced to a system with minimum impact on memory space by using the data bus for both address and data. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while additional and useful features are provided which are not found on standard memories. While the multiple uses of the RAMport are difficult to convey to potential users with only a name; closer inspection of the device reveals an economical special purpose nonvolatile memory with many microprocessor and microcontroller applications.





# 4

# Using Nonvolatile Static RAMs Application Note – 63



#### MONARDA DIN GOOM

larry types of memories have been devised to meet vaying application needs. However, norwolatile read/ write random access memories can be substituted for write random types independent of application, if cost is

DRAM: Dynamic Random Access Memory. A DRAM, similar to an SRAM, stores information as a 1 or a 0. In an SRAM, this information is stored in a four to six translation file-flop which is easy to address, but requires a store tile-flop which is easy to address, but requires a stores list 1 or 0 as a charge on a small capacitor, requiring much more current then an SRAM to maintain the stored data. The not memory cell size is smaller for the DRAM than for the SRAM, so the total cost per bit of memory is less. The DRAM's capacitors must be constraintly refreshed so that they retain their charge, and require more so this interface shoulder.

SRAM. Static Random Access Memory. An SRAM is seentially a stable DC flip-flop requiring no clock time or refreshing. The contents of an SRAM type namory are relained so long as power is supplied, and support extremely fast access times. SRAMs also have relatively few shirt timing requirements and a parallel

NV SRAM: An NV SRAM is a single package which contains a low current SRAM, a memory controller capable of measuring voltage, and a lithium type battery. When the power supply to this single modular package which shalls below the minimum requirement to maintain the contents of the SRAM, the memory controller in the contents of the SRAM, the memory controller in the source to the internal lithium battery, and write protects the SRAM. These transparent to the SRAM, transform power source are transparent to the SRAM, transforming it into a true non-volatile memory. This unique content is true to combines the strategic advantages of SRAM, addition combines the strategic advantages of SRAM. PROM technologies. Battery backed SRAM modules from Daltas Seniconductor are pin-to-pin compatible from battery backed SRAM, making them ideal for

091191 1/11

Vast resources have been expended by the semiconductor industry trying to build a nonvolatile random access read/write memory. The effort has been undertaken because nonvolatile RAM offers several advantages over other memory devices – DRAM, Static RAM, Shadow RAM, EEPROM, EPROM and ROM – which were developed to meet specific applications needs.

Characteristics of the ideal nonvolatile RAM are: low power consumption, higher performance, greater reli-

ability, higher density, low cost, and the ability to be used in any semiconductor memory application.

While the various memory components designed to date do not meet the ideal memory scenario, each excels in meeting one or more of the sought after attributes (Figure 1).

	COST	EASE OF INTERFACE	NONVOLATILE	DENSITY	PERFORMANCE	READ/WRITE	DATA RETENTION
DRAM	+++			+++	++	+++	
STATIC RAM		+++		+	+++	+++	
NV SRAM		+++	++	+	+++	+++	++
PARTITIONABLE NV SRAM		+++	++	+	+++	+++	++
PSEUDO STATIC	+	+		++	+	+++	
FLASH	++	++	++	+	++	+	++
EEPROM	+	++	+	+		+	+
EPROM	++	++	++	++	+		++
OTP EPROM	+++	+++	+++	+++	+		+++
ROM	+++	***	+++	+++	+		+++

+ = Degree of excellence

#### TYPES OF MEMORY

Many types of memories have been devised to meet varying application needs. However, nonvolatile read/write random access memories can be substituted for all memory types independent of application, if cost is not a primary consideration.

DRAM: Dynamic Random Access Memory. A DRAM, similar to an SRAM, stores information as a 1 or a 0. In an SRAM, this information is stored in a four to six transistor flip—flop which is easy to address, but requires a relatively large memory cell. A DRAM, by comparison, stores its 1 or 0 as a charge on a small capacitor, requiring much more current then an SRAM to maintain the stored data. The net memory cell size is smaller for the DRAM than for the SRAM, so the total cost per bit of memory is less. The DRAM's capacitors must be constantly refreshed so that they retain their charge, and require more sophisticated interface circuitry.

SRAM: Static Random Access Memory. An SRAM is essentially a stable DC flip-flop requiring no clock timing or refreshing. The contents of an SRAM type memory are retained so long as power is supplied, and support extremely fast access times. SRAMs also have relatively few strict timing requirements and a parallel address structure, making them particularly suited for

cache and other low density, frequent access applica-

NV SRAM: An NV SRAM is a single package which contains a low current SRAM, a memory controller capable of measuring voltage, and a lithium type battery. When the power supply to this single modular package falls below the minimum requirement to maintain the contents of the SRAM, the memory controller in the module switches the power supply from the external source to the internal lithium battery, and write protects the SRAM. These transitions to and from the external power source are transparent to the SRAM, transforming it into a true non-volatile memory. This unique construction combines the strategic advantages of SRAMaddressing structure, high speed access, and timing requirements, with the non-volatility advantages of EE-PROM technologies. Battery backed SRAM modules from Dallas Semiconductor are pin-to-pin compatible with non battery backed SRAMs, making them ideal for any application where a traditional SRAM would be suitable.

PARTITIONABLE NV SRAM: A partitionable Dallas Semiconductor NV SRAM offers the same nonvolatility, addressing structure, and timing requirements of a reg-

4

ular Dallas Semiconductor NV SRAM product with the additional feature of the ability to write protect selected blocks of memory, regardless of V<sub>CC</sub>.

The write protection feature requires no additional pins, and is instead controlled by a unique combination of addressing and read cycles (see DS1630 and DS1645 data sheets). This feature allows a designer to use a battery backed SRAM as both a RAM and a ROM – in one device. Because no additional pins are required for control, partitionable devices can be substituted for non–partitionables in existing designs, without making costly hardware changes.

PSEUDO STATIC RAM: Pseudo Static Random Access Memory. The advantages of using a Static Ram are the simplicity of the interface circuitry required, and the fact that the device is by nature "static", not requiring periodic refreshing to retain its data. A DRAM, however, provides lower cost per bit advantages and a higher memory density. A Pseudo static RAM combines the advantages of the SRAM and DRAM by using dynamic storage cells to retain memory, and by placing all the required refresh logic on—chip so that the device functions similarly to an SRAM.

FLASH: A flash memory combines the electrical erase capability of the EEPROM in a cell that is similar to an EPROM. The result is that the modified cell may be block erased electrically instead of with UV light. This feature allows a Flash memory to accept new code updates or information while it is functioning in a system.

EEPROM: Electrically Erasable/Programmable Read Only Memory. A significant disadvantage of the EPROM is the fact that it cannot be reprogrammed while in a circuit. The EPROM requires the external programming device to receive new code or data. An EEPROM eliminates this problem by providing a write function which can be used while the EEPROM is still in a circuit. A penalty of obtaining the write function while the EE-PROM is still in a circuit is having to provide a high voltage (12.5V or above) source for the EEPROM to source when accepting new code, or buying a more expensive EEPROM which has a charge pump in its package that allows the EEPROM to be used with a standard 5->7V input. Although nonvolatile, EEPROM memory cells exhibit slow read/write access rates, making them most suitable for systems where performance is not an issue. The other read/write capable memories listed in Figure 1 provide the ability to frequently read and write data continuously over their entire lifetimes, in excess of 10 years, while EEPROM memory cells can rarely be rewritten more than 10,000 times—you could wear out the EEPROM memory in less than a second! An EEPROM can be placed in a system and accessed as a standard RAM.

EPROM: Electrically Programmable Read Only Memory. An EPROM is a nonvolatile memory source which offers flexibility to both program and erase the contents of the memory multiple times. An EPROM

must be programmed using a 12.5 voltage or above PROM programmer, and then transferred into the system in which it is intended to function. EPROMs can be erased by shining ultraviolet light into the window in the top of the IC package. The process of writing data into an EPROM and then erasing it may be repeated almost indefinitely. EPROMs are usually used for product development, and later replaced with less expensive one—time programmable EPROMS.

OTP EPROM: One Time Programmable EPROM. An EPROM which can only be written with code/data once instead of multiple times. Generally, OTP EPROMs are less expensive then erasable EPROMs.

ROM: Mask Programmable Read Only Memory. Mask programmable ROM's are the most durable form of memory storage. They are, however, "read only" and offer fairly slow performance. If a design has code/data that is very stable and will not need to be changed, a custom mask for the IC die can be made which will significantly reduce the cost of the ROM. A drawback to using a masked ROM is the significant cost penalty that must be incurred if an error in the code/data being stored forces a mask set change. The OTP EPROM fills the gap between ROM applications (no changes) and EPROMs (frequent changes).

#### **MEETING APPLICATIONS NEEDS**

NMOS DRAM memory provides performance and density, but, on the down side, must be constantly refreshed to retain data. At the opposite extreme are ROMs, offering nonvolatility and density, but lacking the ability to be updated with new data because information is burned in only once. Between these two are a wide range of devices that fulfill some characteristics of the ideal memory.

Two popular devices, EEPROMs and Shadow RAMs, are designed to emulate a static RAM but also have the ability to retain data after a power loss. But despite their capability to retain data, both EEPROMs and Shadow RAMs fall short of meeting the industry's needs for several reasons.

Most notably, the EEPROM requires a special slow write cycle. The EEPROM's inability to support standard write cycle hinders performance in applications where memory is updated immediately as new data is available.

Another problem with EEPROMs is their wear out mechanisms. These raise reliability concerns due to the limited number of write cycles allowed – sometimes as few as 10,000. If a static RAM with a 200 ns cycle time had this limitation, it would wear out in a mere 20 ms. An application that requires constant updating, such as the buffer memory of a cashier's checkout terminal or a printer, the EEPROM's wear out mechanism is not acceptable.

Finally, because of the complexity of programming circuits, the cell structure and the special process technology required, the density of EEPROMs has not kept up with industry demands.

In systems requiring store—and—forward data, the non-volatile RAM must provide the desired fast write cycle as well as protection of memory in the event of a power loss. Despite the promise of such a memory device and the effort invested by the industry, the ideal nonvolatile RAM remains elusive.

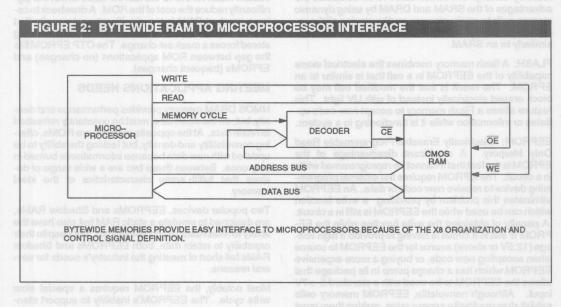
To more nearly emulate the ideal nonvolatile RAM, Dallas Semiconductor combines its intelligent CMOS control circuitry (DS1210), a lithium energy source, and a very low power SRAM to offer a high density, nonvolatile memory.

Four devices, the DS1220 (2K x 8 bits), DS1225 (8K x 8 bits), DS1230 (32K x 8 bits), and DS1245 (128K x 8 bits), use this fusion of technologies to provide a nonvol-

atile random access memory solution at a density of up to 1024K bits.

CMOS static RAMs currently available have read and write cycle times of under 100 ns, which exceed most system requirements. This alleviates the problem of the EEPROM, because there is no wear—out mechanism or write cycle limitation.

Static RAMs are also the easiest to use and interface because the pinout configurations are standard throughout the industry. In fact, X8 or bytewide static RAMs can be interfaced directly to microprocessors (Figure 2). In addition, CMOS static RAMs offer low power in both active and standby modes, a characteristic sought by many designers. In most designs, RAMs remain in standby much of the time, keeping power consumption negligible. In the standby mode, current drain consists only of leakage currents in the tens of nanoamperes.



## 4

#### **PUTTING LITHIUM AND RAM TOGETHER**

The minute leakage current of CMOS RAMs can be sustained with a backup energy source to yield a most attractive nonvolatile memory. However, the actual solution involves more than just a CMOS memory and back up energy source (see Figure 3).

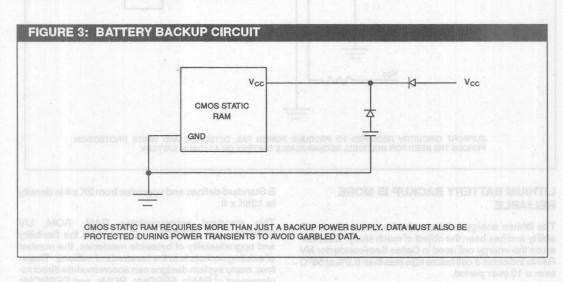
Battery backup design schemes are many and varied. The increase in density and availability of low powered CMOS memories in recent years has made this approach even more attractive. Yet problems still exist with battery backup design due to battery packaging and a lack of the appropriate standard components to implement the support circuitry. One problem is providing isolation between the battery and power supply (see Figure 4). Diodes can provide isolation but produce a voltage drop which requires nonstandard power supplies and also subtracts from the battery voltage. A second problem is the circuitry must be powered from the battery. Unless these devices draw an extremely modest amount of current, battery selection changes drastically. In fact, a current drain of even a couple of micro-

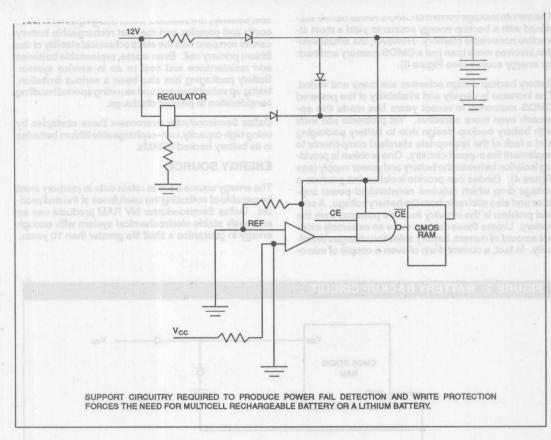
amperes dictates the use of either rechargeable batteries or a replaceable battery scheme. If rechargeable batteries are selected, the recharging circuit can be costly and complex and the best rechargeable battery cannot compare with the electrochemical stability of the lithium primary cell. Even worse, replaceable batteries add maintenance and cost to an in–service system. Battery packaging has also been a serious limitation, taking up valuable space and requiring special handling consideration to prevent discharge.

Dallas Semiconductor overcomes these obstacles by using high capacity, non-rechargeable lithium batteries in its battery backed SRAMs.

#### **ENERGY SOURCE**

The energy source used to retain data in memory must be capable of outlasting the usefulness of the end product. Dallas Semiconductor NV RAM products use an extremely stable electrochemical system with enough energy to guarantee a shelf life greater than 10 years.





# LITHIUM BATTERY BACKUP IS MORE RELIABLE

The lithium energy cell has raised concern about reliability and has been the object of much study. Data taken on the energy cell used in Dallas Semiconductor NV RAMs indicates a cell failure rate less than 0.5% at 55°C over a 10 year period.

Additional life studies taken on the same lithium energy source encapsulated in the manufacture of Dallas Semiconductor's NV RAMs have produced no failures in over 12 million device hours at 85°C. The lithium energy cell, then, is ideal for commercial and industrial semiconductor applications.

#### RETROFITTING EXISTING DESIGNS

The pinout of Dallas Semiconductor NV RAMs is an established industry standard (Figure 9). The Joint Electronic Devices Engineering Council's Bytewide Version

B Standard defines and upgrades from  $2K \times 8$  in density to  $128K \times 8$ .

This standard accommodates RAM, ROM, UV EPROMs, and EEPROMs. Because of the flexibility and upgradeability of bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore, many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs, and EEPROMs with Dallas Semiconductor NV SRAMs. These solutions add real time programmability and/or density upgrades to existing systems without redesign. Real time programmability gives the system the ability to be personalized by the end user. In other words, NV SRAMs can be retrofitted into existing designs without making changes to existing hardware. This retrofitting offers a cost effective, practical solution for companies who have invested in other memory devices that are less than ideal for their needs. For example, a design using conventional static RAM can be upgraded to nonvolatile

4

memory by substituting a Dallas Semiconductor NV SRAM for the RAM memory.

#### IN-CIRCUIT PROGRAMMABILITY

The advantages of NV SRAM can be related to the capability of software. Modern systems seek customization for the cost of standard product. In this aspect, software can be adapted in a system to perform specialized functions. It is even possible to totally modify a system personality over the telephone. In-circuit programming also reduces maintenance cost by eliminating service calls to update software. Software stored in RAM can be updated as often as necessary, depending on the configuration or application of the system.

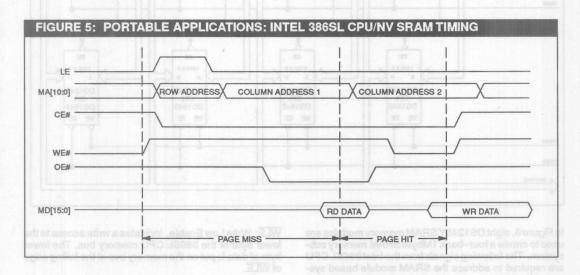
#### PORTABLE APPLICATIONS

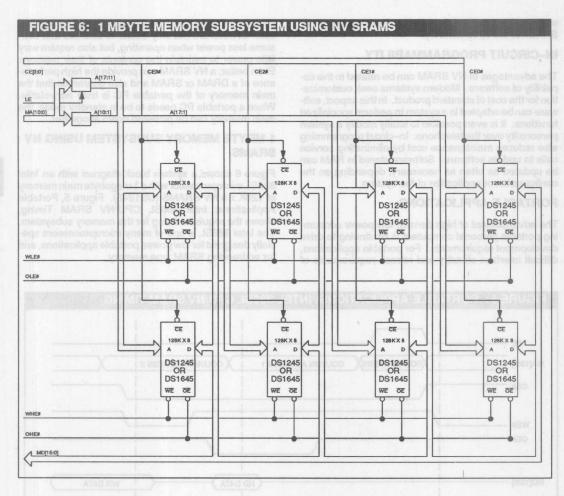
The advancement of high density, low power consuming portable personal computers is continuing to drive development requirements. For portable applications, difficult interface circuitry and refresh requirements of

DRAM memories make them unsuitable for this application. SRAMs are not only easier to address and consume less power when operating, but also require very little power to maintain the contents of their memory. Even better, a NV SRAM can provide the high performance of a DRAM or SRAM and also guarantee that the main memory of the portable PC is truly nonvolatile. When a portable PC needs to be in standby mode, the main memory can be powered down altogether.

# 1 MBYTE MEMORY SUBSYSTEM USING NV SRAMS

Figure 6 shows a system block diagram with an Intel 386SL microprocessor with a 1 megabyte main memory of 128K x 8 NV SRAMS (DS1245). Figure 5, Portable Applications: Intel 386SL CPU/NV SRAM Timing, shows the requisite timing for the memory subsystem. The Intel 386SL is one of many microprocessors specially designed for low power, portable applications, and for addressing SRAM type memory.





In Figure 6, eight DS1245Y SRAM memory modules are used to create a four-bank 1Mbyte SRAM memory subsystem. The following signals from the Intel 386SL CPU are required to address the SRAM module based system. The 386SL memory controller must be configured in its SRAM addressing mode for this application.

LE: Latch Enable. This signal selects is active high and serves to indicate that a row address is to be put on the address bus. A row address must be latched at this signal's falling edge. LE is connected to the latch enable input of the SRAM address latch.

MA[10:0]: Multiplexed Memory Address Bus. This bus provides address information for the Memory Controller Unit. The bus provides a 22 bit address in a multiplexed row/column sequence.

CE[3:0]: Chip Enable outputs. These signals provide upper and lower byte enables for each SRAM bank.

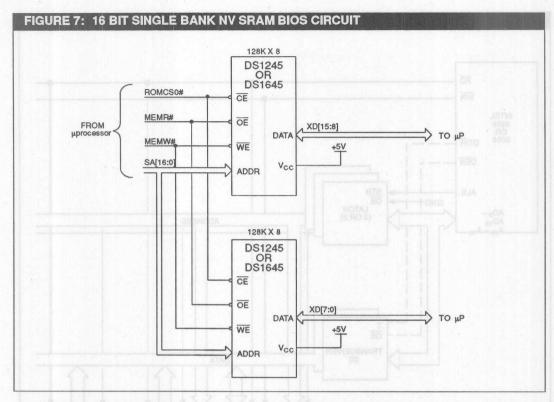
WLE: Write Low Enable. Indicates a write access to the lower byte of the 386SL CPU memory bus. The lower byte of data is put on the memory bus at the falling edge of WLE.

WHE: Write High Enable. Indicates a write access to the high byte of the 386SL CPU memory bus. The high byte of data is put on the memory bus at the falling edge of WHE.

OLE: Output Low Enable. Enables the lower byte output from the SRAM modules.

OHE: Output High Enable. Enables the high byte output from the SRAM modules.

MD[15:0]: Memory Data Bus. This bus provides data information for the Memory Controller Unit. Accesses from the Memory Controller Unit to the SRAM memory modules take place through this bus.



# 16 BIT SINGLE BANK NV SRAM BIOS CIRCUIT

Figure 7 shows Dallas NV SRAMs providing bios memory storage for an Intel 386SL CPU. Using the DS1645 NV SRAMs provide several advantages over using either OTP EPROM or FLASH type memories.

Flash memories require more operating current than NV SRAMs. Flash memories also require a high voltage source, 12V+, for any writes or updates that must be made to bios. NV SRAMs, on the other hand, require access. Like Flash memories, a DS1645 NV SRAM maintains the contents of its memory in the absence of V $_{\rm CC}$ . A DS1645 has the additional feature that it can be easily programmed (through a series of 20 sequential reads) to write protect user selected blocks of memory. In effect, individual memory blocks in the SRAM module can be configured to appear as ROM memory, without detracting from the DS1645's ability to receive BIOS updates in its non write protected blocks of memory.

Traditional OTP EPROM's, while nonvolatile and very low power consuming like the DS1245 and DS1645 NV SRAMs, are lacking in that they can only be programmed once, and usually require a special fixture to be programmed. DS1245 and DS1645 NV SRAMs are

almost equally low power consuming, and provide the capability to update BIOS. DS1245 and DS1645 NV SRAMs also provide fast 100ns access times, negating the need to insert additional wait states into BIOS access timing requirements.

The signals shown in Figure 7 are taken directly from the Intel 386SL CPU:

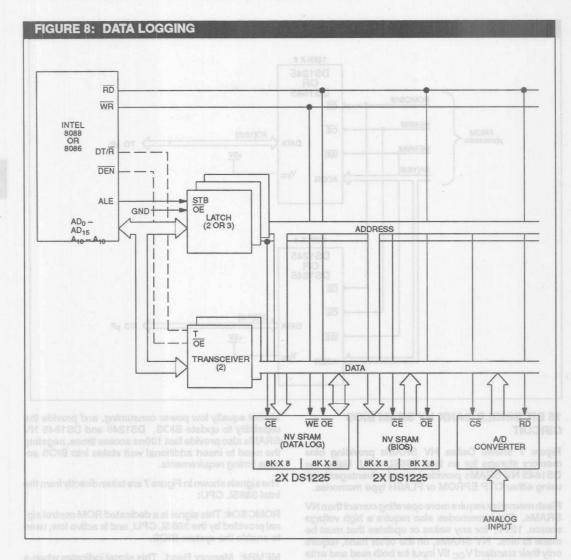
ROMCSO#: This signal is a dedicated ROM control signal provided by the 386SL CPU, and is active low, used to enable the system BIOS.

MEMR#: Memory Read. This signal indicates when a memory read access is occurring on the ISA-bus or X-bus, and is active low.

MEMW#: Memory Write. This signal indicates when a memory write access is occurring on the ISA-bus or X-bus, and is active low.

XD[15:0]: X-bus Data. Buffered data lines from the system data bus. These signals are produced using an external transceiver (see Intel 386SL Superset System Design Guide).

SA[16:0]: System Address Bus. This bus is driven by the 386SL CPU for system I/O accesses, and supplies both the ISA-bus and X-bus.

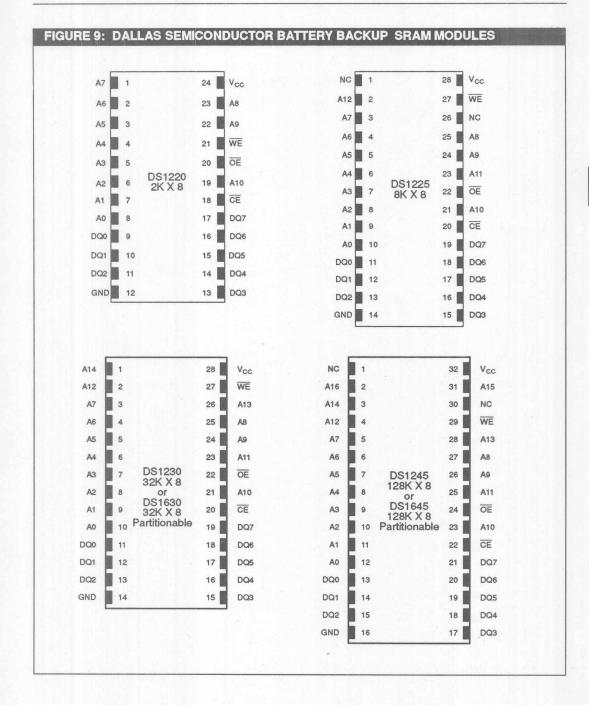


#### **DATA LOGGING**

Figure 8 shows Dallas Semiconductor's NV SRAMs can provide a special advantage in environments where the power supply is not entirely reliable, or when power must periodically be shutdown. Dallas Semiconductor NV SRAMs contain memory control circuitry which not only maintains the data in the SRAM in the absence of power, but also write protects the device if  $V_{\rm CC}$  is out of tolerance. This feature ensures that an unstable power supply does not corrupt data which has been collected.

In this application, an Intel 8086 is shown in its minimal mode, connected to an address latch and bus transceiv-

er to demultiplex the 8086's bus (see Figure 8). The resulting address and data busses may then be connected directly to two memory banks, one 8K x 16 bios memory consisting of two DS1225 NV SRAMs, the other an 8K x 16 memory bank consisting of two DS1225's acting as a data log. A data collecting device, such as an A/D converter, can be addressed as a read only peripheral device to sample a value and write it to the DS1225 acting as a data log. The DS1225 acting as the data log can transmit its data on the data bus to another peripheral, or may be removed from the system and taken to another location to have their logs extracted.



**Silicon Timed Circuits** 

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

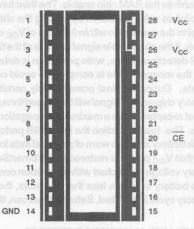
# DALLAS

## DS1213B SmartSocket 16K/64K

#### **FEATURES**

- Accepts standard 2K x 8 or 8K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K x 8 to 8K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

#### PIN ASSIGNMENT



28-Pin Intelligent Socket

#### **PIN DESCRIPTION**

All pins pass through except 20, 26, 28.

Pin 20 CE - Conditioned Chip Enable

Pin 26 V<sub>CC</sub> - Switched V<sub>CC</sub> for 24-pin RAM

Pin 28 V<sub>CC</sub> - Switched V<sub>CC</sub> for 28-pin RAM

Pin 14 GND - Ground

#### DESCRIPTION

The DS1213B SmartSocket 16/64K is a 28-pin, 0.6 inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K x 8 or 24-pin 2K x 8 lower-justified JE-DEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility . The SmartSocket monitors incoming V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write

protection is unconditionally enabled to prevent garbled

Using the SmartSocket saves printed circuit board space since the combination of the SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pins 28, 26, 20, and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

#### **OPERATION**

The DS1213B SmartSocket performs five circuit functions required to battery back up a CMOS memory. First, a switch is provided to direct power from the battery or V<sub>CC</sub> supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power-fail detection. Power-fail detection occurs between 4.75 and 4.5 volts. The DS1213B constantly monitors the V<sub>CC</sub> supply. When V<sub>CC</sub> falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of V<sub>CC</sub> or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213B performs is to check battery status to warn of potential data loss. Each time that V<sub>CC</sub> power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1213B Smart-Socket provides an internal isolation switch which provides for the connection of two batteries. During battery back up the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mA/hr capacity, making the total 70 mA/hr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the  $V_{CC}$  pin. In order to read the cell potential, apply  $V_{CC}$  and then remove power. The cell potential will then be available on pins 26, 28, and 20.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to 7.0V 0°C to 70°C 40°C to +70°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	Vcc	4.75	5.0	5.5	nbec <b>y</b> ed III BK x B or 2	1,3
Logic 1 PIN 20 L	V <sub>IH</sub>	2.2	Apos tini ital Apos tini ital	V <sub>CC</sub> +0.3	٧	1,3
Logic 0 PIN 20 L	vino ee u x V <sub>IL</sub> Sma	-0.3	ry volatility .	+ 0.8	Isbo V.s am	1,3

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	Icc			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	Vcco	V <sub>CC</sub> -0.2		14."	V	3, 8
PIN 26 U, PIN 28 U Supply Current	Icco			80	mA	3,8
PIN 20 L CE Input Leakage	II.	-1.0		+1.0	μА	3, 4
PIN 20 U CE Output @ 2.4 V	Гон	-1.0			mA	2,3
PIN 20 U CE Output @ .4V	loL	1	VLT.	4.0	mA	2,3

(0°C to 70°C, V<sub>CC</sub> < 4.5V)

	THE REAL PROPERTY.	B		1-		
PIN 20 U Output	Vohl	V <sub>CC</sub> -0.2 V <sub>BAT</sub> -0.2			V	. 3
PIN 26 U, PIN 28U Battery Current	IBAT			1	μА	3,6
PIN 26 U, PIN 28 U Battery Voltage	V <sub>BAT</sub>	2	3	3.6	V	3

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

CAFACITANCE						(1A - 23 C
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	CIN	aV.	1/	5	/ 3	3
Output Capacitance PIN 20 U	C <sub>OUT</sub>			7	3	3

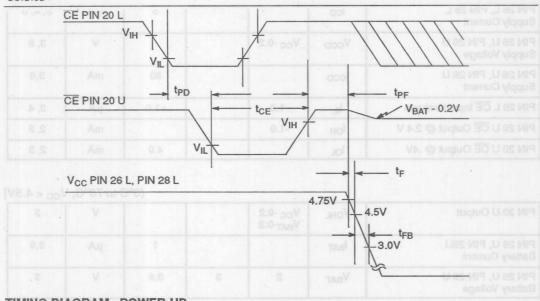
### AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 4.75 \text{ to } 5.5\text{V})$ 

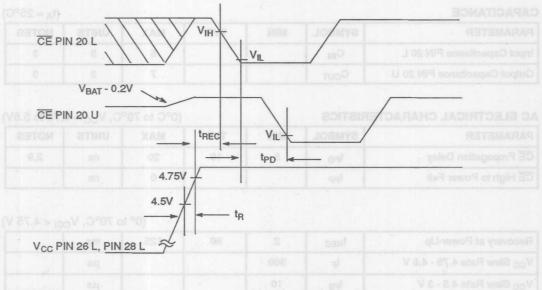
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE Propagation Delay	t <sub>PD</sub>	5 9	10	20	ns	2,9
CE High to Power Fail	tpF		1	0	ns	De la constant

(0° to 70°C, V<sub>CCI</sub> < 4.75 V)

Recovery at Power-Up	t <sub>REC</sub>	2	80	125	ms	Yor P
V <sub>CC</sub> Slew Rate 4.75 - 4.5 V	t <sub>F</sub>	300			μs	
V <sub>CC</sub> Slew Rate 4.5 - 3 V	t <sub>FB</sub>	10			μs	m Less core as
V <sub>CC</sub> Slew Rate 4.5-4.75 V	bev <sup>t</sup> Ris et	0	s elcortarebs	u evitegen er	μs	ndo on rebn
CE Pulse Width	t <sub>CE</sub>	Minist Bened	a eguaricali	1.5	μs	7



#### **TIMING DIAGRAM - POWER-UP**

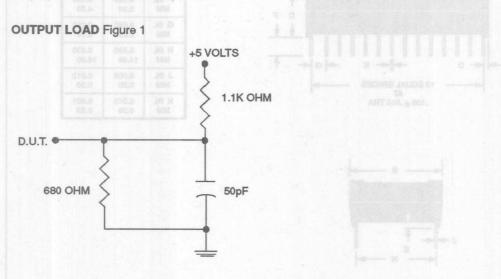


#### WARNING:

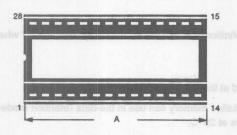
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal will discharge internal lithium source as exposed voltage pins are present.

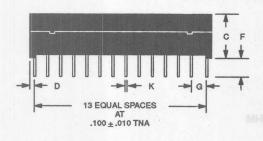
#### NOTES:

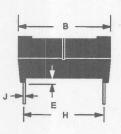
- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 1.
- 3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
- 4. No memory inserted in the socket.
- 5. Pin 26 L may be connected to V<sub>CC</sub> or left disconnected at the PC board.
- I<sub>BAT</sub> is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
- 7. t<sub>CE</sub> max. must be met to ensure data integrity on power loss.
- 8. V<sub>CC</sub> is within nominal limits and a memory is installed in the socket.
- 9. Input pulse rise and fall times equal 10 ns.



### DS1213B INTELLIGENT SOCKET 28 PIN (FOR 600 MIL DIP)







PKG	28-	PIN	
DIM	MIN	MAX	
A IN.	1.380 35.05	1.420 36.07	
B IN.	0.690	0.720	
MM	17.53	18.29	
C IN.	0.350 8.89	0.395 10.03	
D IN.	0.035	0.065	
MM	0.89	1.65	
E IN. MM	0.015 0.38	0.035	
F IN.	0.120	0.160	
MM	3.04	4.06	
G IN.	0.090	0.110	
MM	2.29	2.79	
H IN.	0.590	0.630	
MM	14.99	16.00	
J IN.	0.008	0.012	
MM	0.20	0.30	
K IN.	0.015	0.021	
MM	0.38	0.53	

DS1213C

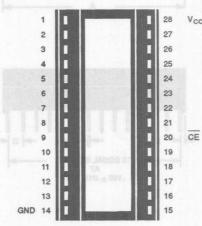
# SmartSocket 64K/256K



#### **FEATURES**

- Accepts standard 8K x 8 or 32K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K x 8 to 32K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

#### PIN ASSIGNMENT



28-Pin Intelligent Socket

#### **PIN DESCRIPTION**

All pins pass thorough except 20, 28.

Pin 20 CE - Conditioned Chip Enable

Pin 28 V<sub>CC</sub> - Switched V<sub>CC</sub>

Pin 14 GND - Ground

#### DESCRIPTION

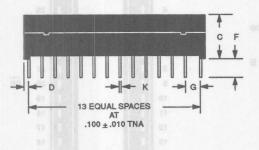
The DS1213C SmartSocket is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

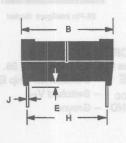
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

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PKG	28-	PIN
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN.	0.350 8.89	0.395
D IN. MM	0.035 0.89	0.065 1.65
E IN.	0.015 0.38	0.035
F IN.	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630
J IN. MM	0.008	0.012
K IN.	0.015	0.021

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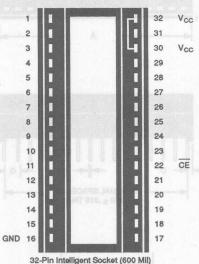
## **DALLAS** SEMICONDUCTOR

## DS1213D SmartSocket 64K/256K/1M

#### **FEATURES**

- Accepts standard 8K x 8, 32K x 8, 128K x 8, or 512K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- · Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K x 8 to 512K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

All pins pass through except 22, 30 and 32.

Pin 22 CE - Conditioned Chip Enable

Pin 32 V<sub>CC</sub> - Switched V<sub>CC</sub> for 32-pin RAM

Pin 30 V<sub>CC</sub> - Switched V<sub>CC</sub> for 28-pin RAM

Pin 16 GND - Ground

#### DESCRIPTION

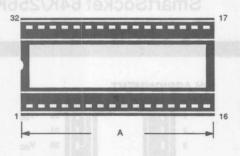
The DS1213D SmartSocket is a 32-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8 or 512K x 8 bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

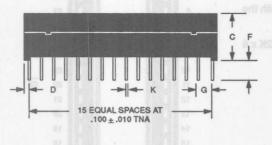
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

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## DS1213D INTELLIGENT SOCKET 32-PIN (FOR 600 MIL DIP)





B

PKG	. 32-	PIN
DIM	MIN	MAX
A IN. MM	1.580 40.13	1.620 41.15
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.410
D IN.	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN.	0.120 3.04	0.160 4.06
G IN.	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN.	0.015	0.021

Using the SmartSocket saves printed circuit board apace since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

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aled with memory votatility. The SmartSocket monire incoming V<sub>CC</sub> for an out-of-tolerance condition, then such a condition occurs, an internal lithium surce is automatically switched on an internal coloration.

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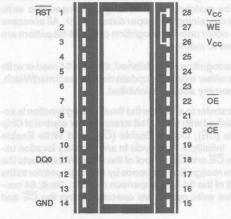
# DALLAS

## DS1216B SmartWatch/RAM 16K/64K

#### **FEATURES**

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K x 8 and 8K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min/month @25°C

#### **PIN ASSIGNMENT**



28-Pin Intelligent Socket

#### **PIN DESCRIPTION**

All Pins Pass Through Except 20, 26, 28

Pin 1 RST - Reset

Pin 11 DQ0 - Data Input/Output 0

Pin 14 GND - Ground

Pin 20 CE - Conditioned Chip Enable

Pin 22 OE - Output Enable

Pin 26 V<sub>CC</sub> - Switched V<sub>CC</sub> for 24 Pin RAM

Pin 27 WE - Write Enable

Pin 28 V<sub>CC</sub> - Switched V<sub>CC</sub> for 28 Pin RAM

#### DESCRIPTION

The DS1216B SmartWatch/RAM 16/64K is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V<sub>CC</sub>

for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The Smart-Watch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

#### **OPERATION**

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ( $\overline{\text{CE}}$ ), Output Enable ( $\overline{\text{OE}}$ ), and Write Enable ( $\overline{\text{WE}}$ ). Initially, a read cycle to any memory location using the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the  $\overline{\text{CE}}$  and

WE control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the OE pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with CE cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

### SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1 000 ages of the segment patterns of the segment pat

										HEX
	7							0		VALUE
BYTE 0	1	leadfi -	0	0	0	1	0	1	]_	C5
BYTE 1	0	0	01/10	a.1 mg	1	0	1	0		зА
BYTE 2	1	0	10	0	0	0	1	1	]	А3
BYTE 3	0	1	0	1	1	1	0	0	]-	5C
BYTE 4	1	DI 10	0	0	0	1	0	1	]•]	C5
BYTE 5	0	0	1	1	1	0	1	. 0		зА
BYTE 6	1	0	1	0	0	0	1	1	]-	A3
BYTE 7	0	ns no b	0	1	1	1	0	0	]-	5C

#### NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10<sup>19</sup>. This pattern is sent to the SmartWatch LSB to MSB.

### NONVOLATILE CONTROLLER OPERATION

The DS1216B SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or Vcc supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartWatch provides is power-fail detection. Power-fail detection occurs at approximately 4.0 volts. The DS1216B constantly monitors the V<sub>CC</sub> supply. When V<sub>CC</sub> goes out of tolerance, a comparator outputs a power-fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of Vcc or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

### **SMARTWATCH REGISTER INFORMATION**

The SmartWatch information is contained in eight registers of eight bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Smart-Watch registers, each register must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the

registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

### AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

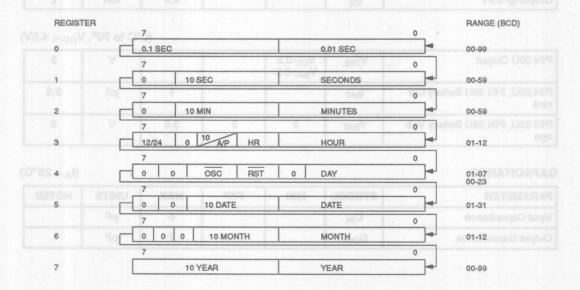
# OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit is set to logic 0, a low input on the RESET pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 1 o, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

#### **ZERO BITS**

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

# **SMARTWATCH REGISTER DEFINITION** Figure 2



**ABSOLUTE MAXIMUM RATINGS\*** 

VOLTAGE ON ANY PIN RELATIVE TO GROUND
OPERATING TEMPERATURE
STORAGE TEMPERATURE
SOLDERING TEMPERATURE

-0.3V TO 7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

# RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	Vcc	4.5	5.0	5.5	menV <sub>ery</sub> cl	1,3
Logic 1	V <sub>IH</sub>	2.2	INTERBITE DE	V <sub>CC</sub> +0.3	V	1,10
Logic 0	V <sub>IL</sub>	-0.3	ROTAM	+0.8	V	1,10

# DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub>=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply	Icci	RES OF	be handled Hadividual t	5	mA	3,4,5
PIN 26U, PIN 28U Supply Voltage	Vcco	V <sub>CC</sub> -0.2	neous mean	ma soubon	blucy rate	3,8
PIN 26U, PIN 28U Supply Current	Icco	anoit		80	mA	3,8
Input Leakage	IIL	-1.0	golfine bas	+1.0	μΑ	4,10,13
Output @ 2.4V	Іон	-1.0	a warns	aao aan	mA	2
Output @ 0.4V	loL			4.0	mA	2

(0°C to 70°, V<sub>CC</sub> < 4.5V)

PIN 20U Output	V <sub>OHL</sub>	V <sub>CC</sub> -0.2 V <sub>BAT</sub> -0.2		201	V	3
PIN 26U, PIN 28U Battery Cur- rent	I <sub>BAT</sub>			1	μА	3,6
PIN 26U, PIN 28U Battery Voltage	V <sub>BAT</sub>	2	3	3.6	V	3

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>		TO MONTH	7	pF	-8

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# AC ELECTRICAL CHARACTERISTICS

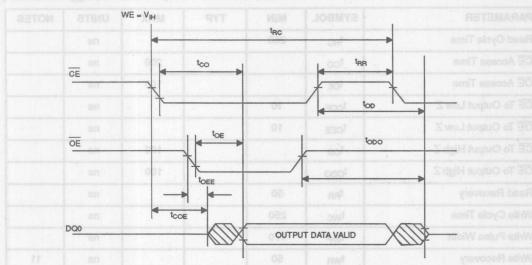
(0°C to 70°C, V<sub>CC</sub>=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	250		p	ns	
CE Access Time	tco		L 001	200	ns	
OE Access Time	t <sub>OE</sub>			100	ns	
CE To Output Low Z	tcoe	10			ns	
OE To Output Low Z	toee	10	and		ns	
CE To Output High Z	top			100	ns	
OE To Output High Z	topo	\		100	ns	
Read Recovery	t <sub>RR</sub>	50	р	(minuted in the control of the contr	ns	
Write Cycle Time	twc	250		00 -	ns	
Write Pulse Width	t <sub>WP</sub>	170	KO -		ns	
Write Recovery	t <sub>WR</sub>	50			ns	11
Data Setup Time	t <sub>DS</sub>	100	E TO SMA	ITE CYCL	ns	12
Data Hold Time	t <sub>DH</sub>	0		18V w 30	ns	12
CE Pulse Width	tcw	170			ns	
RESET Pulse Width	t <sub>RST</sub>	200			ns	
CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	2, 9
CE High to Power-Fail	tpF	1	1	0	ns	

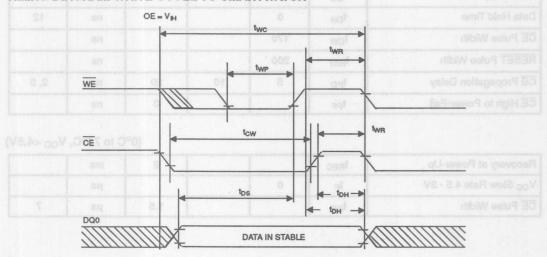
(0°C to 70°C, V<sub>CC</sub> <4.5V)

Recovery at Power-Up	tREC		2	ms	
V <sub>CC</sub> Slew Rate 4.5 - 3V	t <sub>F</sub>	0		μѕ	
CE Pulse Width	t <sub>CE</sub>	14.	1.5	μs	7

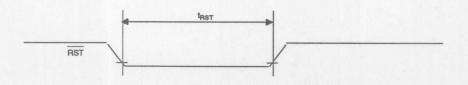
# TIMING DIAGRAM-READ CYCLE TO SMARTWATCH



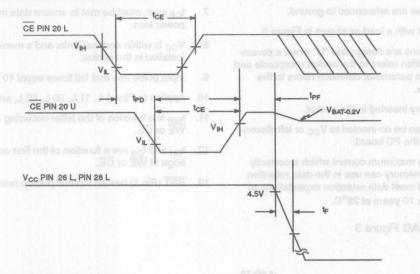
# TIMING DIAGRAM-WRITE CYCLE TO SMARTWATCH



# **TIMING DIAGRAM-RESET FOR SMARTWATCH**

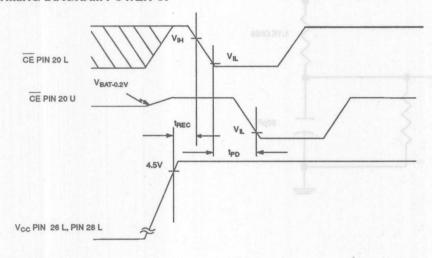


# **TIMING DIAGRAM-POWER-DOWN**



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# **TIMING DIAGRAM-POWER-UP**



# WARNING

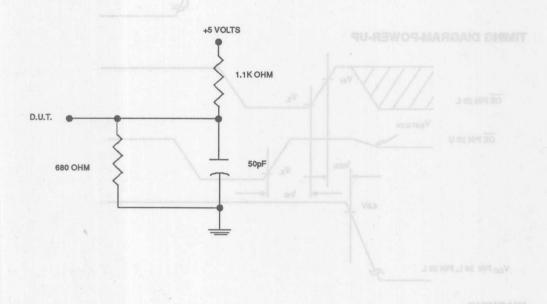
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

# NOTES

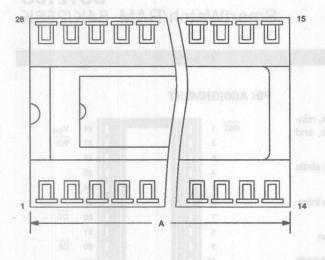
- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 3.
- Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
- 4. No memory inserted in the socket.
- Pin 26L can be connected to V<sub>CC</sub> or left disconnected at the PC board.
- I<sub>BAT</sub> is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.

- t<sub>CE</sub> max. must be met to ensure data integrity on power loss.
- V<sub>CC</sub> is within nominal limits and a memory is installed in the socket.
- 9. Input pulse rise and fall times equal 10 ns.
- 10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L.
- t<sub>WR</sub> is a function of the latter occurring edge of WE or CE.
- 12.  $t_{DH}$  and  $t_{DS}$  are a function of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 13. RST (Pin 1) has an internal pull-up resistor.

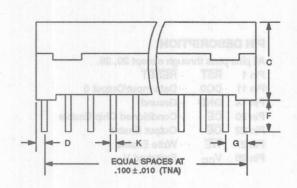
# **OUTPUT LOAD Figure 3**

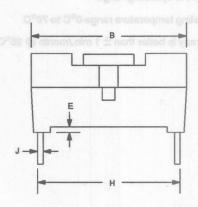


# DS1216B SMARTWATCH



PKG	28-F	PIN	32-F	PIN
DIM	MIN	MAX	MIN	MAX
A IN.	1.390	1.420	1.580	1.620
MM	35.31	36.07	40.13	41.14
B IN.	0.690	0.720	0.690	0.720
MM	17.53	18.29	17.53	18.29
C IN.	0.350	0.395	0.350	0.410
MM	8.89	10.03	8.89	10.40
D IN.	0.035	0.065	0.035	0.065
MM	0.89	1.65	0.89	1.65
E IN.	0.015	0.035	0.015	0.035
	0.38	0.89	0.38	0.89
F IN.	0.120	0.160	0.120	0.160
	3.04	4.06	3.04	4.06
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.590	0.630	0.590	0.630
	14.99	16.00	14.99	16.00
J IN.	0.008 0.20	0.012 0.30	0.008 0.20	0.012
K IN.	0.015	0.021	0.015	0.021
	0.38	0.53	0.38	0.53





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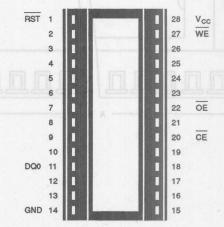


# DS1216C SmartWatch/RAM 64K/256K

### **FEATURES**

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K x 8 and 32K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 min/month @ 25°C

### **PIN ASSIGNMENT**



28-Pin Intelligent Socket

# **PIN DESCRIPTION**

All pins pass through except 20, 28.

Pin 1 RST - RESET

Pin 11 DQ0 - Data Input/Output 0

Pin 14 GND - Ground

Pin 20 CE - Conditioned Chip Enable

Pin 22 OE - Output Enable

Pin 27 WE - Write Enable

Pin 28 V<sub>CC</sub> - Switched V<sub>CC</sub>

### DESCRIPTION

The DS1216C SmartWatch/RAM is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS stat ic RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory vol-

atility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

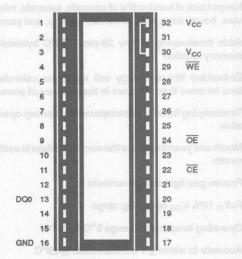
### **FEATURES**

- Converts standard 8K x 8, 32K x 8, 128K x 8, and 512K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 min./month @ 25°C

# DESCRIPTION

The DS1216D SmartWatch/RAM 256K/1M is a 32-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8, or 512K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to prob-

# **PIN ASSIGNMENT**



32-Pin Intelligent Socket

# PIN DESCRIPTION

All pins pass through except 22, 30 and 32.

Pin 1 RST - RESET

Pin 13 DQ0 - Data Input/Output 0

Pin 16 GND - Ground

Pin 22 CE - Conditioned Chip Enable

Pin 24 OE - Output Enable

Pin 29 WE - Write Enable

Pin 30 V<sub>CC</sub> - Switched V<sub>CC</sub> for 28-pin RAM

Pin 32 V<sub>CC</sub> - Switched V<sub>CC</sub> for 32-pin RAM

lems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

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# DS1216E SmartWatch/ROM 64K/256K

#### **FEATURES**

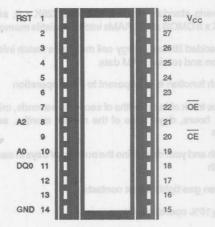
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% V<sub>CC</sub> operating range
- Operating temperature range 0°C to 70°C
- Accurate to within ± 1 minute/month @25°C

# DESCRIPTION

The DS1216E SmartWatch/ROM 64/256K is a 28-pin, 600 mil-wide DIP socket with a built-in CMOS time-keeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of the SmartWatch and the mated memory

### **PIN ASSIGNMENT**



28-Pin Intelligent Socket

### **PIN DESCRIPTION**

Pin 1	RST	Decet
PID 1	HSI	- Reset

Pin 8 A2 - Address Bit 2 (READ/WRITE)

Pin 10 A0 - Address Bit 0 (Data Input)
Pin 11 DQ0 - I/O<sub>0</sub> (Data Output)

Pin 14 GND - Ground

Pin 20 CE - Conditioned Chip Enable

Pin 22 OE - Output Enable

Pin 28 V<sub>CC</sub> -+5 VDC to the Socket

All pins pass through to the socket except 20.

device takes up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20, and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 (CE), which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

### **OPERATION**

A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnects the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals OE and CE, and data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal (OE or CE) must transition low to begin and high to end memory cycles that are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle.

Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch, ensuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of READ/ WRITE (A2). Cycles to other locations outside the memory block can be interleaved with CE and OE cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 (RESET) low if enabled, or on power-up. The RESET can occur during pattern recognition or while accessing the SmartWatch registers. RESET causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

# NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V<sub>CC</sub> supply, depending on which voltage is greater. The second function provides power-fail detection. Power-fail detection typically occurs at approximately 4.0 volts. Finally, the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power-fail detection has occurred. Power-fail detection also has the same effect on data transfer as the RESET input.

### SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

# AM-PW12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

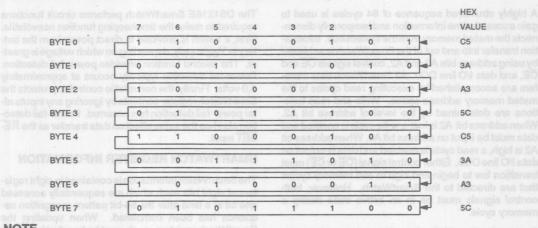
### OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit is set to logic 0, a low input on the RESET pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is turned off. When set to logic 0, the oscillator turns on and the watch becomes operational. Both bits are set to a logic 1 when shipped from the factory

### **ZERO BITS**

Registers 1,2,3,4,5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

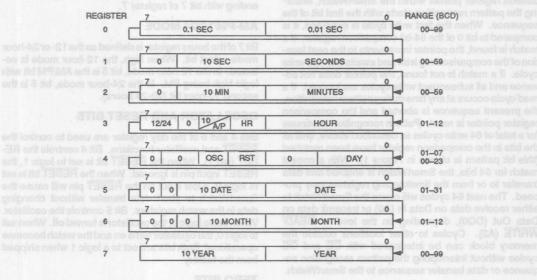
# **SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1**



# NOTE

The pattern recognition sequence in Hex is C5, 3A, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch are less than 1 in 1019. This pattern is sent to the SmartWatch LSB to MSB.

# **SMARTWATCH REGISTER DEFINITION Figure 2**



5

**ABSOLUTE MAXIMUM RATINGS\*** 

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE

-0.3V TO 7.0V 0°C TO 70°C -40°C TO +70°C

SOLDERING TEMPERATURE

260°C FOR 10 SECONDS

# RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L Supply Voltage	Vcc	4.5	5.0	5.5	V	1, 3
Logic 1	V <sub>IH</sub>	2.2	679	V <sub>CC</sub> +0.3	V	1,6
Logic 0	V <sub>IL</sub>	-0.3	THE	+0.8	V	1, 6

# DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub>=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L, Supply Current	Icci	0.4	- WO	5	mA	3,4
Input Leakage	J <sub>IL</sub>	-1.0	HW	+1.0	μА	4,6,10
Output @ 2.4V	Іон	-1.0	80/		mA	2
Output @ 0.4V	l <sub>OL</sub>	1 0	1 407	4.0	mA	2

### CAPACITANCE

(ta = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# AC ELECTRICAL CHARACTERISTICS

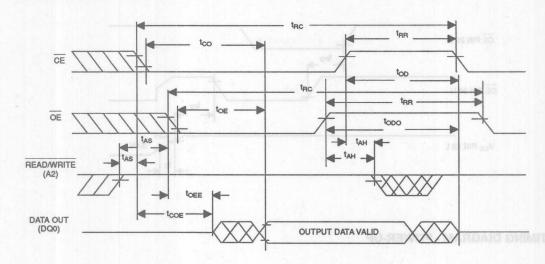
(0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

	1/0.3.02	EVE A.	UNITORS D	CHAPTA IES	I LAN YEAR D	DEPORT
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	250	E MINE S	BRU	ns	DUIRBILL
CE Access Time	tco			200	ns	
OE Access Time	t <sub>OE</sub>	ann to nois	ctions of this	100	ns	nis is a si hose ladi
CE To Output Low Z	tCOE	10	to aboined be	for extend	ns	altsi mun
OE To Output Low Z	toee	10	TORON OF	magago	ns	RAMINO OF
CE To Output High Z	top	1 3,053	Luseume	100	ns	Name of the
OE To Output High Z	topo			100	. ns	ch too Ut
Address Setup Time	t <sub>AS</sub>	20	1 00		ns	9
Address Hold Time	t <sub>AH</sub>		11111	10	ns	8
Read Recovery	t <sub>RR</sub>	50	1		ns	7
Write Cycle Time	twc	250	smes	HACTER	ns	roaus:
CE Pulse Width	tcw	170	Loguiya		ns	TOU A CLA
OE Pulse Width	tow	170			ns	o toe M
Write Recovery	t <sub>WR</sub>	50			ns	7
Data Setup Time	t <sub>DS</sub>	100	lou		ns	8
Data Hold Time	t <sub>DH</sub>	0	lou	-	ns	8
RST Pulse Width	t <sub>RST</sub>	200			ns	
CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	2,5
CE High to Power-Fail	tpF	MIN	TORMAS	0	ns	THMARK

(0°C to 70°C, V<sub>CC</sub> < 4.5V)

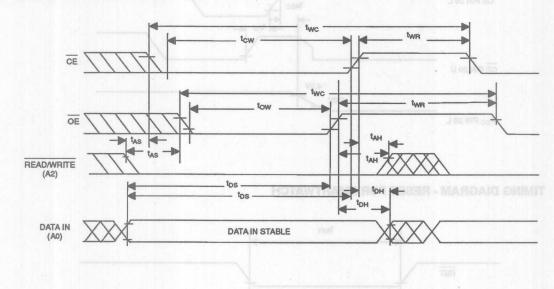
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	tREC			2	ms	
V <sub>CC</sub> Slew Rate 4.5 - 3V	t <sub>F</sub>	0			μs	

# **TIMING DIAGRAM - READ CYCLE**



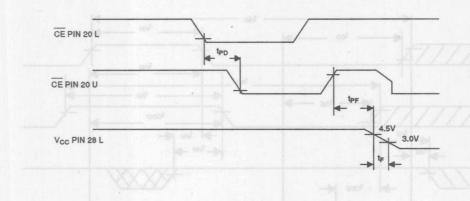
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# **TIMING DIAGRAM - WRITE CYCLE**

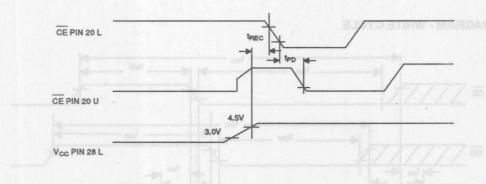


WARNING

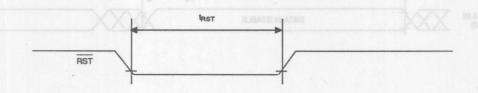
# **TIMING DIAGRAM - POWER-DOWN**



# **TIMING DIAGRAM - POWER-UP**



# TIMING DIAGRAM - RESET FOR SMARTWATCH



# WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

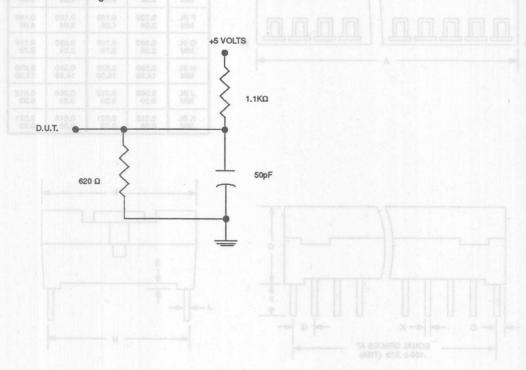
# NOTES

- 1. All voltages are referenced to ground.
- 2. Measured with a load shown in Figure 3.
- Pin locations are designated "U" when a parameter definition refers to the socket receptacle and
  "L" when a parameter definition refers to the
  socket pin.
- 4. No memory inserted in the socket.
- 5. Input pulse rise and fall times equal 10 ns.

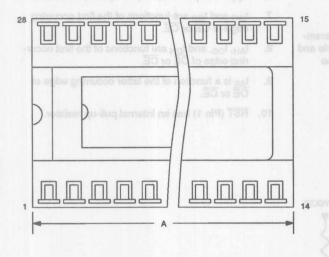
- 6. Applies to pins 1 L, 8 L, 10 L, 20 L, and 22 L.
- t<sub>WR</sub> and t<sub>RR</sub> are functions of the first occurring edge of OE or CE.
- 8.  $t_{AH}$ ,  $t_{DS}$ , and  $t_{DH}$  are functions of the first occurring edge of  $\overline{OE}$  or  $\overline{CE}$ .
- 9.  $\frac{t_{AS}}{OE}$  is a function of the latter occurring edge of  $\overline{OE}$  or  $\overline{CE}$ .
- 10. RST (Pin 1) has an internal pull-up resistor.

**OUTPUT LOAD** Figure 3

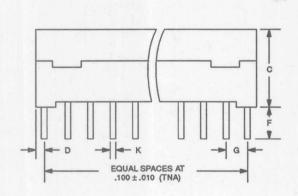
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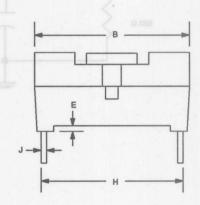


# **DS1216E SMARTWATCH**



PKG	28-F	PINSOLS	32-F	PIN	
DIM	MIN	MAX	MIN	MAX	
AIN.	1.390	1.420	1.580	1.620	
MM	35.31	36.07	40.13	41.14	
B IN.	0.690	0.720	0.690	0.720	
MM	17.53	18.29	17.53	18.29	
C IN.	0.350	0.395	0.350	0.410	
	8.89	10.03	8.89	10.40	
D IN.	0.035	0.065	0.035	0.065	
MM	0.89	1.65	0.89	1.65	
E IN.	0.015	0.035	0.015	0.035	
MM	0.38	0.89	0.38	0.89	
FIN.	0.120	0.160	0.120	0.160	
	3.04	4.06	3.04	4.06	
G IN.	0.090	0.110	0.090	0.110	
MM	2.29	2.79	2.29	2.79	
H IN.	0.590	0.630	0.590	0.630	
	14.99	16.00	14.99	16.00	
J IN.	0.008	0.012	0.008	0.012	
MM	0.20	0.30	0.20	0.30	
KIN.	0.015	0.021	0.015 0.02		
	0.38	0.53	0.38 0.53		





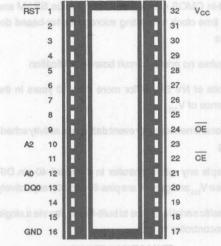
# **DALLAS** SEMICONDUCTOR

# DS1216F SmartWatch/ROM 64K/256K/1M

### **FEATURES**

- Adds timekeeping to any 32-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% V<sub>CC</sub> operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C

### **PIN ASSIGNMENT**



32-PIN INTELLIGENT SOCKET

# PIN DESCRIPTION

Pin 1	RST	- RESET
Pin 10	A2	- Address Bit 2 (READ/ WRITE)
Pin 12	AO	- Address Bit 0 (Data Input)
Pin 13	DQ0	- I/O <sub>0</sub> (Data Output)
Pin 16	GND	- Ground
Pin 22	CE	- Conditioned Chip Enable
Pin 24	OE	- Output Enable
Pin 32	Vcc	- +5 VDC to the Socket
All pins		rough to the socket except 22.

# DESCRIPTION

The DS1216F SmartWatch/ROM is a 32-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeping function remains transparent to the memory device placed above. The SmartWatch monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source automatically switches on to prevent loss of time and calendar data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22, and 24 for time-keeper control. All pins pass through to the socket receptacle except for pin 22 (CE), which is inhibited during the transfer of time information.

See the DS1216E SmartWatch/ROM/64/256K data sheet for technical details.

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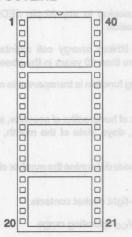


# DS1310/DS1311 Super Socket

### **FEATURES:**

- Built-in CMOS circuitry adds nonvolatile SRAM and real time clock to existing microcontroller-based designs
- Requires no printed circuit board modification
- ${}^{\bullet}$  4K bits of NV SRAM for more than 10 years in the absence of  ${\rm V_{CC}}$
- Optional timekeeper for event dating and activity scheduling
- Accepts any microcontroller in standard 40-pin DIP whose V<sub>CC</sub> and ground are pins 40 and 20, respectively
- Parasitic serial interface to built-in circuitry via a single microcontroller I/O pin
- Special wake-up pattern for invoking added functionality
- Proven gas-tight socket contacts

# **PACKAGE OUTLINE**



PIN ASSIGNMENTS (\ indicates condition low.)
All pins pass through except for:

Pin 20 - Ground

Pin 40 - Vcc

Any pin except for 20 and 40 can be user-configured for added functionality by closing the appropriate shorting pads of the Super Socket with solder.

# CIRCUIT DESCRIPTION

DS131x Super Sockets are 40-pin, 0.6-inch wide DIP sockets with built-in CMOS circuitry that adds new functions to existing microcontroller-based systems. The circuits within the Super Socket are special versions of a 1-Wire peripheral integrated circuit designed to support parasitic communication on a single I/O pin of the microcontroller.

The Super Socket accepts any 40-pin, single-chip microcontroller with V<sub>m</sub> and ground on pins 40 and 20, respectively. When mated with a microcontroller, the Super Socket provides access to its built-in, 1-Wire chip by means of a wake-up pattern that is sent via a single bidirectional I/O pin on the microcontroller. As a result, the chip resides as a parasite on an I/O pin without encumbering the pin's normal function.

The DS131x is an effective upgrade option for previously-designed, single-chip systems and requires only slight software modification.

#### **OPERATION**

Each Super Socket incorporates a special 1-Wire peripheral chip with some features deleted to support parasitic operation. Table 1 below summarizes the functions associated with each Super Socket along with its built-in, 1-Wire embedded chip.

# SUPER SOCKET STANDARD VERSIONS Table 2

Part Number	Description	Embedded Chip
DS1310-00	4Kbit NVSRAM	DS2413
DS1311-00	4Kbit NVSRAM w/ Timekeeper	DS2414

A special ROM mask configures all chips of this type to have a common 64-bit code that is used as a wake-up pattern in parasitic communication.

The DS2413 and DS2414 are special versions of the DS2403 and DS2404 1-Wire peripherals, respectively. The unique aspects of the DS2413 and DS2414 are described in this data sheet. The user should refer to the DS2403 and DS2404 data sheets for basic 1-Wire operational information.

The DS241x part embedded within the DS131x socket functions identically with its standard 1-Wire counterpart with the exception that Match is the only valid 1-wire command. Read, Skip, Search and Presence Detect, which are used in the Super Sockets, have been ROM-masked out of the DS2413/14. This prevents the DS131x from responding to one of these 8-bit codes when noise on the I/O pin happens to emulate one of these commands. In order to have a known wake-up pattern, all DS131x devices were given the same 64-bit code. This code also allows identical single-chip microcontroller systems to be programmed with the same code changes residing in all systems, thus making manufacturing a large number of identical units much simpler from a software standpoint.

The DS131x remains transparent until the 1-Wire Match command has been issued. The DS241x then checks the ID type, serial number and CRC byte that follow this command. If a match is established, then the DS241x looks for a second command on the I/O pin to be sent. This command will be a Read Scratch, Write Scratch, Copy Scratch to Secure Memory, or Read Secure Memory. When one of these commands has been issued, the DS241x responds with the appropriate action. If this format is not followed exactly, the DS241x will wait in a null state for the microcontroller to issue a 1-Wire reset command. (See the DS2403/04 data sheet for this reset format and other operational information.)

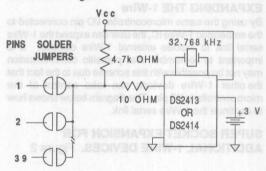
#### STANDARD VERSION

The DS1310-00 and DS1311-00 are standard versions of the Super Socket. These parts have only pins 20 and 40 connected to the built-in, 1-Wire chip. The data line of the 1-Wire device must be connected to an I/O pin, selected by the customer, by closing the appropriate shorting pad on the DS1310-00. The user has complete control over the I/O pin to be designated as the 1-Wire interface. The DS1311-00 uses one of four predefined I/O pins: 4, 8, 24, or 36.

Each pin of the DS1310-00, with the exception of pins 20 and 40, is connected to one side of a shorting pad (see Figure 1). The other side of this pad is connected to the I/O pin of the DS241x 1-Wire serial IC. With this arrangement, the user can select any I/O pin of the microcontroller, with the exception of pins 20 and 40, to be used as the communication line between the microcontroller and the DS1310-00.

Note that only one set of shorting pads will be closed in the DS1310-00. Any other condition will result in unknown data transfers.

# SUPER SOCKET EMBEDDED CIRCUIT Figure 1



#### SPECIAL VERSIONS

Special versions of the DS1310-00 and DS1311-00 are available from Dallas Semiconductor with fixed I/O designations. Please contact Dallas Semiconductor for ordering information on these special versions.

# PARASITIC COMMUNICATION

The 1-Wire interface to the Super Socket's built-in circuitry allows added functionality with minimal impact on existing system hardware in retrofit applications. However, in these situations, the pin used for communication must be appropriately selected in order for the 1-Wire IC to reside as a parasite on that pin.

The following are rules for pin selection:

- 1. The pin to be used for communication must be a bidirectional I/O pin of the microcontroller.
- 2. The pin must be able to be toggled without consequence to existing hardware.
- 3. The pin must be able to time 15*u*s and 60 *u*s signal transitions. This means that the microcontroller must be clocked at some minimum frequency.

Rules #1 and #3 are requirements for communication with the built-in, 1-Wire IC itself. Rule #2 is a consideration for retrofit applications to eliminate the need for hardware change.

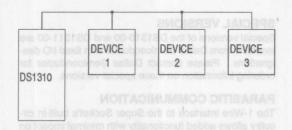
Examples of pins used in typical application which can also serve as the communication line include those used for interface to keyboards and/or displays, as well as those used as data lines to external serial or parallel peripheral devices.

Note that there is a 4.7K pull-up resistor inside the DS131x that is connected to the data line of the built-in, 1-Wire IC (see Figure 1).

## **EXPANDING THE 1-Wire**

By using the same microcontroller I/O pin connected to the embedded 1-Wire IC, the user can expand the 1-Wire serial link to include external 1-Wire devices. It is important to remember that parasitic communication may not be possible with this scheme due to the fact that the other 1-Wire devices can take control of the microcontroller's I/O pin. The diagram below shows how to continue the 1-Wire serial link.

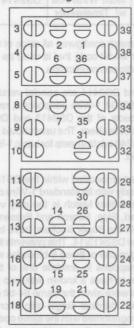
# SUPER SOCKET EXPANSION FOR ADDITIONAL 1-WIRE DEVICES. Figure 2



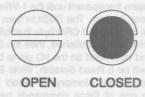
### JUMPERING INSTRUCTIONS

Identify the pin of the microcontroller to be used for communication. Locate the shorting pads of the DS131x that correspond to the selected microcontroller pin. Use the jumper guide to locate these pads (see Figure 3). Close these pads by soldering them together with a droplet of solder (see Figure 4). The Super Socket is now ready for installation and use in the desired hardware. Plug in any 40-pin microcontroller (with +5 on pin 40 and ground on pin 20) whose software has been modified for use with the 1-Wire interface.

# JUMPER GUIDE Figure 3



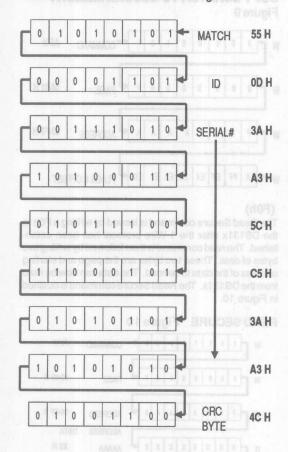
# JUMPER PADS Figure 4



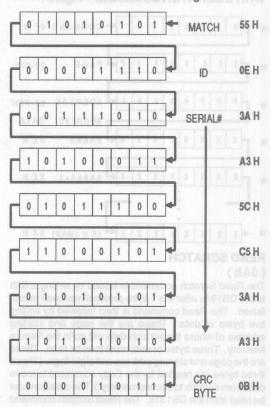
# 1-WIRE COMMANDS

Only the Match 1-Wire command is enabled in the DS241x. Skip, Read, Search, and Presence Detect are disabled on the DS241x for use in the Super Socket. The Match command must be sent to the Super Socket's embedded IC followed by a one-byte type ID, a six-byte fixed serial number, and a one-byte CRC. This protocol is given in Figures 5 and 6. Once the 1-Wire protocol has been established, the functions of the DS241x are available. A flow diagram for the DS131x is shown in Figure 14. Figures 15-19 are the timing diagrams for Write One, Write Zero, Read Data, Interrupt, and Reset Pulse for the 1-Wire.

# DS1310 MATCH COMMAND Figure 5



# DS1311 MATCH COMMAND Figure 6



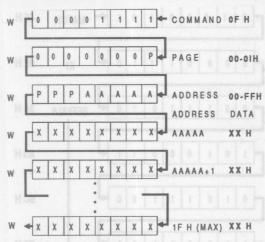
### **COMMAND MODE**

The command mode is the second layer of protocol that must be met before any data can be exchanged between the microcontroller and the Super Socket's embedded IC.

The second layer protocol consists of a command byte followed by the appropriate action. There are four valid command codes: Write Scratch, Read Scratch, Copy Scratch to Secure, and Read Secure. These commands are described separately in the following text.

# WRITE SCRATCH (0Fh)

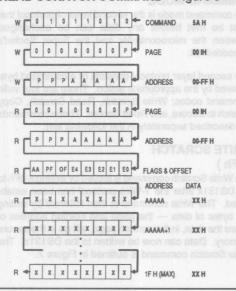
The Write Scratch command is issued by writing a 0Fh to the DS131x after the 1-Wire protocol has been established. The Write command is then followed by writing two bytes of data — the page and starting address of where the data, in the scratch page, will go in the secure memory. Data can now be written to the DS131x. The Write Scratch command is outlined in Figure 7.



# READ SCRATCH (5Ah)

The Read Scratch command is issued by writing a 5Ah to the DS131x after the 1-Wire protocol has been established. The Read command is then followed by writing two bytes of data. These are the page and starting address of where the scratch data will go in the Secure Memory. Three bytes of data must then be read. These are the page and starting address and eight flags. (These three bytes are needed for the Copy command to move data from scratch to secure memory.) The data can now be read from the DS131x. The Read Scratch command is outlined in Figure 8.

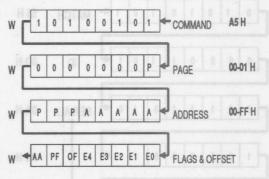
# **READ SCRATCH COMMAND** Figure 8



### ( NON )

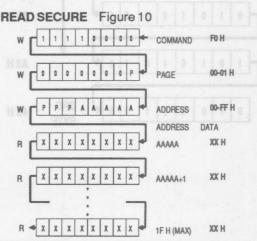
The Copy Scratch to Secure Memory command is issued by writing a A5h to the DS131x after the 1-Wire protocol has been established. The Copy command is then followed by writing three bytes of data. These are the page and starting address and flags that were read from the Read Scratch command. After the last bit of these three bytes is received, the copy will take place using these three bytes as a starting and ending page, as well as the address of where to copy the scratch to. The Copy Scratch to Secure Memory command is outlined in Figure 9.

# COPY SCRATCH TO SECURE MEMORY Figure 9



# (F0h)

The Read Secure command is issued by writing a F0h to the DS131x after the 1-Wire protocol has been established. The read command is then followed by writing two bytes of data. These two bytes are the page and starting address of the data to be read. The data can now be read from the DS131x. The Read Secure command is outlined in Figure 10.

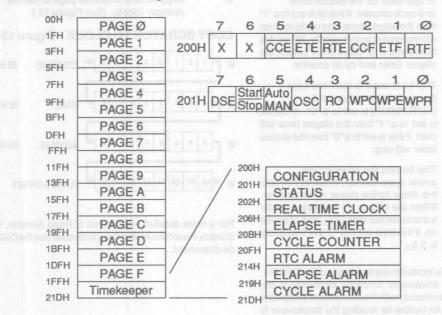


The timekeeper in the DS1311 is located in a special page of secure memory in the DS2414. A number of control bits are associated with this timekeeper. These are located in the first byte of the timekeeper's memory space. The control bit assignment, timekeeping memory map and data memory map are shown in Figure 11.

The timekeeper is a series of binary counters. The data in the timkeeper registers are accumulated binary counts from the time power was applied and the oscillator was turned on.

NOTE: DS1310 has only 16 pages of secure memory. There is no Timekeeping page.

# RTC CONTROL REGISTER Figure 11



200 H					
0	RTF	FUNCTION Real time clock interrupt flag. When this bit is a "1" a real time alarm has occurred. This bit is cleared only after bit 0, 1 and 2 of this register are all read.	5	CCE\	Real time interrupt enable. When this bit is set to a "0" the real time alarm interrupt will be enabled.
1	ETF	Elapse time interrupt flag. When this bit is a "1" an elapse time alarm has occurred. This bit is cleared only after bit 0, 1 and 2 of this register are all read.	7 201 H	Unused	
2	CCF	Cycle counter interrupt flag. When this bit is a "1" a cycle counter alarm has occurred. This bit is cleared only after bit	0	WPR	Permanentwrite protectreal time clock bit. This bit if set to a "1" will write protect the real time clock and real time alarm registers permanently.
3	RTE\	0, 1 and 2 of this register are all read.  Real time interrupt enable. When	1	WPE	Permanent write protect elapse timer alarm registers permanently.
4	ETE\	this bit is set to a "0" the real time alarm  Real time interrupt enable. When this bit is set to a "0" the real time alarm	2	WPC	Permanent write protect cycle counter bit. This bit if set to a "1" will write protect the cycle counter and cycle counter alarm registers permanently.
					alaimiegisters permanently.

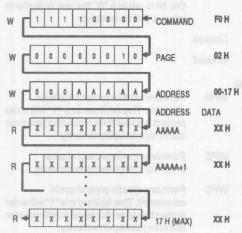
5

- 3 RO This bit must be set to a "1" to read data or timekeeper register if any of the write protect bits have been set.
- 4 OSC This bit sets the mode of operation for the elapse timer and cycle counter. If this bit is a "0" then the clock oscillator will be stopped.
- 5 AUTO/ This bit sets the mode
  MAN\ of operation for the elapse timer
  and cycle counter. If this bit is set to a "1"
  then the elapse timer and cycle counter
  will increment automatically. When this
  bit is set to a "0" bits 6 and 7 control the
  elapse timer and cycle counter.
- START/ This bit is used to start and stop STOP\ the elapse timer when bit 5 (AUTO/MAN\) is set to a "0". If this bit is set to a "1" then the elapse timer will start. If this is set to a "0" then the elapse timer will stop.
- 7 DSEL This bit sets the delay for the power cycle counter. When this bit sets the delay forthe power cycle counter. When the bit is a "1" the cycle counter is incremented after 123±2mS of power up. If this bit is set to a "0" the time delay is 3.5+.

## READING

The timekeeper is located in a special page of the DS2414. Reading of the timekeeper functions identically to the reading of secure memory with the exception of the special page address. An outline for reading the timekeeper is shown in Figure 12.

# **READ CLOCK** Figure 12

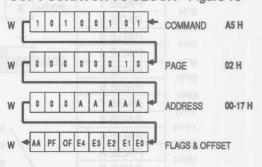


# WRITING

Writing data to the timekeeper involves three steps. These steps are outlined below:

- Write the timekeeper data to scratch memory. (See Figure 7.)
- Read scratch memory to get offset and flags. (See Figure 8.)
- Copy scratch to special page of secure memory (clock). (See Figure 13.)

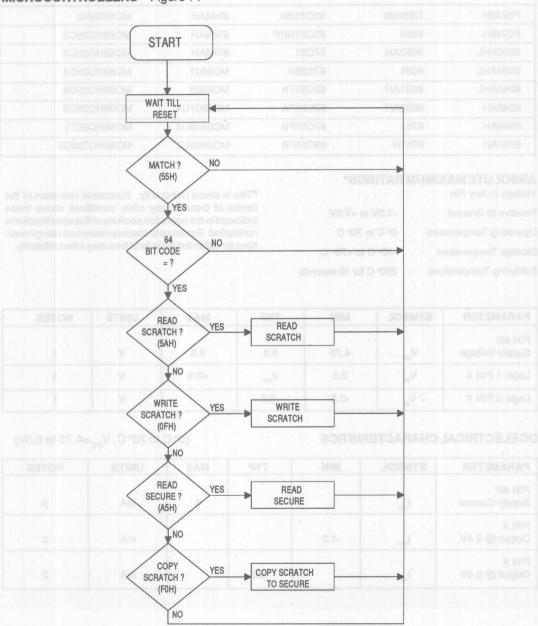
# COPY SCRATCH TO CLOCK Figure 13



For a more detailed explanation of Read Scratch, Write Scratch, Read Secure and Copy to Secure, see the DS2403/04 data sheet.

The DS131x responds to commands as shown in the flow diagram in Figure 14.

COMPATIBLE
MICROCONTROLLERS Figure 14



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that can be used. If the desired microcontroller is not on this list, it can still be used if it comes in a 40-pin DIP with Vcc on pin 40 and ground on pin 20, and if it has a single bidirectional I/O pin.

P8748H	DS5000	80C31BH	8044AH	MC6805R2
P8749H	8051	80C51BHP	8344AH	MC68HC05C2
8035AHL	8052AH	87C51	8744AH	MC68HC05C3
8039AHL	8031	8752BH	MC6801	MC68HC05C4
8040AHL	8031AH	83C51FA	MC6803	MC68HC05C8
8048AH	8032AH	87C51FA	MC6801U4	MC68HC05C9
8049AH	8751	87C51FB	MC6803U4	MC68HC05T1
8050AH	8751H	83C51FB	MC6805U2	MC68HC705C8

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage in Any Pin

Relative to Ground

-1.0V to +7.0V

Operating Temperature

0° C to 70° C

Storage Temperature

-40° C to +70° C

Soldering Temperature

260° C for 10 seconds

\*This is stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 40 Supply Voltage	V <sub>cc</sub>	4.75	5.0	5.5	v	1
Logic 1 PIN X	V <sub>IH</sub>	2.2	V <sub>cc</sub>	+0.3	V	1
Logic 0 PIN X	V <sub>IL</sub>	-0.3	+0.8	m / 370	V	1

# **DCELECTRICAL CHARACTERISTICS**

(0° C to 70° C, V<sub>cc</sub>=4.75 to 5.5v)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 40 Supply Current	I <sub>cc</sub>		0880 880088	5	mA	3
PIN X Output @ 2.4V	I <sub>OH</sub>	-1.0		OH)	mA	2
PIN X Output @ 0.4V	l <sub>oL</sub>	10	4.0	831 YF	mA	2

# CAPACITANCE

(Ta=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance PIN X	C <sub>IN</sub>	5	pF	

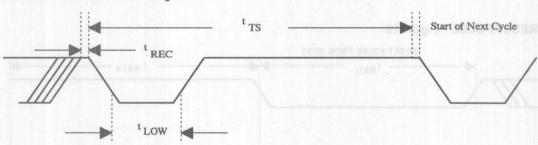
# ACELECTRICAL CHARACTERISTICS:

1-WIREINTERFACE

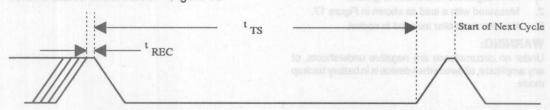
(0° C to 70° C; V<sub>cc</sub>=5.0V+/-10%)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Time Slot	T <sub>TS</sub>	60	120		μѕ	
Recovery Time	T <sub>REC</sub>	1		DET FOR	μѕ	
Low Time	T <sub>LOW</sub>	1	15		μs	
Reset Time High	T <sub>RSTH</sub>	N		480	μѕ	/
Reset Time Low	T <sub>RSTL</sub>			480	μѕ	1

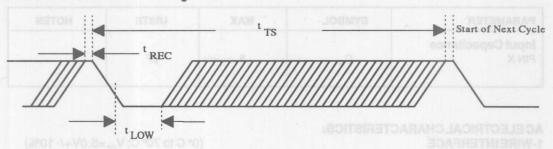
# WRITE ONE TIME SLOT Figure 15

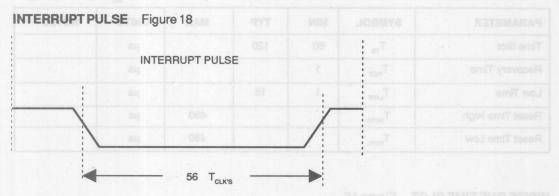


# WRITEZEROTIMESLOT Figure 16

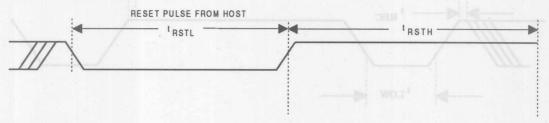


# **READ DATA TIME SLOTS** Figure 17





# **RESET PULSE** Figure 19



# NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 17.
- 3. No microcontroller inserted in socket.

### WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

# 5

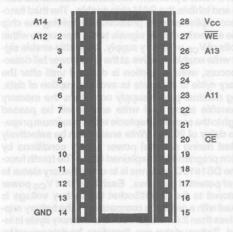
# **DALLAS**SEMICONDUCTOR

# DS1613C Partitioned SmartSocket 256K

#### **FEATURES**

- Accepts standard 32K x 8, CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Unconditionally write protects all of memory when V<sub>CC</sub> is out of tolerance
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

# **PIN ASSIGNMENT**



28-PIN INTELLIGENT SOCKET

# PIN DESCRIPTION

A14	- Address 14
A12	- Address 12
GND	- Ground
CE	- Conditioned Chip Enable
A11	- Address 11
A13	- Address 13
WE	- Conditioned Write Enable
Vcc	- Switched Vcc

All pins pass through except 20, 28, and 27.

#### DESCRIPTION

The DS1613C SmartSocket is a 28-pin, 0.6 inch wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts a 32K x 8 JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that in-

advertent write cycles do not corrupt program and special data space.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pins 28, 27 and 20 for RAM control. All other pins are passed straight through to the socket receptacle. Pins 1, 2, 23, and 26 are address inputs used to set memory partitions.

# **OPERATION**

The DS1613C SmartSocket performs five circuit functions required to battery backup a CMOS memory. First. a switch is provided to direct power from the battery or V<sub>CC</sub> supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power-fail detection. Power-fail detection occurs between 4.75 volts and 4.5 volts. The DS1613C constantly monitors the V<sub>CC</sub> supply. When V<sub>CC</sub> falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable and write enable signals to the memory to within 0.2 volts of V<sub>CC</sub> or battery supply. If the chip enable signal or write enable is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal and write enable will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. Write enable can be selectively inhibited during nominal power supply conditions by partition programming explained later. The fourth function the DS1613C performs is to check battery status to warn of potential data loss. Each time that Vcc power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1613C SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery backup the battery with the highest voltage is selected for use. If one battery fails,

the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mA/hr capacity, making the total 70 mA/hr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the V<sub>CC</sub> pin. In order to read the cell potential, apply V<sub>CC</sub> and then remove power. The cell potential will then be available on pins 28, 27 and 20.

# **PARTITION PROGRAMMING MODE**

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11-A14. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is determined by the size of the memory. For example, a 32K x 8 memory would be divided into 16 partitions of 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1613C to inhibit WE from going low whenever A11 A12 A13 A14=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 16 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

ш	п	н	8	ı	B
v	۰	۰	-	7	
ø	9				
ı		a	·	7	

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER																								
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

ABLE 2:	PARTITION REG	ISTER MAPPING	
Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>14</sub> A <sub>13</sub> A <sub>12</sub> A <sub>11</sub> )
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111 tug
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101 A
A13	BIT 24	PARTITION 14	1110 sonat
A14	BIT 24	PARTITION 15	1111

# **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE

SOLDERING TEMPERATURE

-0.5V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

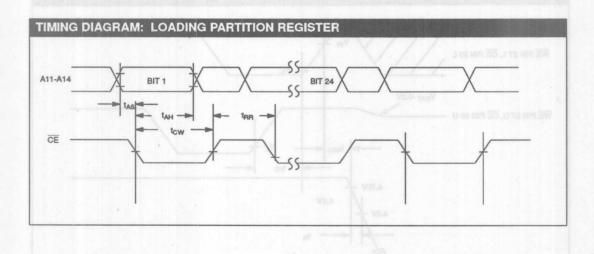
RECOMMENDED DC OF	PERATING CO	NDITIONS	(0°C TO	70°C)		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Voltage	Vcc	4.75	5.0	5.5	٧	1, 3
Logic 1	VIH	2.2		V <sub>CC</sub> + 0.3	V	1, 3
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1,3

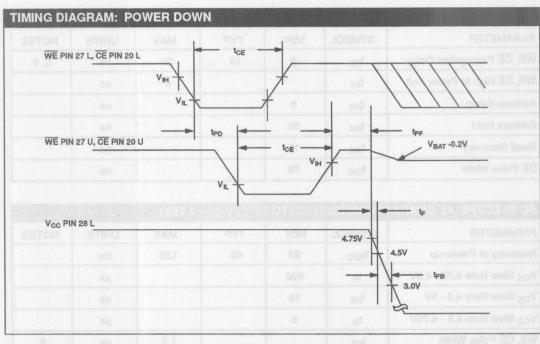
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Current	Icc	sectoral/Len	iting 9	5	mA	3, 4, 5
Pin 28 U Supply Voltage	V <sub>cco</sub>	V <sub>CC</sub> -0.2	RAR	25 TIE	V	3, 7
Pin 28 U Supply Current	Icco	- Homm	FAS	150	mA STA	3, 7
Pin 20 L CE, Pin 27 L WE Input Leakage Address A11-A14	lığ	-1.0	RAR	+1.0	μA <sub>ETA</sub>	3, 4
Pin 20 U CE, Pin 27 U WE Output @ 2.4V	ІОН	-1.0	TA9	\$8.718	mA	2, 3
Pin 20 U CE, Pin 27 U WE Output @ 0.4V	loL	LITTON 6	RAR	4.0	mA	2, 3
Pin 20 U Output Pin 27 U Output	V <sub>OLH</sub>	V <sub>CC</sub> -0.2 V <sub>BAT</sub> -0.2	PAP	BIT 22 BIT 23	V 17A	3
Pin 28 U Battery Current	I <sub>BAT</sub>	e MOITIT	RAS	at ma	μА	3
Pin 28 U Battery Voltage	V <sub>BAT</sub>	2	3	3.6	V sta	3

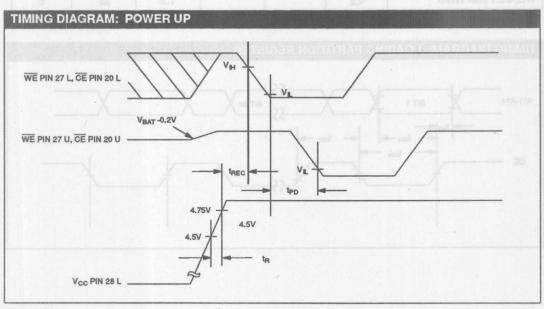
CAPACITANCE (t	$_{A}=25^{\circ}C$	<b>(</b> )					
PARAMETER	1101	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	pert	CIN	FI NOM	PAR	5	pF 8tA	3
Output Capacitance Pin 27 U, Pin 20 U		C <sub>OUT</sub>		RAR	7	pF	3

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
WE, CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	2,8
WE, CE High to Power Fail	tpF	1		0	ns	
Address Setup	t <sub>AS</sub>	0		of all	ns	
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	10			ns	100 EVV
CE Pulse Width	tcw	75			ns	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-up	tREC	25	80	125	ms	
V <sub>CC</sub> Slew Rate 4.75 - 4.5V	t <sub>F</sub>	300			μs	
V <sub>CC</sub> Slew Rate 4.5 - 3V	t <sub>FB</sub>	10			μs	
V <sub>CC</sub> Slew Rate 4.5 - 4.75V	t <sub>R</sub>	0			μs	
WE, CE Pulse Width	tcE			1.5	μs	6







# WARNING

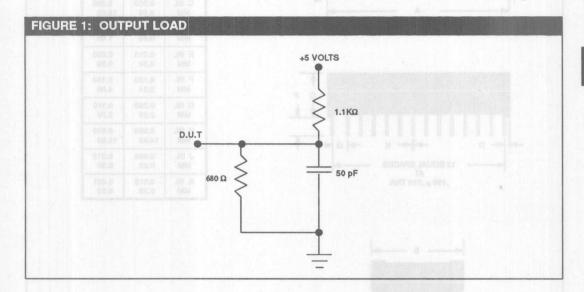
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source as exposed voltage pins are present.

#### NOTES

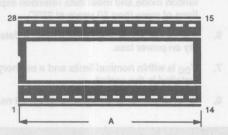
- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 1.
- Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
- 4. No memory inserted in the socket.

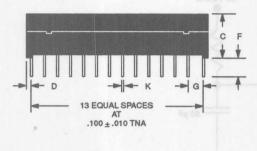
- I<sub>BAT</sub> is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
- t<sub>CE</sub> maximum must be met to ensure data integrity on power loss.
- V<sub>CC</sub> is within nominal limits and a memory is installed in the socket.
- 8. Input pulse rise and fall times equal 10 ns.

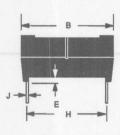


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#### DS1613C INTELLIGENT SOCKET 28 PIN (FOR 600 MIL DIP)







PKG	28-	PIN
DIM	MIN	MAX
A IN.	1.380 35.05	1.420 36.07
B IN.	0.690 17.53	0.720 18.29
C IN.	0.350	0.395
MM	8.89	10.03
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120 3.04	0.160 4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

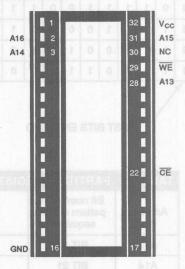
# DALLAS

#### DS1613D Partitioned SmartSocket 1M

#### **FEATURES**

- Accepts standard 128K x 8, CMOS static RAM
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Unconditionally write protects all of memory when V<sub>CC</sub> is out of tolerance
- Write protects selected blocks of memory regardless of V<sub>CC</sub> status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

#### **PIN ASSIGNMENT**



32-PIN SOCKET (600 MIL)

#### **PIN DESCRIPTION**

CE	- Conditioned Chip Enable
WE	- Conditioned Write Enable
NC	- No Connection on Socket
Vcc	Bottom-top Side is V <sub>CC</sub> - Switched V <sub>CC</sub> for 32-pin RAM
GND	Ground

GND - Ground A13-A16 - Address Lines

All pins pass through except 22, 29, 30 and 32.

#### DESCRIPTION

The DS1613D SmartSocket is a 32-pin, 0.6 inch wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts 128K x 8 byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The Smart-Socket monitors incoming  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to uncondi-

tionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space.

Using the SmartSocket saves printed circuit board spacing since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pin 22, 29, 30, and 32 for RAM control. All other pins are passed straight through to the socket receptacle. Pins 2, 3, 28, and 31 are address inputs used to set memory partitions.

5

The DS1613D is exactly the same as the DS1613C with the exceptions that the DS1613D has 32 pins and the DS1613C is 28 pins and the address and control signals are on different pin numbers and locations. The upper order address lines used to set the memory partitions also differ because of the density of RAM for the Smart-Socket. Tables 1 and 2 illustrate the pattern match required for partitioning of the DS1613D. See the DS1613C data for all additional technical details and specifications.

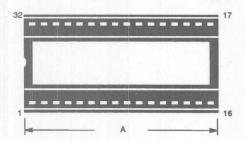
			-		-		-			100	44	10	40	4.4	45	10	47	40	40	00	04	00	000	101
	1	2	3	4	5	6	/	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

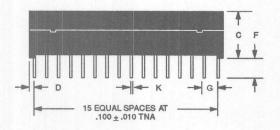
FIRST BITS ENTERED

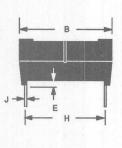
LAST GROUP ENTERED

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>16</sub> A <sub>15</sub> A <sub>14</sub> A <sub>13</sub> )
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

#### DS1613D INTELLIGENT SOCKET 32 PIN (FOR 600 MIL DIP)

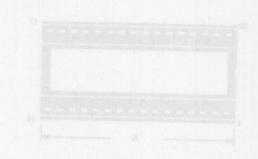






PKG	32-	PIN
DIM	MIN	MAX
A IN. MM	1.580 40.13	1.620 41.15
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.410
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.39	0.035 0.89
F IN.	0.120 3.04	0.160 4.06
G IN.	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012
K IN.	0.015	0.021

SECOND THE LUGENT SOCKET 32 PIN GOR 500 MIL DIP







PAR PROPERTY

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

## **Timekeeping**

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

Type of Interface	Product Name and Number	NV SRAM Bytes	Cycle Times	Special Features
	Real Time Clock DS1287	50		Replaces MC 146818A; MS-DOS
Multiplexed Address/Data Bus	RAMified Real Time Clock DS1387, DS1397	4K	385ns	compatible; programmable interrupts, square wave output. DS13XX, DS14XX, and DS15XX meet MCA and EISA NVRAM
	RAMified Real Time Clock DS1488, DS1497, DS1587	8K		requirements. DS1587 includes silicon serial number.
	Watchdog Timekeeper DS1286	50	150ns	CPU watchdog; programmable
Parallel Interface	RAMified Watchdog Timekeeper DS1386-8, DS1386-32, DS1486	8K/32K/128K	120ns, 150ns	interrupts; square wave output; wake up interrupts.
Bytewide SRAM Bus	NV Timekeeper RAM DS1642, DS1643, and DS1644	2K/8K/32K	120ns, 150ns	PIN compatible with MK48T02 and MK48T08. JEDEC bytewide RAM pin compatible.
	SmartWatch/RAM DS1216B, C, D	2K→ 512K		Timekeeper built into a socket; mated SRAM converts to
Conventional Bytewide SRAM and EPROM Bus with	SmartWatch/ROM DS1216E, F	(EPROM) 8K→ 512K		NVRAM.
Phantom Interface	NV SRAM with Phantom Clock DS1243Y, DS1244Y, DS1248Y	8K/32K/128K	120ns, 150ns, 200ns	NV SRAM packaged with timekeeper.
Serial Interface	Elapsed Time Counter DS1603	No RAM		Vcc active counter and continuous counter.
	Real Time Clock Chip DS1285	50		Replaces MC 146818A, MS-DOS
Multiplexed Address/Data Bus	RAMified Real Time Clock Chip DS1385, DS1395	4K	385ns	compatible; programmable interrupts; square wave output. Meets MCA and EISA NVRAM requirements. DS1585 includes
	RAMifiedReal Time DS1485, DS1585	8K		silicon serial number.
Parallel Interface	Watchdog Timekeeper Chip DS1283, DS1284	50	150ns	Programmable interrupts; square wave output. DS1284 provides battery backup circuitry for SRAM DS1283 provides 2.5 -5.5 volt operation.
Conventional Bytewide SRAM and EPROM Bus Controller with Phantom Interface	Phantom Time Chip DS1215	external		Battery backup circuitry for SRAM. Add-in real time clock uses same SRAM/EPROM signals.
3-Wire Serial	Serial Timekeeper Chip DS1202	24		2.0-5.5 volt operation; serial I/O for minimum pin count.
Interface	Elapsed Time Counter Chip DS1602	No RAM		Vcc active counter and continuous counter.
3-Wire or 1-Wire Serial Interface	EconoRAM Time Chip DS2404	512		Time of day, elapsed time, power on cycle counter, silicon number.

	RAMilled Watchdop Timotecner DS1386-8, DS1396-32, DS1486	120ns, 150ns	

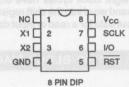
# **DALLAS**SEMICONDUCTOR

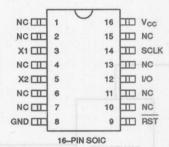
### DS1202, DS1202S Serial Timekeeping Chip

#### **FEATURES**

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0-5.5 volt full operation
- Uses less than 300 nA at 2 volts
- Single-byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL-compatible (V<sub>CC</sub> = 5V)
- Optional industrial temperature range -40°C to +85°C

#### **PIN ASSIGNMENT**





#### PIN DESCRIPTION

NC - No Connection

X1, X2 - 32,768 kHz Crystal Input

GND - Ground RST - Reset

I/O - Data Input/Output

SCLK - Serial Clock
V<sub>CC</sub> - Power Supply Pin

#### DESCRIPTION

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified by using

synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) RST (Reset), (2) VO (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

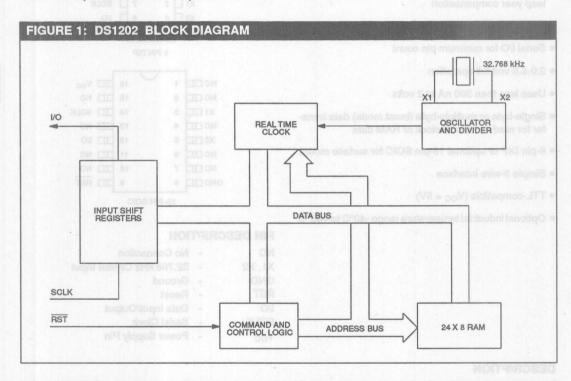
#### **OPERATION**

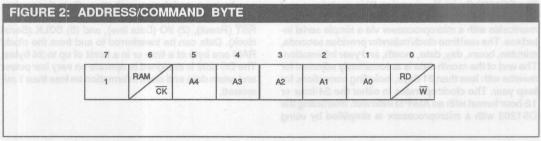
The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, RST is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read or input data for a write.

The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

#### **COMMAND BYTE**

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is zero, further action will be terminated. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).





#### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RST input high. The RST input serves two functions. First, RST turns on the control logic which allows access to the shift register for the address/command sequence. Second, the RST signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. All data transfer terminates if the RST input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

#### **DATA INPUT**

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

#### **DATA OUTPUT**

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as RST remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

#### **BURST MODE**

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specified clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM registers.

#### CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

#### **CLOCK HALT FLAG**

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is

stopped and the DS1202 is placed into a low-power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic 0, the clock will start.

#### **AM-PM/12-24 MODE**

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

#### WRITE PROTECT REGISTER

Bit 7 of write protect register is the write protect bit. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

#### **CLOCK/CALENDAR BURST MODE**

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

#### RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

#### **RAM BURST MODE**

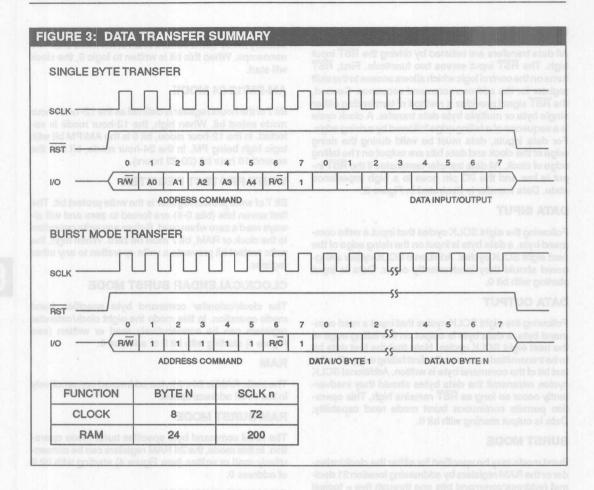
The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

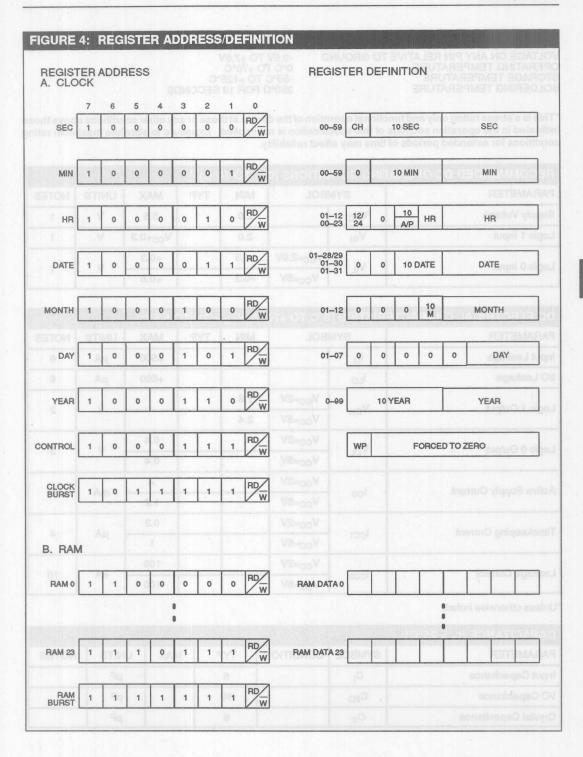
#### REGISTER SUMMARY

A register data format summary is shown in Figure 4.

#### **CRYSTAL SELECTION**

A 32.768 kHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.





#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.5V TO +7.0V 0°C TO +70°C -55°C TO +125°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERA	TING COI	NDITIONS (0	°C TO 7	0°C)			
PARAMETER	SY	MBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	1-10	2.0	11 0	5.5	V	<sub>284</sub> 1
Logic 1 Input	V <sub>IH</sub>		2.0		V <sub>CC</sub> +0.3	٧	1
Logic O Input	VIL	V <sub>CC</sub> =2.0V	-0.3		+0.3	- V	REAC
Logic 0 Input		V <sub>CC</sub> =5V	-0.3		+0.8		1

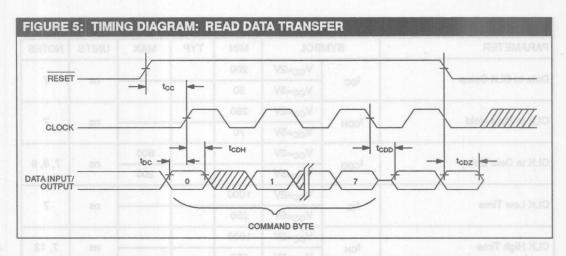
PARAMETER	SY	MBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	Iù V	-10		0 1	+500	μА	6
I/O Leakage	ILO				+500	μА	6
RASY RAS	ren , es	V <sub>CC</sub> =2V	1.6	1 1	0 0	0 1	2
Logic 1 Output	V <sub>OH</sub>	V <sub>CC</sub> =5V	2.4			μΑ μΑ V - V - mA	2
Lorio O Order de PETO PETO DE LA CONTRACTOR DE LA CONTRAC	170	V <sub>CC</sub> =2V	NOR!	T.	0.4	0 1, 1	3
Logic 0 Output	VoL	V <sub>CC</sub> =5V			0.4	μΑ μΑ V - V - mA	3
A.1. 0 . 1.0		V <sub>CC</sub> =2V	Non!		.4		5
Active Supply Current	lcc	V <sub>CC</sub> =5V	W.W.		1.2	1 mA	5
		V <sub>CC</sub> =2V			0.3	V V mA μA	
Timekeeping Current	Icc1	V <sub>CC</sub> =5V			1		4
		V <sub>CC</sub> =2V			100		10
Leakage Current	Icc2	V <sub>CC</sub> =5V	-KT 0	0 0	100	nA	10

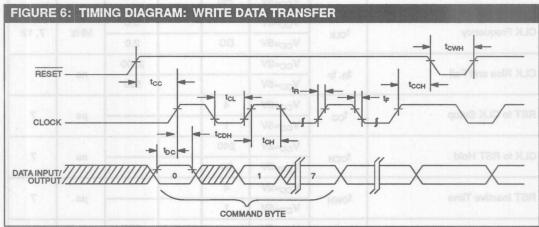
<sup>\*</sup>Unless otherwise noted.

CAPACITANCE (t <sub>A</sub> = 25°	°C)					
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	CI		5		pF	
I/O Capacitance	C <sub>VO</sub>		10	1111	pF	SAAR TERME
Crystal Capacitance	C <sub>X</sub>		6		pF	

PARAMETER	SYI	MBOL	MIN	TYP	MAX	UNITS	NOTES
D		V <sub>CC</sub> =2V	200		*		-
Data to CLK Setup	t <sub>DC</sub>	V <sub>CC</sub> =5V	50	-0-	el el-n	ns	7
		V <sub>CC</sub> =2V	280				-
CLK to Data Hold	tcDH	V <sub>CC</sub> =5V	70			ns	7
CLV to Date Dalou	-Plus 19-	V <sub>CC</sub> =2V	- HOSE   7		800		700
CLK to Data Delay	tcdd	V <sub>CC</sub> =5V	MILL	V a	200	ns	7, 8, 9
CLK Low Time		V <sub>CC</sub> =2V	1000				7
CLK LOW TIME	tcL	V <sub>CC</sub> =5V	250			T IIS	1
CLK High Time		V <sub>CC</sub> =2V	1000			T	7, 12
CLK High Time	tсн	V <sub>CC</sub> =5V	250			- IIS	7,12
CLK Frequency		V <sub>CC</sub> =2V			0.5	MHz	7, 12
CLK Frequency	tCLK	V <sub>CC</sub> =5V	DC		2.0	IVITIZ	7, 12
CLK Rise and Fall	t <sub>R</sub> , t <sub>F</sub>	V <sub>CC</sub> =2V			2000		uene -
CLR RISE and Fall	YR, YF	V <sub>CC</sub> =5V			500	ns  ns  μs  μ	
RST to CLK Setup		V <sub>CC</sub> =2V	4				7
HOT to OLK Setup	tcc	V <sub>CC</sub> =5V	1			ns ns ns ns ns h ns  μs ns	7
CLK to RST Hold		V <sub>CC</sub> =2V	240	+ 53	10-		7
CER to HST Hold	фссн	V <sub>CC</sub> =5V	60	1	TITTE	ns	TURBEAT
RST Inactive Time		V <sub>CC</sub> =2V	4	1	ATTENTA	110	7
TIOT IIIactive Tillie	tcwh	V <sub>CC</sub> =5V	und.			μѕ	
RST to I/O High Z	to-	V <sub>CC</sub> =2V			280	1	7
NOT to I/O riigii Z	tcdz	V <sub>CC</sub> =5V			70	ns	POT

<sup>\*</sup>Unless otherwise noted.





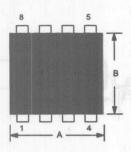
#### NOTES

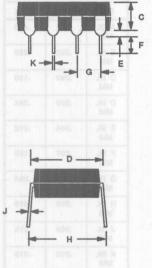
- All voltages are referenced to ground.
- Logic one voltages are specified at a source current of 1 mA at V<sub>CC</sub>=5V and .4 mA at V<sub>CC</sub>=2V, V<sub>OH</sub>=V<sub>CC</sub> for capacitive loads.
- Logic zero voltages are specified at a sink current of 4 mA at V<sub>CC</sub>=5V and 1.5 mA at V<sub>CC</sub>=2V.
- I<sub>CC1</sub> is specified with I/O open, RST set to a logic 0, and clock halt flag=0 (oscillator enabled).
- I<sub>CC</sub> is specified with the I/O pin open, RST high, SCLK=2 MHz at V<sub>CC</sub>=5V; SCLK=500 kHz, V<sub>CC</sub>=2V and clock halt flag=0 (oscillator enabled).
- RST, SCLK, and I/O all have 40KΩ pulldown resistors to ground.

- Measured at V<sub>IH</sub>=2.0V or V<sub>IL</sub>=0.8V and 10 ms maximum rise and fall time.
- Measured at V<sub>OH</sub>=2.4V or V<sub>OL</sub>=0.4V.
- Load capacitance = 50 pF.
- I<sub>CC2</sub> is specified with RST, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
- At power–up, RST must be at a logic 0 until V<sub>CC</sub>≥2 volts. Also, SCLK must be at a logic 0 when RST is driven to a logic one state.
- If t<sub>CH</sub> exceeds 100 ms with <del>RST</del> in a logic one state, then I<sub>CC</sub> may briefly exceed I<sub>CC</sub> specification.

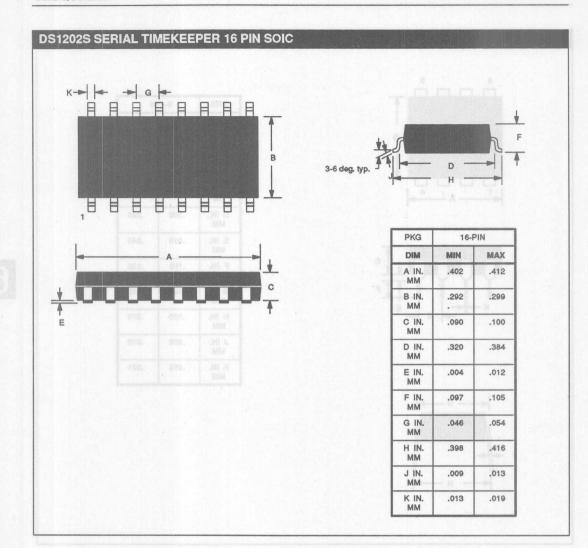








PKG	8-P	IN
DIM	MIN	MAX
A IN. MM	.360	.400
B IN. MM	.240	.260
C IN.	.120	.140
D IN. MM	.300	.325
E IN.	.015	.040
F IN.	.110	.135
G IN.	.090	.110
H IN. MM	.320	.370
J IN. MM	.008	.012
K IN. MM	.015	.021

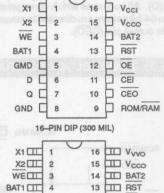


### DS1215 **Phantom Time Chip**

#### **FEATURES**

- · Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and vears
- · Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-reliability applications
- Uses a 32.768 kHz watch crystal
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Space-saving, 16-pin DIP package and SOIC

#### **PIN ASSIGNMENT**





16-PIN SOIC (300 MIL)

#### PIN DESCRIPTION

X1, X2	-	32.768 kHz Crystal Connections
WE	-	Write Enable
BAT1	-	Battery 1 Input
GND	-	Ground
D	-	Data In
Q	-	Data Out
ROWRAM	-	ROM/RAM Select
CEO	-	Chip Enable Out
CEI	-	Chip Enable Input
OE	-	Output Enable
RST	-	Reset
BAT2	-	Battery 2 Input
Vcco	-	
V <sub>CCI</sub>	-	+5 VDC Input
	pins	5 and 8 must be grounded.

#### DESCRIPTION

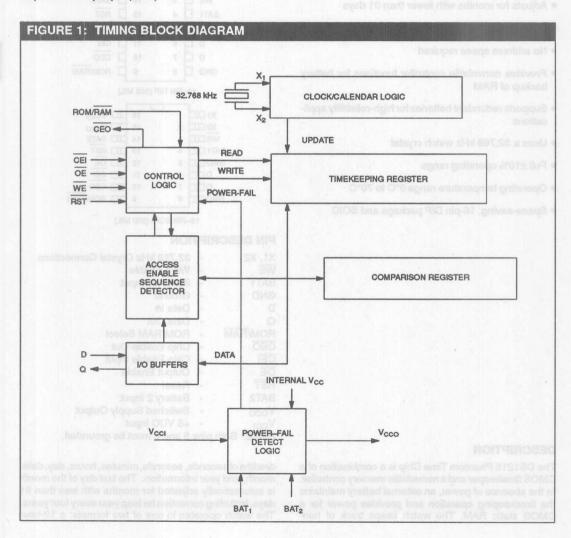
The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

#### **OPERATION**

The block diagram of Figure 1 illustrates the main elements of the Time Chip. Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin (CEO).

After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and CEO remains high during this time, disabling the connected memory.

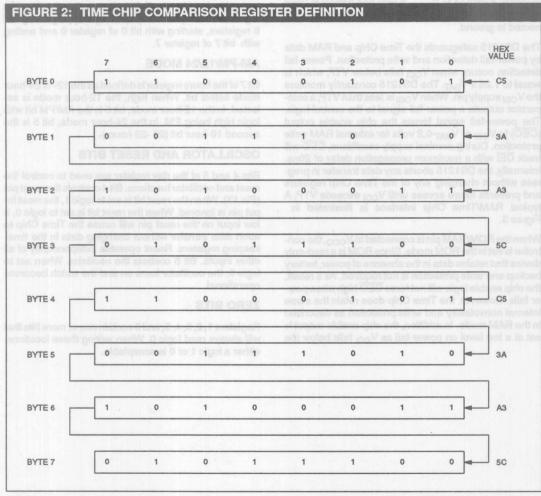
Data transfer to an from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ( $\overline{\text{CEI}}$ ), output enable ( $\overline{\text{OE}}$ ), and write enable ( $\overline{\text{WE}}$ ). Initially, a read cycle using the  $\overline{\text{CEI}}$  and  $\overline{\text{OE}}$  control of the Time Chip starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the  $\overline{\text{CEI}}$  and  $\overline{\text{WE}}$  control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.



When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2.) With a correct match for 64 bits, the Time Chip is enabled and data transfer to or

from the timekeeping registers may proceed. The next 64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of  $\overline{\text{OE}}$  pin or the  $\overline{\text{WE}}$  pin. Cycles to other locations outside the memory block can be interleaved with  $\overline{\text{CEI}}$  cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A 32,768 Hz quartz crystal, Seiko part no. DS-VT-200 or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C<sub>L</sub>) of 6 pF.



#### NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in  $10^{19}$ .

#### NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/RAM select pin. When ROM/RAM is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or  $V_{\rm CCI}$  to  $V_{\rm CCO}$  with a maximum voltage drop of 0.3 volts. The  $V_{\rm CCO}$  output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to  $V_{\rm CCO}$ . If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when  $V_{\rm CCI}$  falls below VTP, which is equal to 1.26 x  $V_{\rm BAT}$ . The DS1215 constantly monitors the  $V_{\rm CCI}$  supply pin. When  $V_{\rm CCI}$  is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output  $(\overline{\rm CEO})$  to  $V_{\rm CCI}$  or  $V_{\rm BAT}$ -0.2 volts for external RAM write protection. During nominal supply conditions,  $\overline{\rm CEO}$  will track  $\overline{\rm CEI}$  with a maximum propagation delay of 20ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until  $V_{\rm CCI}$  exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/RAM pin is connected to  $V_{CCO}$ , the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force  $\overline{\text{CEO}}$  high when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as  $V_{CCI}$  falls below the

level of  $V_{BAT}$ . A typical ROM/Time Chip interface is illustrated in Figure 4.

#### TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

#### AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AWPM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 -23 hours).

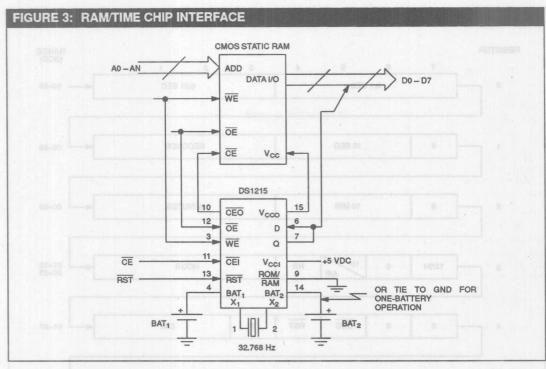
#### **OSCILLATOR AND RESET BITS**

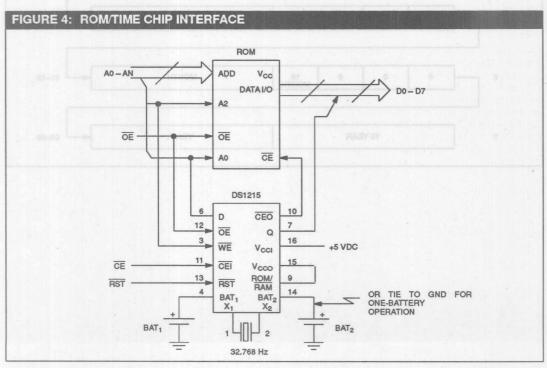
Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the time-keeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

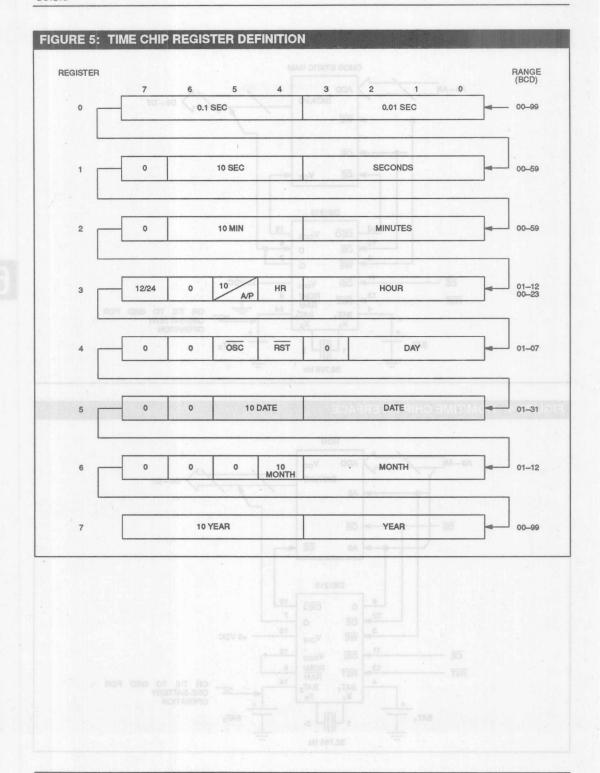
#### **ZERO BITS**

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.









#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND
OPERATING TEMPERATURE
STORAGE TEMPERATURE
SOLDERING TEMPERATURE
O°C TO 70°C
-55°C TO +125°C
260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	coar1 <sub>bac</sub>
Logic 1	VIH	2.2	twc	V <sub>CC</sub> +0.3		eloyo1eth
Logic 0	VIL	-0.3	and the	+0.8	٧	salud eth
V <sub>BAT1</sub> or V <sub>BAT2</sub> Battery Voltage	V <sub>BAT</sub>	2.5	aud-	3.7	V	7

DC ELECTRICAL CHARACTI		Name and Address		OR OTHER DESIGNATION OF THE PERSON OF THE PE		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icci	ons	yaut	5	mA	6
Supply Current V <sub>CCO</sub> = V <sub>CCI</sub> -0.3	I <sub>CCO1</sub>		T must	80	mA	8
Input Leakage	IIL	-1.0	land	+1.0	μА	11
Output Leakage	ILO	-1.0		+1.0	μА	
Output @ 2.4V	loH	-1.0		BELOASIA	mA	2
Output @ 0.4V	loL	T MINA	TORMY?	4.0	mA	2

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V <sub>CC</sub> < 4.5V)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
CEO Output	V <sub>OH1</sub>	V <sub>CCI</sub> or V <sub>BAT</sub> -0.2		Mons	V	9	
V <sub>BAT1</sub> or V <sub>BAT2</sub> Battery Current	I <sub>BAT</sub>	FUN7	TOSMI	1	μА	6	
Battery Backup Current @ V <sub>CCO</sub> = V <sub>BAT</sub> -0.2V	I <sub>CCO2</sub>		Cour	10	μА	10	

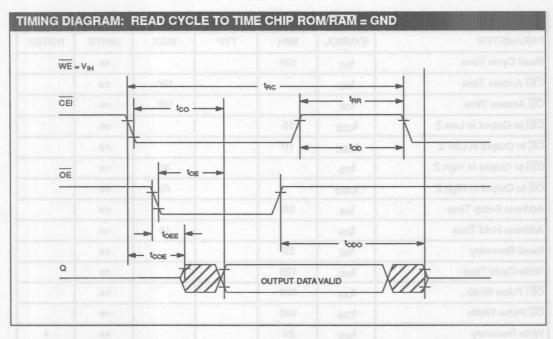
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120		31	ns	TBOARC
CEI Access Time	tco	O GE		100	ns	DMREG.
OE Access Time	t <sub>OE</sub>	reb erli to n	ilterago (sno	100	ns	rde a el el
CEI to Output Low Z	tcoe	10	ellipeds situ	e enolloss	ns	ni belso di partifi
OE to Output Low Z	t <sub>OEE</sub>	10			ns	
CEI to Output High Z	top	10 210		40	ns	
OE to Output High Z	topo	KIM	JOBMA	40	ns	ET BASAR
Read Recovery	t <sub>RR</sub>	20	Vec		ns	BoV Vide
Write Cycle	twc	120	Ver		ns	gio 1
Write Pulse Width	t <sub>WP</sub>	100	JaV		ns	gic 0
Write Recovery	t <sub>WR</sub>	20	Value	egatio	ns	4
Data Setup	t <sub>DS</sub>	40			ns	5
Data Hold Time	t <sub>DH</sub>	10	III I SUL	L. Ballia	ns	5
CEI Pulse Width	tcw	100	J.C. Carrott		ns	o i competitio
RST Pulse Width	t <sub>RST</sub>	200	130		ns	un- Adili
CEI Propagation Delay	t <sub>PD</sub>	5	10	20	ns	2,3
CEI High to Power-Fail	tpF	D214	3	0	ns	SASBIT AND

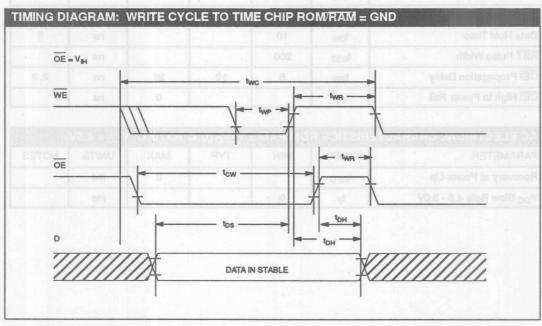
AC ELECTRICAL CHARACTERISTICS ROM/RAM = GND (0°C TO 70°C, V <sub>CC</sub> > 4.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t <sub>REC</sub>			2	ms	
V <sub>CC</sub> Slew Rate 4.5 - 3.0V	t <sub>F</sub>	0			ms	

CAPACITANCE (t <sub>A</sub> = 25	°C)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	ned moto
Output Capacitance	C <sub>OUT</sub>		5	10	pF	V=coaV

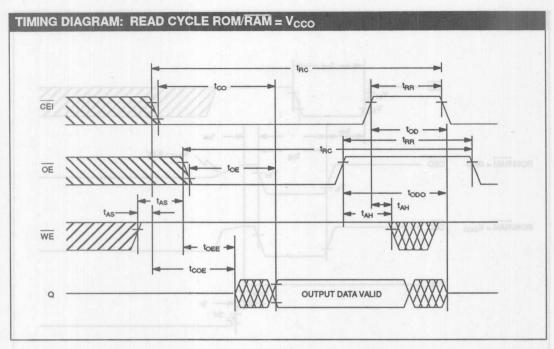
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120			ns	W.
CEI Access Time	t <sub>CO</sub>	ad		100	ns	
OE Access Time	t <sub>OE</sub>	-24	ļ.,	100	ns	ao III
CEI to Output in Low Z	tcoe	10			ns	
OE to Output in Low Z	toee	10			ns	
CEI to Output in High Z	t <sub>OD</sub>		(C)-tress-	40	ns	155
OE to Output in High Z	topo			40	ns	-
Address Setup Time	t <sub>AS</sub>	20		1	ns	
Address Hold Time	t <sub>AH</sub>			10	ns	
Read Recovery	t <sub>RR</sub>	20		4- 807 -	ns	
Write Cycle Time	twc	120	100		ns	0
CEI Pulse Width	tcw	100	- 112	Y	ns	
OE Pulse Width	tow	100			ns	
Write Recovery	t <sub>WR</sub>	20			ns	4
Data Setup Time	t <sub>DS</sub>	40	AT ST SJ	Po avisi	ns	5
Data Hold Time	t <sub>DH</sub>	10			ns	5
RST Pulse Width	trest	200			ns	30
CEI Propagation Delay	t <sub>PD</sub>	5	10	20	ns	2,3
CEI High to Power Fail	tpF			0	ns	3W

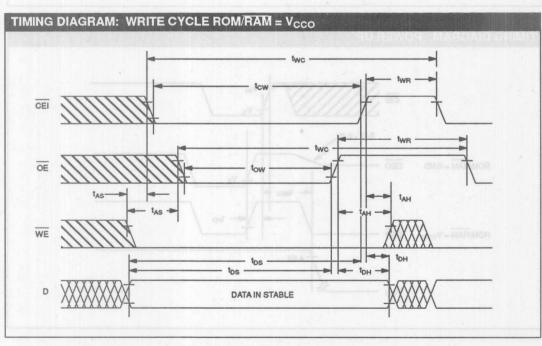
AC ELECTRICAL CHARACTERISTICS ROM/RAM = V <sub>CCO</sub> (0°C TO 70°C; V <sub>CC</sub> < 4.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t <sub>REC</sub>		Apl	2	ms	
V <sub>CC</sub> Slew Rate 4.5 - 3.0V	t <sub>F</sub>	0		1	ms	

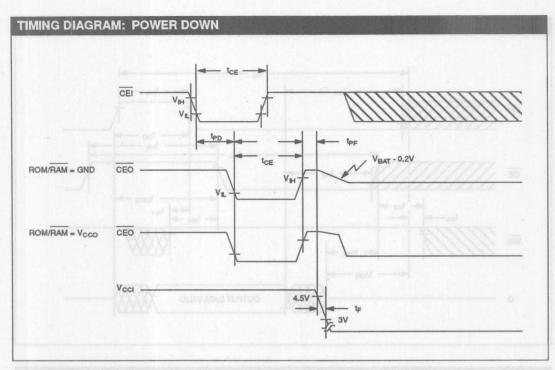


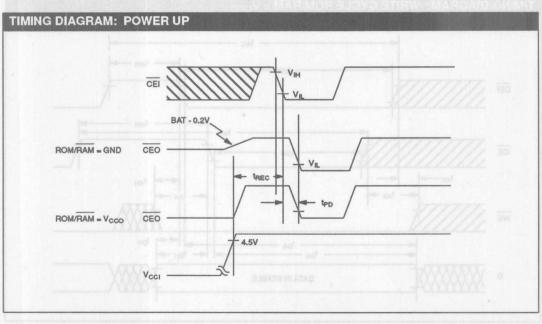


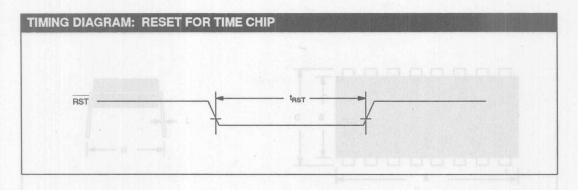










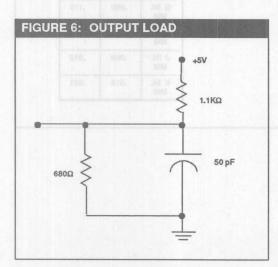


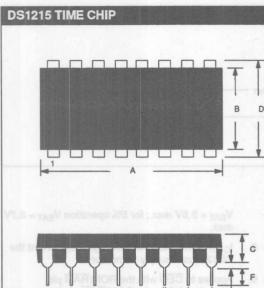
#### NOTES

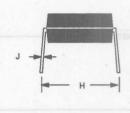
- All voltages are referenced to ground.
- 2. Measured with load shown in Figure 6.
- 3. Input pulse rise and fall times equal 10ns.
- t<sub>WR</sub> is a function of the latter occurring edge of WE or CE in RAM mode, or OE or CE in ROM mode.
- t<sub>DH</sub> and t<sub>DS</sub> are functions of the first occurring edge of WE or CE in RAM mode, or OE or CE in ROM mode.
- 6. Measured without RAM connected.
- 7. Trip point voltage for power-fail detect.  $V_{TP} = 1.26 \times V_{BAT}$ . For 10%  $V_{CC}$ = 5V + 10% operation

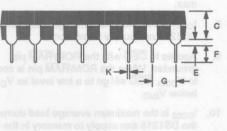
 $V_{BAT}$  = 3.5V max.; for 5% operation  $V_{BAT}$  = 3.7V max.

- I<sub>CC01</sub> is the maximum average load current the DS1215 can supply to memory.
- Applies to CEO with the ROWRAM pin grounded. When the ROM/RAM pin is connected to V<sub>CCO</sub>, CEO will go to a low level as V<sub>CCI</sub> falls below V<sub>BAT</sub>.
- I<sub>CC02</sub> is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
- Applies to all input pins except RST. RST is pulled internally to V<sub>CCI</sub>.









all famous	and the same	L minned
PKG	16-	PIN
DIM	MIN	MAX
A IN.	.740	.780
B IN. MM	.240	.260
C IN.	.120	.140
D IN. MM	.300	.325
E IN. MM	.015	.040
F IN.	.110	.140
G IN. MM	.090	.110
H IN. MM	.300	.370
J IN. MM	.008	.012
K IN. MM	.015	.021



## 64K NV SRAM with Phantom Clock

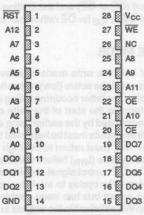
#### **FEATURES**

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 8K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 200 ns access time

#### DESCRIPTION

The DS1243Y 64K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with a built-in real time clock. The DS1243Y has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{\rm CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

#### **PIN ASSIGNMENT**



28-PIN ENCAPSULATED PACKAGE (720 MIL EXTENDED)

#### **PIN DESCRIPTION**

A <sub>0</sub> -A <sub>12</sub>		Address Inputs
CE	edi pi	Chip Enable
GND	grin.	Ground
DQ <sub>0-</sub> DQ <sub>7</sub>	10 1	Data In/Data Out
Vcc		Power (+5V)
WE	Wa.	Write Enable
OE	111-1	Output Enable
NC	01 147	No Connect
RST	10.04	Reset

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

#### **RAM READ MODE**

The DS1243Y executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

#### **RAM WRITE MODE**

The DS1243Y is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in today from its falling edge.

#### **DATA RETENTION MODE**

The DS1243Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAM constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

#### PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory. After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

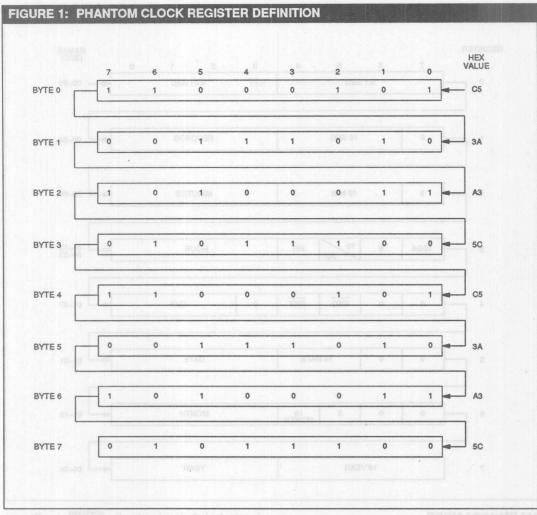
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable (CE), Output Enable (OE), and Write Enable (WE). Initially, a read cycle to any memory location using the CE and OE control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the CE and WE control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the OE pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with CE cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

#### PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

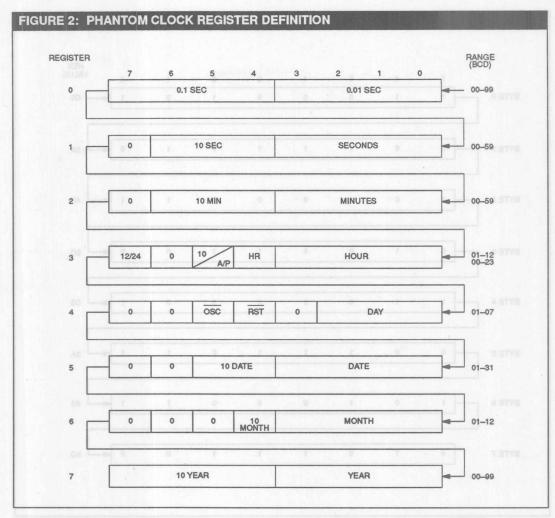
Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.





#### NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10<sup>19</sup>. This pattern is sent to the Phantom Clock LSB to MSB.



### AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AWPM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

### **OSCILLATOR AND RESET BITS**

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit

is set to logic 0, a low input on the  $\overline{RESET}$  pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

### **ZERO BITS**

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO 7.0V 0°C TO 70°C -55°C TO 125°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	egnan		
Input Logic 1	V <sub>IH</sub>	2.2	awa	V <sub>CC</sub> +0.3	Versi	tita Cycle		
Input Logic 0	V <sub>IL</sub>	0.3	9)((8	0.8	V	rite Pulso		

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0	ward	+1.0	μА	12
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0	eaf	+1.0	μА	quieS atr
Output Current @ 2.4V	Гон	-1.0	1 140		mA	CROPT ELE
Output Current @ 0.4V	loL	2.0			mA	D TEST
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10	mA	bao.i tro
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	and the second
Operating Current t <sub>CYC</sub> = 200 ns	I <sub>CC01</sub>		1.6V	85	mA	1313

### DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t <sub>A</sub> = 25°C					E HA	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>VO</sub>		5	10	pF	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	200			ns	THOMAC
Access Time	tACC			200	ns	
OE to Output Valid	toE	veb edito ni too si antis	ilfanego lano	100	ns	ento s al ai
CE to Output Valid	tco	t religiting.	ne may effec	200	ns	ditions fo
OE or CE to Output Active	tcoe	5			ns	5
Output High Z from Deselection	top	E AMERICA	o o de el chaid Lanca ava	100	ns	5
Output Hold from Address Change	t <sub>oH</sub>	5	Vgc		ns	Wet Supp
Write Cycle Time	twc	200	N/H		ns	eigo,l tuc
Write Pulse Width	t <sub>WP</sub>	150	V <sub>IL</sub>		ns	3
Address Setup Time	t <sub>AW</sub>	0			ns	
Write Recovery Time	t <sub>WR</sub>	20		ENPARA	ns	BELLER
Output High Z from WE	topw	AH.	TORWAS	80	ns	5
Output Active from WE	toew	5	3		ns	5
Data Setup Time	t <sub>DS</sub>	80	- oi		ns	4
Data Hold Time from WE	t <sub>DH</sub>	20		-	ns	4

### **AC TEST CONDITIONS**

Output Load: 50 pF + 1TTL Gate

Input Pulse Levels: 0-3V

Timing Measurement Reference Levels

Input: Am 48 1.5V Output: 1.5V Input Pulse Rise and Fall Times: 5 ns

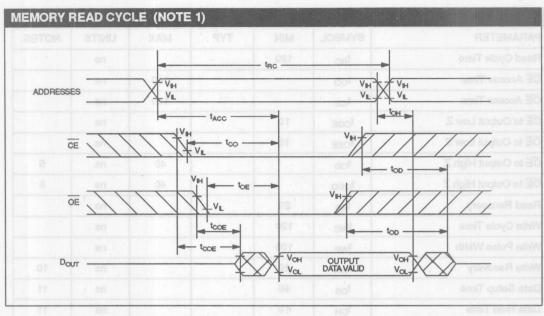
PHANTOM CLOCK AC E	LECTRICAL CH	ARACTE	RISTICS (0°	C 10 70°C,	V <sub>CC</sub> = 4.5	10 5.5V)
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120			ns	
CE Access Time	t <sub>co</sub>			100	ns	
OE Access Time	t <sub>OE</sub>			100	ns	
CE to Output Low Z	tcoe	10	past		ns	
OE to Output Low Z	toee	10	- 00 <sup>1</sup> - 1	W/	ns	
CE to Output High Z	top			40	ns	5
OE to Output High Z	topo		- pg/	40	ns	5
Read Recovery	t <sub>RR</sub>	20	sv./	W	ns	
Write Cycle Time	t <sub>WC</sub>	120	La Book		ns	
Write Pulse Width	t <sub>WP</sub>	100	- Inc.		ns	
Write Recovery	t <sub>WR</sub>	20	<b>P</b>		ns	10
Data Setup Time	t <sub>DS</sub>	40			ns	11
Data Hold Time	t <sub>DH</sub>	10			ns	11
CE Pulse Width	tcw	100		ionnen.	ns	NATIONE
RESET Pulse Width	trst	200			ns	
CE High to Power-Fail	tpF			0	ns	

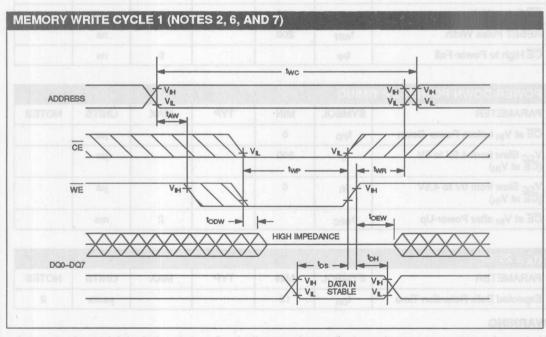
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0	17	777	μѕ	
V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	t <sub>F</sub>	300		1	μs	
V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	t <sub>R</sub>	0	1//	Far	μѕ	
CE at V <sub>IH</sub> after Power-Up	tREC		n- wad	2	ms	

(t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t <sub>DR</sub>	10	- Constant		years	9

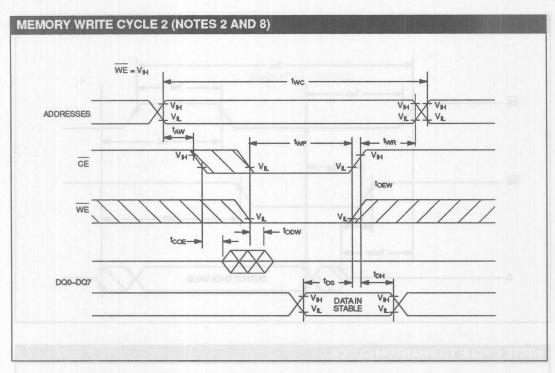
### WARNING

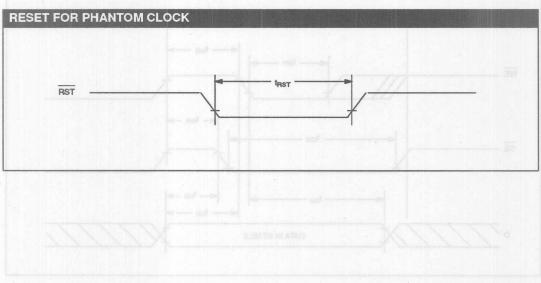
 $Under \, no\, circumstances\, are\, negative\, undershoots, of\, any\, amplitude, allowed\, when\, device\, is\, in\, battery\, backup\, mode.$ 

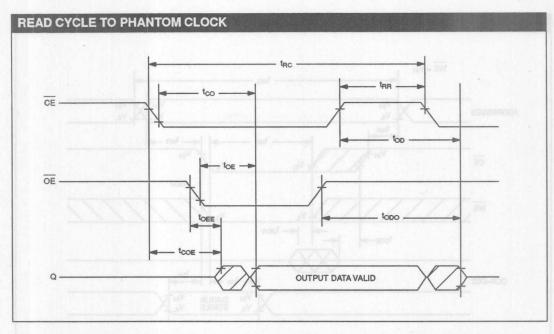


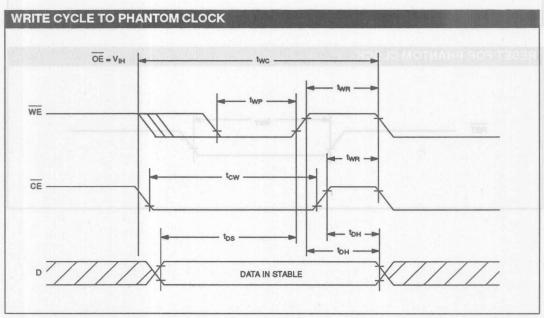


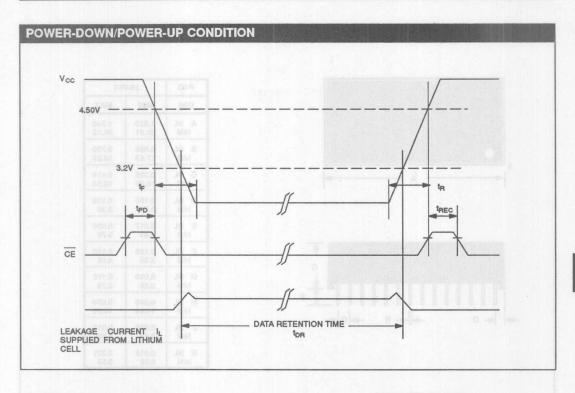










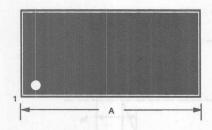


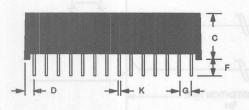
### NOTES

- WE is high for a read cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of <u>CE</u> and <u>WE</u>. t<sub>WP</sub> is measured from the latter of <u>CE</u> or <u>WE</u> going low to the earlier of <u>CE</u> or <u>WE</u> going high
- t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- These parameters are sampled with a 50 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

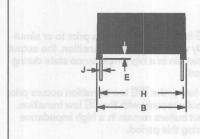
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> with the clock oscillator running.
- t<sub>WR</sub> is a function of the latter occurring edge of WE or CE.
- t<sub>DH</sub> and t<sub>DS</sub> are a function of the first occurring edge of WE or CE.
- 12. RST (Pin1) has an internal pull-up resistor.

### DS1243Y 28 PIN EXTENDED BOTTOM 720 MIL BODY WIDTH (DIMENSION B)





PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015 0.38	0.021





## 256K NV SRAM with Phantom Clock

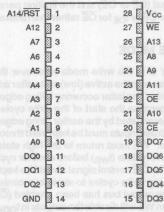
### **FEATURES**

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 32K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

#### DESCRIPTION

The DS1244Y 256K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 32,768 words by 8 bits) with a built-in real time clock. The DS1244Y has a self-contained lithium energy source and control circuitry which constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

### PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE (740 MIL EXTENDED)

### **PIN DESCRIPTION**

100	Address Inputs
rit pi	Chip Enable
N. S.	Ground
OVE	Data In/Data Out
	Power (+5V)
Vel	Write Enable
ride!	Output Enable
0.144	No Connect
8.647	Reset

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

### **RAM READ MODE**

The DS1244Y executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

### **RAM WRITE MODE**

The DS1244Y is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topw from its falling edge.

### **DATA RETENTION MODE**

The DS1244Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAM constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

### PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory. After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

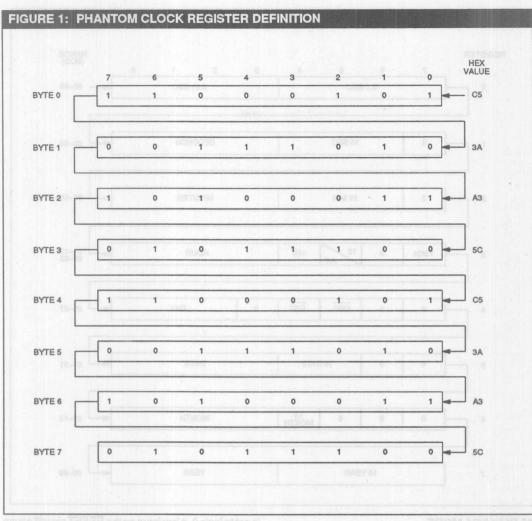
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable (CE), Output Enable (OE), and Write Enable (WE). Initially, a read cycle to any memory location using the CE and OE control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the CE and WE control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the OE pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with CE cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

### PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

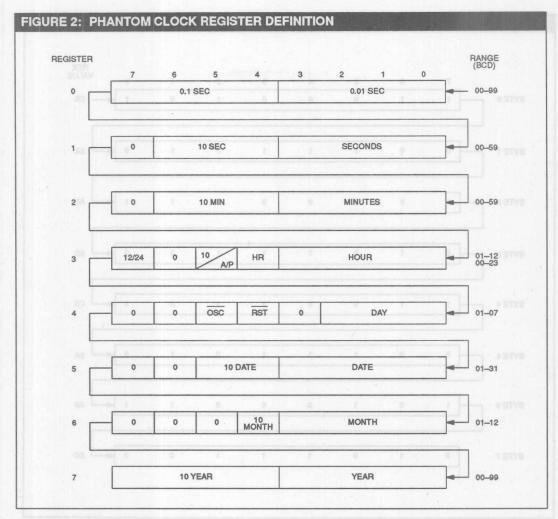
Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.





### NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10<sup>19</sup>. This pattern is sent to the Phantom Clock LSB to MSB.



### AM-PW12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AWPM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

### **OSCILLATOR AND RESET BITS**

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit

is set to logic 0, a low input on the RESET pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

### **ZERO BITS**

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

### 6

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Power Supply Voltage	Vcc	4.5	5.0	5.5	٧		
Input Logic 1	VIH	2.2	No.	V <sub>CC</sub> +0.3	V	nangar.	
Input Logic 0	cos V <sub>IL</sub> (a)	0.3	at I aw	0.8	Vemil	rita Cycla	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	07 IIL	-1.0	word	+1.0	μА	12
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	lio a	-1.0	wso!	+1.0	μА	HitoA forepu
Output Current @ 2.4V	Іон	-1.0	80		mA	Question de la lite
Output Current @ 0.4V	loL	2.0	BQ BQ		mA	CHOY) SIS
Standby Current CE = 2.2V	I <sub>CCS1</sub>		5.0	10	mA O	o rear o
Standby Current CE = V <sub>CC</sub> - 0.5V	I <sub>CCS2</sub>		3.0	5.0	mA	bead load
Operating Current t <sub>CYC</sub> = 200 ns	I <sub>CC01</sub>			85	mA	

### DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>VO</sub>		5	10	pF	

DADAMETED	OVALDOL	DS1244Y-120		DS1244Y-150		DS1244Y-200		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120		150		200		ns	
Access Time	tACC	priveb e	120	fare qu	150	nul best	200	ns	k is ai airi Necesti
OE to Output Valid	t <sub>OE</sub>	oility.	60	eito ve	70	iods el	100	ns	enalithn
CE to Output Valid	tco		120		150		200	ns	I KEC
OE or CE to Output Active	tCOE	5	LANA.	5		5		ns	5
Output High Z from Deselection	t <sub>OD</sub>		40		70		100	ns	5
Output Hold from Address Change	t <sub>oH</sub>	5	22	5	V	5		ns	goJ Avq
Write Cycle Time	twc	120	8.0	150	V	200		ns	god tug
Write Pulse Width	t <sub>WP</sub>	90		100		150		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		0		ns	
Write Recovery Time	t <sub>WR</sub>	20	MIM	20	HAY 8	20		ns	BNARA
Output High Z from WE	topw		40		70		80	ns	5
Output Active from WE	t <sub>OEW</sub>	5	0,1-	5	del l	5		ns	5
Data Setup Time	t <sub>DS</sub>	50	0.1-	60		80	3/25	ns	4
Data Hold Time from WE	t <sub>DH</sub>	20	-	20		20		ns	4

### AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate

Input Pulse Levels: 0-3V

Timing Measurement Reference Levels

Input: 1.5V Output: 1.5V Input Pulse Rise and Fall Times: 5 ns

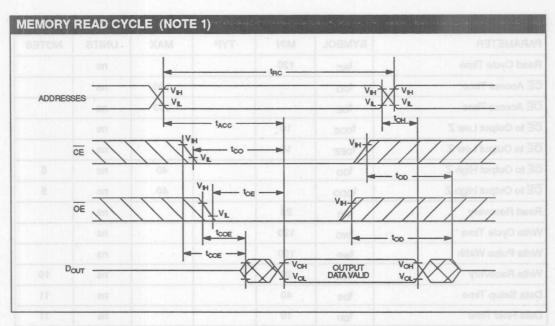
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
			111	IVIAA	ONTO	NOTES
Read Cycle Time	t <sub>RC</sub>	120			ns	
CE Access Time	tco			100	ns	
OE Access Time	toE			100	ns	
CE to Output Low Z	tcoe	10	lace	and the same of th	ns	
OE to Output Low Z	toee	10	- 001	1//	ns	
CE to Output High Z	top			40	ns	5
OE to Output High Z	topo		10 - 11 HV	40	ns	5
Read Recovery	t <sub>RR</sub>	20	44	1//	ns	
Write Cycle Time	twc	120	25		ns	
Write Pulse Width	t <sub>WP</sub>	100	- 1001 m	6	ns	
Write Recovery	t <sub>WR</sub>	20		ocama a lav nik is jumpi	ns	10
Data Setup Time	t <sub>DS</sub>	40			ns	11
Data Hold Time	t <sub>DH</sub>	10			ns	11
CE Pulse Width	t <sub>CW</sub>	100	De la Visa		ns	vy Haire
RESET Pulse Width	t <sub>RST</sub>	200			ns	
CE High to Power-Fail	tpF			0	ns	

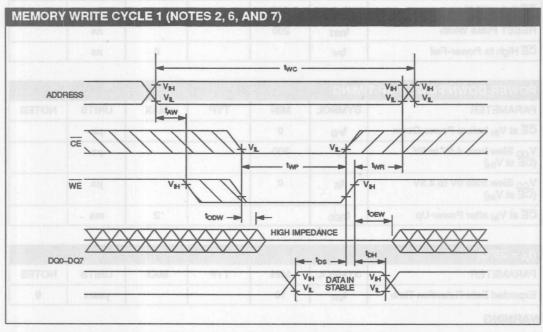
POWER-DOWN/POWER-UP TIMING									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES			
CE at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0	1777	777	μѕ				
V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	t <sub>F</sub>	300	3//		μѕ				
V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	t <sub>R</sub>	0	177	FIN	μs				
CE at V <sub>IH</sub> after Power-Up	tREC		a- wad	2	ms				

(t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t <sub>DR</sub>	10			years	9

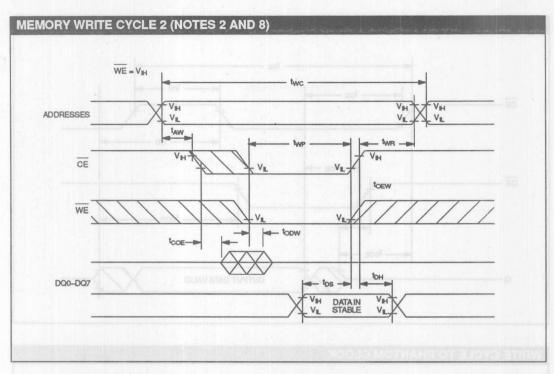
### WARNING

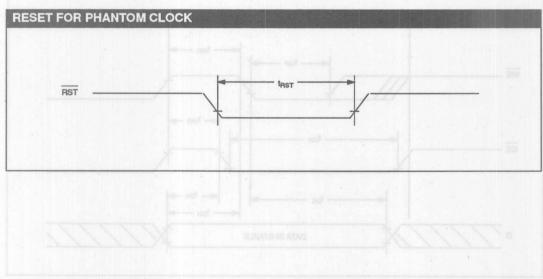
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

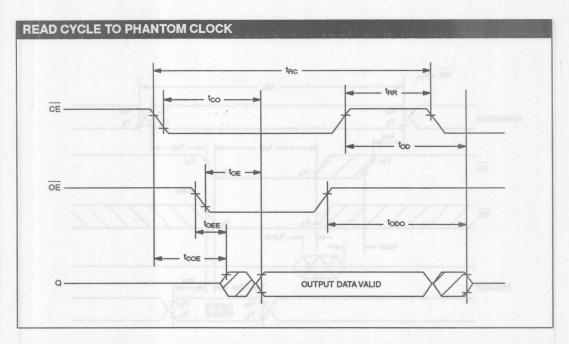


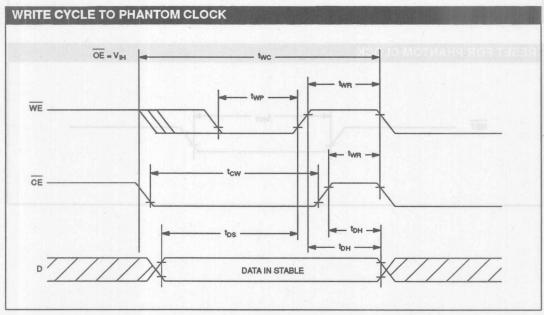


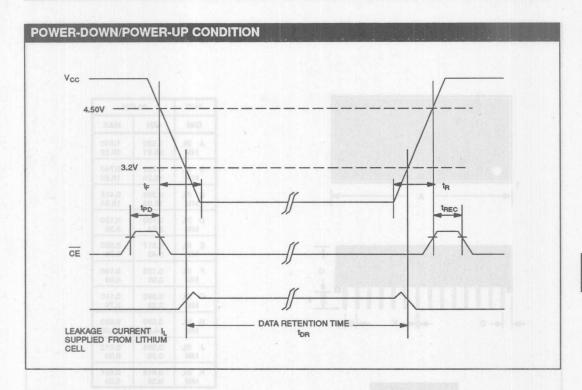










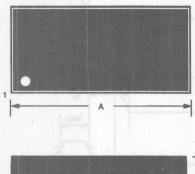


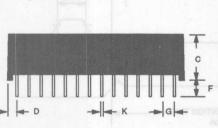
### **NOTES**

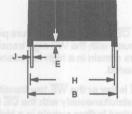
- WE is high for a read cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state
- t<sub>WP</sub> is specified as the logical AND of CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
- t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- These parameters are sampled with a 50 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> with the clock oscillator running.
- t<sub>WR</sub> is a function of the latter occurring edge of WE or CE.
- t<sub>DH</sub> and t<sub>DS</sub> are a function of the first occurring edge of WE or CE.
- 12. RST (Pin1) has an internal pull-up resistor.

### DS1244Y 256K NV SRAM WITH PHANTOM CLOCK







PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.520 38.61	1.540 39.12
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.395 10.03	0.415 10.54
D IN. MM	0.100 2.54	0.130 3.30
E IN.	0.017 0.43	0.030 0.76
F IN.	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021



## 1024K NV SRAM with Phantom Clock

### **FEATURES**

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 128K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

### DESCRIPTION

The DS1248Y 1024K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 128K words by 8 bits) with a built-in real time clock. The DS1248Y has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tol-erance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

### **PIN ASSIGNMENT**

	parameter and the same of the		
RST	1	32	Vcc
A16	2	31	A15
A14	3	30	NC
A12	₫ 4	29 🖺	WE
A7	5	28	A13
A6	6	27	A8
A5	₹ 7	26	A9
A4	3 8	25	A11
АЗ	9	24	OE
A2	10	23 🗓	A10
A1	11	22	CE
AO	12	21 🗵	DQ7
DQ0	13	20 🖺	DQ6
DQ1	14	19 🖺	DQ5
DQ2	15	18	DQ4
GND	16	17 🖺	DQ3

32-PIN ENCAPSULATED PACKAGE (740 MIL FLUSH)

### PIN DESCRIPTION

Junishbo Am		Address Invests
A <sub>0</sub> -A <sub>16</sub>	adi b	Address Inputs
CE	ifus	Chip Enable
GND	90¥	Ground
DQ <sub>0-</sub> DQ <sub>7</sub>	sollo:	Data In/Data Out
Vcc	emp	Power (+5V)
WE	ove	Write Enable
OE	12 (110) 12 (10)	Output Enable
NC	10.00	No Connect
RST	orinto.	Reset

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

### **RAM READ MODE**

The DS1248Y executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which of the 128K bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

### **RAM WRITE MODE**

The DS1248Y is in the write mode whenever the WE and CE signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t<sub>WR</sub>) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topw from its falling edge.

### **DATA RETENTION MODE**

The DS1248Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAM constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

### PHANTOM CLOCK OPERATION

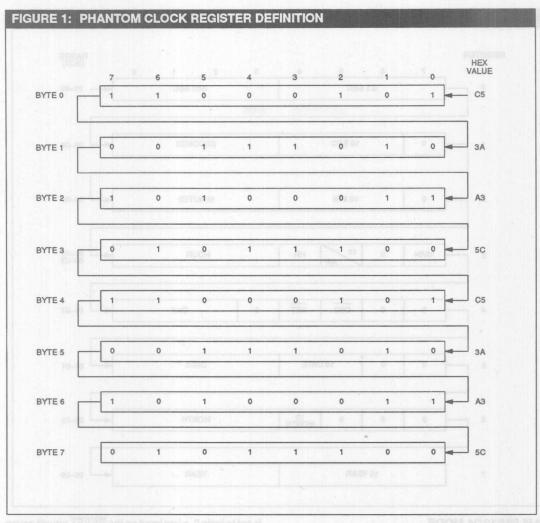
Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory. After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable (CE), Output Enable (OE), and Write Enable (WE). Initially, a read cycle to any memory location using the CE and OE control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the CE and WE control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the OE pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with CE cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

### PHANTOM CLOCK REGISTER INFORMATION

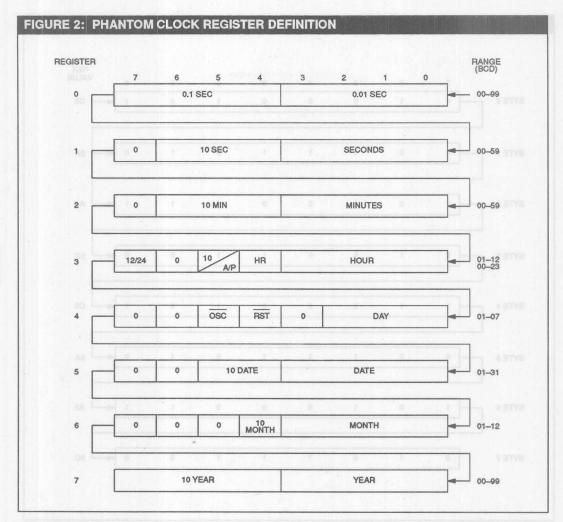
The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.



### NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10<sup>19</sup>. This pattern is sent to the Phantom Clock LSB to MSB.



### **AM-PW/12/24 MODE**

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AWPM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

### **OSCILLATOR AND RESET BITS**

Bits 4 and 5 of the day register are used to control the RESET and oscillator functions. Bit 4 controls the RESET (pin 1). When the RESET bit is set to logic 1, the RESET input pin is ignored. When the RESET bit

is set to logic 0, a low input on the  $\overline{RESET}$  pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

### **ZERO BITS**

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

### 6

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Power Supply Voltage	Vcc	4.5	5.0	5.5	V		
Input Logic 1	VIH	2.2	Bo <sup>-</sup>	V <sub>CC</sub> +0.3	V	egnsri	
Input Logic 0	VIL Dat	-0.3	ir aw	0.8	V	Alley Cycle	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	as lil	-1.0	werend	+1.0	μА	12
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	lio	-1.0	Wao)	+1.0	μА	utpus Acti
Output Current @ 2.4V	Іон	-1.0	901		mA	quies ara
Output Current @ 0.4V	loL	2.0	F   140		mA	Liors am
Standby Current $\overline{CE} = 2.2V$	I <sub>CCS1</sub>		5.0	10	mA	TEST
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	keed tuqu
Operating Current t <sub>CYC</sub> = 200 ns	I <sub>CC01</sub>			85	mA	

### DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t <sub>A</sub> = 25°C						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	
Input/Output Capacitance	C <sub>VO</sub>		5	10	pF	

PARAMETER	SYMBOL	DS1248Y-120		DS1248Y-150		DS1248Y-200		UNITS	NOTES
PARAMETER	STIMBUL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120		150		200		ns	
Access Time	tACC	eveb s	120	operal social	150	eul bais andres	200	ns	a 6 at 6iri Pastenik
OE to Output Valid	toE	aglilie	60	ay afte	70	o aboli	100	ns	prolition
CE to Output Valid	tco		120	ÉWIE	150		200	ns	Marie I
OE or CE to Output Active	tCOE	5	MARIE MARIE	5	Legisal Leve I	5		ns	5
Output High Z from Deselection	top		40		70		100	ns	5
Output Hold from Address Change	t <sub>oH</sub>	5	S.S	5	V	5		ns	goul lugi
Write Cycle Time	twc	120	E.O-	150	V	200		ns	go.J huqn
Write Pulse Width	t <sub>WP</sub>	90		100		150		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		0		ns	
Write Recovery Time	t <sub>WR</sub>	20	NEW	20	WYS	20		ns	BMAHA
Output High Z from WE	topw		40	1.0	70		80	ns	5
Output Active from WE	toew	5	0.1-	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	50	6.1-	60	3	80	VA	ns	4
Data Hold Time from WE	t <sub>DH</sub>	20		20		20	100	ns	4

### AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate

Input Pulse Levels: 0-3V

Timing Measurement Reference Levels

Input: 1.5V Output: 1.5V Input Pulse Rise and Fall Times: 5 ns

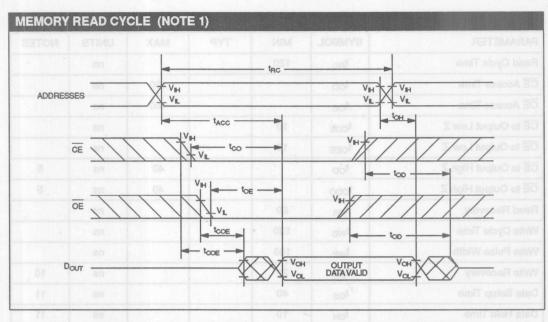
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120			ns	
CE Access Time	tco			100	ns	
OE Access Time	t <sub>OE</sub>			100	ns	
CE to Output Low Z	tcoe	10	- Just -	m-wip]	ns	
OE to Output Low Z	toee	10	- col	1///	ns	
CE to Output High Z	top			40	ns	5
OE to Output High Z	topo	- Marian	10 - m 10 10 10 10 10 10 10 10 10 10 10 10 10	40	ns	5
Read Recovery	t <sub>RR</sub>	20	W/A	1///	ns	
Write Cycle Time	twc	120	les mol		ns	
Write Pulse Width	t <sub>WP</sub>	100	4- sol-		ns	
Write Recovery	t <sub>WR</sub>	20			ns	10
Data Setup Time	t <sub>DS</sub>	40			ns	11
Data Hold Time	t <sub>DH</sub>	10			ns	- 11
CE Pulse Width	tcw	100		STANDED IS	ns	Zelej Kej
RESET Pulse Width	trst	200			ns	
CE High to Power-Fail	tpF			0	ns	

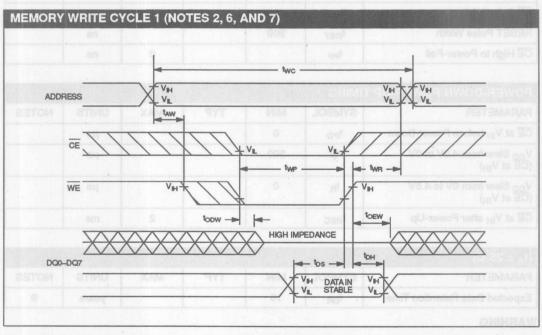
POWER-DOWN/POWER-UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0	177	1777	μѕ	
V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	t <sub>F</sub>	300			μѕ	
V <sub>CC</sub> Slew from 0V to 4.5V (CE at V <sub>IH</sub> )	t <sub>R</sub>	0	17	1 100	μѕ	
CE at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>		-e 2005	2	ms	

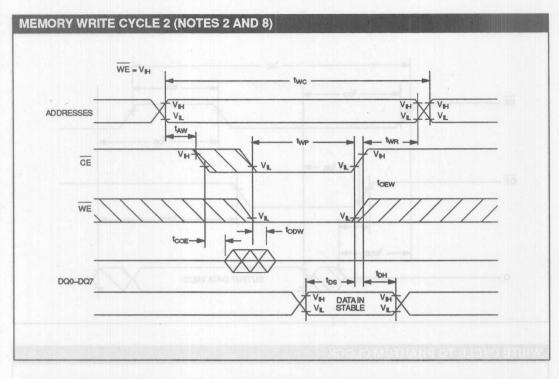
(t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t <sub>DR</sub>	10			years	9

### WARNING

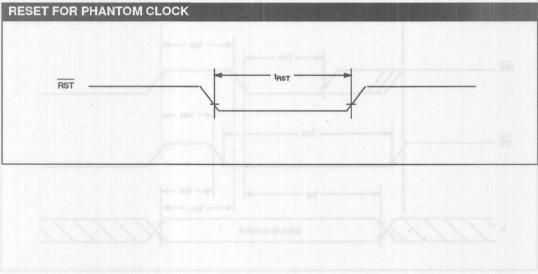
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

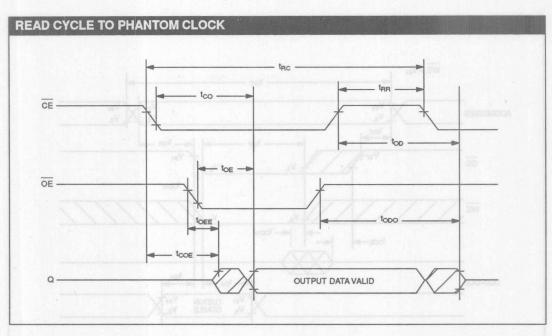


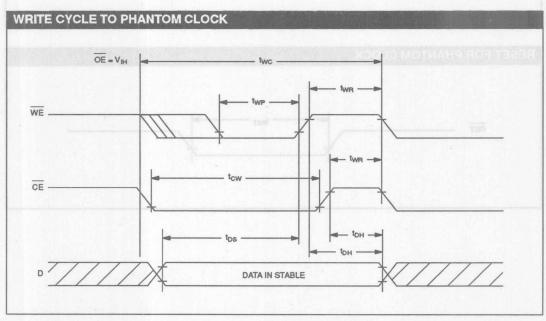


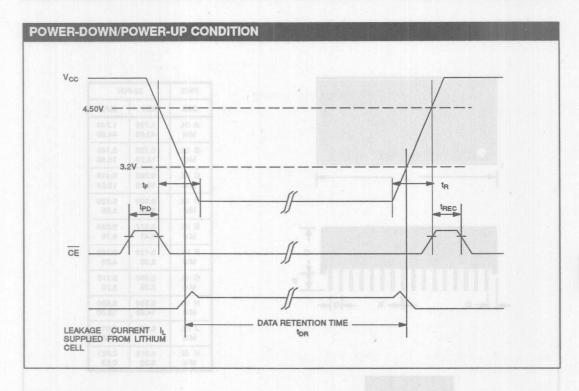


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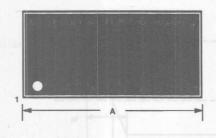


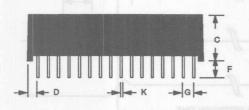
### **NOTES**

- WE is high for a read cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of <del>CE</del> and <del>WE</del>. t<sub>WP</sub> is measured from the latter of <del>CE</del> or <del>WE</del> going low to the earlier of <del>CE</del> or <del>WE</del> going high.
- t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- These parameters are sampled with a 50 pF load and are not 100% tested.
- If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

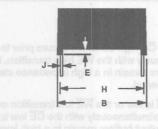
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
- The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> with the clock oscillator running.
- 10. t<sub>WR</sub> is a function of the latter occurring edge of
- 11.  $t_{DH}$  and  $t_{DS}$  are a function of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 12. RST (Pin1) has an internal pull-up resistor.

### DS1248Y 1024K NV SRAM WITH PHANTOM CLOCK





PKG	32-PIN		
DIM	MIN	MAX	
A IN. MM	1.720 43.69	1.740 44.20	
B IN. MM	0.720 18.29	0.740 18.80	
C IN. MM	0.395 10.03	0.415 10.54	
D IN.	0.090 2.29	0.120 3.05	
E IN. MM	0.017 0.43	0.030 0.76	
F IN.	0.120 3.05	0.160 4.06	
G IN. MM	0.090 2.29	0.110 2.79	
H IN.	0.590 14.99	0.630 16.00	
J IN. MM	0.008 0.20	0.012	
K IN.	0.015 0.38	0.021 0.53	



020692 12/12

# **DALLAS**SEMICONDUCTOR

# Watchdog Timekeeper Chip

### **FEATURES**

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function provides notice of real time related occurrences
- Designed for battery operation
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minutes/month at 25°C
- 50 bytes of user nonvolatile RAM
- Optional 28-pin SOIC surface mount package
- $\bullet$  Low-power CMOS circuitry is maintained on less than 1  $\mu A$  in standby mode

### DESCRIPTION

The DS1283 Watchdog Timekeeper Chip is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP or 28-pin SOIC surface mount package. The DS1283 is specifically designed to maintain internal operations from a single low voltage supply. In fact, the only two external components re-

PIN ASSIGNI	WENT				
INTA [	10 9	0	28	] <sup>V</sup> cc	
X1 [	2		27	] WE	
X2 [	3		26	INTB(INTB)	
NC	4		25	VBAT	
A5 [	5		24	RCLR	
A4 [	6		23	SQW	
A3 [	7		22	ŌĒ	
A2 [	8		21	INTP	
A1 [	9		20	CE	
A0	10		19	DQ7	
DQ0	11		18	DQ6	
DQ1	12		17	DQ5	
DQ2	13		16	DQ4	
GND	14	io F	15	DQ3	
		DIP (60	o mil)		
INTA 🗆	1	0	28	□□ Vcc	
X1 🗆	2		27	OD WE	
Х2 🗆	3		26	INTB(INTB)	
NC I	4		25	UD VBAT	
A5 🗆	5		24	RCLR	
A4 🗆	6		23	□□ sow	
АЗ 🗆	7		22	OE OE	
A2 III	8		21	INTP	
A1 🗆	9		20	TI CE	
A0 III	10		19	DQ7	
DQ0 III	11		18	DQ6	
DQ1 III	12		17	DQ5	
DQ2 🗆	13		16	DQ4	
GND 🗆	14		15	DQ3	
788 KHz quart	28-Pin 5	S12839 SOIC (3		- Connections Daine card	

NOTE: Pin 4 must be left disconnected.

quired by the DS1283 are a battery and crystal. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2,  $V_{BAT}$ ,  $V_{CC}$ , and  $\overline{RCLR}$ , see the DS1286 Watchdog Timekeeper data sheet.

### PIN DESCRIPTION

PIN#	NAME	1/0	DESCRIPTION
1	INTA	0	Interrupt Output A
2-3	X1,X2		32.768 KHz Crystal
4	NC	-	No Connection
5-10	A0-A5	l (es	Address Inputs: A5=Pin 5; A0=Pin 10
11	DQ0	1/0	Data Input/Output
12	DQ1	1/0	Data Input/Output
13	DQ2	1/0	Data Input/Output
14	GND		Ground
15	DQ3	1/0	Data Input/Output
16	DQ4	VO	Data Input/Output
17	DQ5	1/0	Data Input/Output
18	DQ6	VO	Data Input/Output
19	DQ7	1/0	Data Input/Output
20	CE	1	Chip Enable
21	INTP	0	Interrupt Output P
22	ŌĒ	0	Output Enable
23	sqw	0	Square Wave
	TABY IN	a	Output
24	RCLR	1	RAM Clear
25	V <sub>BAT</sub>	ggl.	Battery Input
26	INTB (INTB)	0	Interrupt Output B
27	WE	<sup>©</sup> 1	Write Enable
28	Vcc	I	V <sub>CC</sub> Input

### PIN DESCRIPTIONS

X1, X2 – Connections for a standard 32.768 KHz quartz crystal, Daiwa part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuit-

ry is designed for operation with a crystal having a load capacitance (C<sub>L</sub>) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor Part # DS9032.

 $V_{BAT}$  – Battery input for a battery or power supply between 5.5 volts and 2.5 volts. When the DS1283 is powered by the  $V_{BAT}$  pin alone,  $V_{CC}$  and  $V_{BAT}$  must be connected together. When a single supply is used, input and output levels and timing are only guaranteed between the ranges of 4.5 volts and 5.5 volts. In this mode, the active current drain is 2 mA ( $\overline{CE} = V_{IL}$ ), the standby current is 0.5 mA ( $\overline{CE} = V_{IH}$ ), and the data retention mode is less than 1 μA typical and 1.5 μA maximum at 5.5 volts ( $\overline{CE} = V_{BAT}$  - 0.2 volts). These current drain specifications are stated with all outputs unloaded.

 $V_{CC}$  – +5 volt input for connection to the  $V_{CC}$  supply. This supply input is used for inputs and outputs only as the internal functions of the device are powered by the  $V_{BAT}$  pin. The  $V_{CC}$  voltage range should never exceed  $V_{BAT}$  by more than 0.3 volts and  $V_{BAT}$  is normally connected to  $V_{CC}$ . In order to guarantee timing and input/output levels, both  $V_{CC}$  and  $V_{BAT}$  must be between 4.5 and 5.5 volts. However, the DS1283 maintains internal functions with  $V_{CC}$  input as low as 2.5 volts.

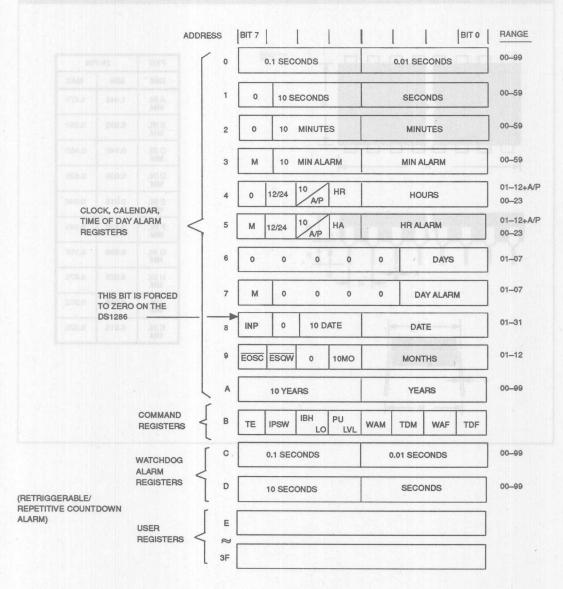
RCLR – The RCLR pin is used to clear (set to logic 1) all 50 bytes of user nonvolatile RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, RCLR must be forced to an input logic 0 (-0.3 to +0.8 volts). The RCLR function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

INTB – Interrupt B on the DS1283 operates identical to interrupt B on the DS1286 except that the sink and source current is limited to 500  $\mu$ Å. This pin should be pushed up or pulled down if not used.

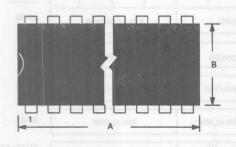
INTP – Interrupt P on the DS1283 was a missing or no connection pin on the DS1286. This interrupt works in the same manner as INTA as programmed by the IPSW bit. However, INTP is also logically ORed with the MSB of the date register (see Figure 1). This bit is called the INP bit on the DS1283 and is forced to zero on the DS1286. When the INP bit (interrupt P bit) is set to logical one, interrupt P will be held active low. When INP is set to logical zero, INTP is always at the same logic state as INTA. This pin is an open drain capable of sinking 4 mA.

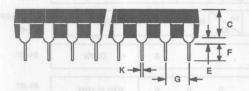


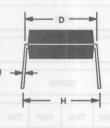




# DS1283 28 PIN DIP

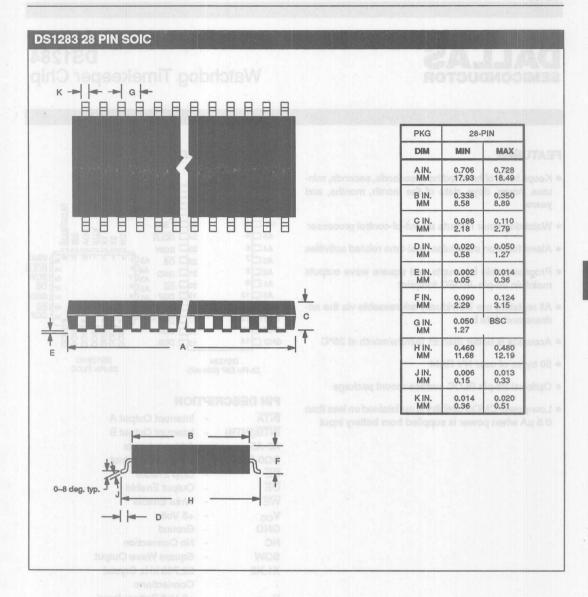






PKG	28-F	PIN	
DIM	MIN	MAX	
AIN. MM	1.445	1.470	
B IN. MM	0.530	0.550	
C IN. MM	0.140	0.160	
D IN. MM	0.600	0.625	
EIN. MM	0.015	0.040	
FIN. MM	0.120	0.145	
G IN. MM	0.090	0.110	
H IN. MM	0.625	0.675	
J IN. MM	0.008	0.012	
KIN. MM	0.015	0.022	





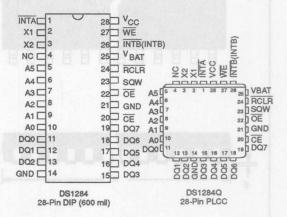


# DS1284 Watchdog Timekeeper Chip

#### **FEATURES**

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- 50 bytes of user NV RAM
- Optional 28-pin PLCC surface mount package
- Low-power CMOS circuitry is maintained on less than 0.5 μA when power is supplied from battery input

#### PIN ASSIGNMENT



#### **PIN DESCRIPTION**

I III DECCI	111011
INTA	- Interrupt Output A
INTB(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
CE	- Chip Enable
OE	- Output Enable
WE	- Write Enable
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
SQW	- Square Wave Output
X1,X2	- 32.768 kHz Crystal
	Connections
VBAT	- +3 Volt Battery Input
RCLR	- RAM Clear

tions other than X1, X2, V<sub>BAT</sub>, and  $\overline{RCLR}$ , see the DS1286 Watchdog Timekeeper data sheet.

#### DESCRIPTION

The DS1284 Watchdog Timekeeper Chip is a self-contained real-time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package or a 28-pin PLCC surface mount package. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descrip-

#### PIN DESCRIPTION

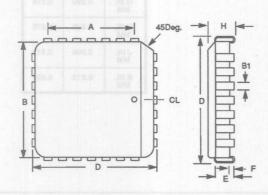
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C<sub>L</sub>) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

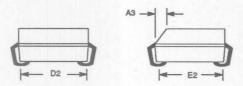
V<sub>BAT</sub> - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to registers containing time, watchdog, alarm, and RAM information is denied is set by internal circuitry as 1.26

x  $V_{BAT}$ . A maximum load of 0.5  $\mu$ A at 25°C in the absence of power should be used to size the external energy source. An optional ground pin is provided for connection to battery negative. This pin should be grounded but can be left floating.

RCLR - The RCLR pin is used to clear (set to logic 1) all 50 bytes of user NV RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, RCLR must be forced to an input logic zero (-0.3 to +0.8 volts) during battery backup mode when VCC is not applied. The RCLR function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

### **DS1284Q 28 PIN PLCC WATCHDOG TIMEKEEPER**

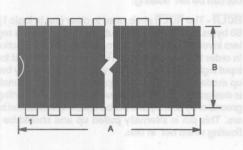


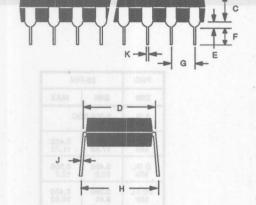


PKG	28-F	PIN		
DIM	MIN	MAX		
AIN.	0.300 BSC			
MM	7.62			
B IN.	0.442	0.462		
MM	17.68	11.73		
D IN.	0.480 12.2	0.500 12.7		
D2 IN.	0.390	0.430		
MM	9.91	10.92		
EIN.	0.090	0.120		
MM	2.29	3.05		
E2 IN.	0.390	0.430		
MM	9.91	10.92		
F IN.	0.015	0.020		
MM	0.38	0.518		
H IN.	0.100 2.54	0.020 0.518		

6







i irimming o trequency	PKG	28-F	PIN
mequance inductor,	DIM	MIN	MAX
w-E by	AIN. MM	1.445	1.470
ige n	B IN. MM	0.530	0.550
is	C IN.	0.140	0.160
i ien	D IN. MM	0.600	0.625
	E IN. MM	0.015	0.040
	F IN.	0.120	0.145
	G IN. MM	0.090	0.110
1	H IN.	0.625	0.675
	J IN. MM	0.008	0.012
0	KIN. MM	0.015	0.022

# DS1285, DS1285Q Real Time Clock

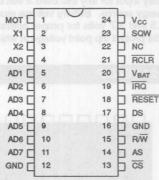
#### **FEATURES**

- Drop-in replacement for IBM AT computer clock/ca-
- Pin configuration closely matches MC146818A
- · Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compen-
- Binary or BCD representation of time, calendar, and
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
- 14 bytes of clock and control registers
- 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
- Time-of-day alarm once/second to once/day
   Periodic rates from 122 μA to 500 ms
- End of clock update cycle
- Optional 28-pin PLCC surface mount package

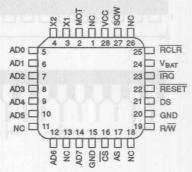
#### DESCRIPTION

The DS1285 Real Time Chip is a direct replacement for the MC146818A in IBM AT computer clock/calendar and other applications. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, VBAT, and RCLR, see the DS1287 data sheet.

#### **PIN ASSIGNMENT**



DS1285 24-PIN DIP DS1285S 24-PIN SOIC



**DS1285Q 28-PIN PLCC** 

#### PIN DESCRIPTION

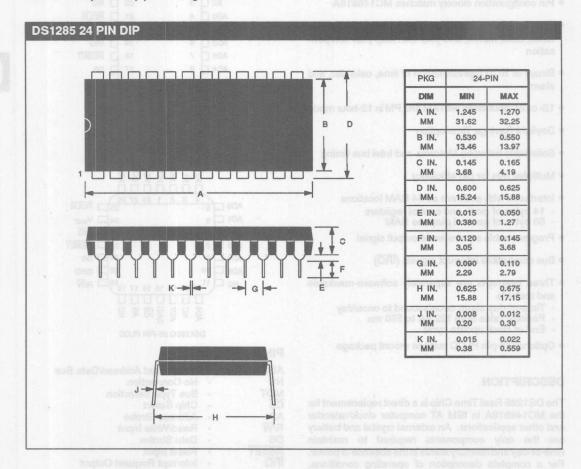
AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
CS	-	Chip Select
AS	-	Address Strobe
R/W	-	Read/Write Input
DS	-	Data Strobe
RESET	-	Reset Input
IRQ	-	
SQW	-	Square Wave Output
V <sub>CC</sub>		+5 Volt Supply
GND	-	Ground
X1,X2		32.768 kHz Crystal Connections
VBAT	-	+3 Volt Battery Input
RCLR	-	RAM Clear

#### PIN DESCRIPTION

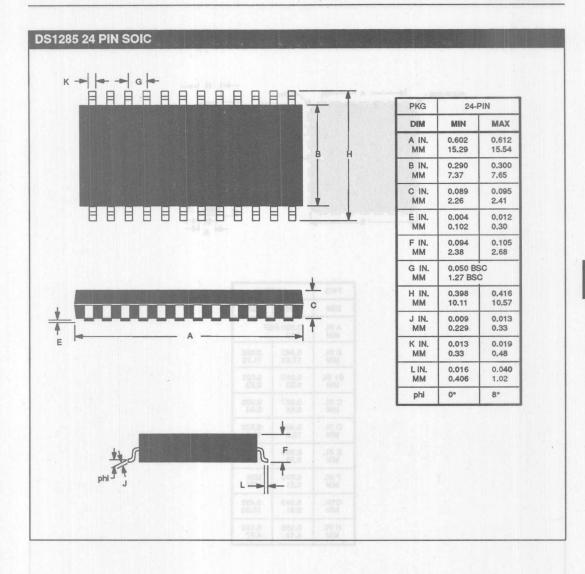
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S, Seiko part number DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. A variable trimming capacitor may be required for extremely high precision timekeeping applications. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V<sub>BAT</sub> - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as  $1.26 \times V_{BAT}$ . A maximum load of .5  $\mu$ A at 25°C in the absence of power should be used to size the external energy source.

RCLR - The RCLR pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V<sub>CC</sub> is not applied. The RCLR function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.







# **DS1285Q 28 PIN PLCC** .010 R (3)0 4 ,45 Deg. PKG 28-PIN MAX DIM MIN 0.300 REF 7.62 A IN. MM B IN. 0.442 17.68 0.462 11.73 B1 IN. MM 0.013 0.33 0.021 0.53 C IN. 0.027 0.033 D IN. 0.480 0.500 E IN. 0.090 0.120 FIN. 0.020 MIN GIN. MM 0.390 0.430 H IN. 0.165 4.19 0.180 4.57

# 6

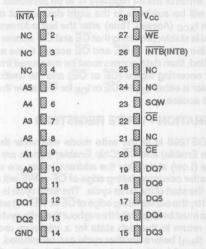
# **DALLAS**SEMICONDUCTOR

# DS1286 Watchdog Timekeeper

#### **FEATURES**

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real time-related activities
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V<sub>CC</sub>
- 50 bytes of user NV RAM

#### **PIN ASSIGNMENT**



28-Pin Encapsulated Package (720 Mil Flush)

#### **PIN DESCRIPTION**

INTA	-	Interrupt Output A
INTB(INTB)		Interrupt Output B
A0-A5	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
CE	-	Chip Enable
OE	-	Output Enable
WE	-	Write Enable
Vcc	-	+5 Volts
GND	-	Ground
NC	-	No Connection
SQW	-	Square Wave Output

# DESCRIPTION

The DS1286 Watchdog Timekeeper is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 64 eight-bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of

V<sub>CC</sub> and write protects memory when V<sub>CC</sub> is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V<sub>CC</sub>. Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with

an AM/PM indicator. The watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

#### **OPERATION - READ REGISTERS**

The DS1286 executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (High) and  $\overline{CE}$  (Chip Enable) and  $\overline{OE}$  (Output Enable) are active (Low). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the latter occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $\overline{OE}$  for  $\overline{OE}$  rather than address access

#### **OPERATION - WRITE REGISTERS**

The DS1286 is in the write mode whenever the WE (Write Enable) and CE (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery state (twR) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t<sub>DS</sub>) and Data Hold Time (t<sub>DH</sub>) with respect to the earlier rising edge of CE or WE. The OE control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active), then WE will disable the outputs in topw from its falling edge.

#### **DATA RETENTION**

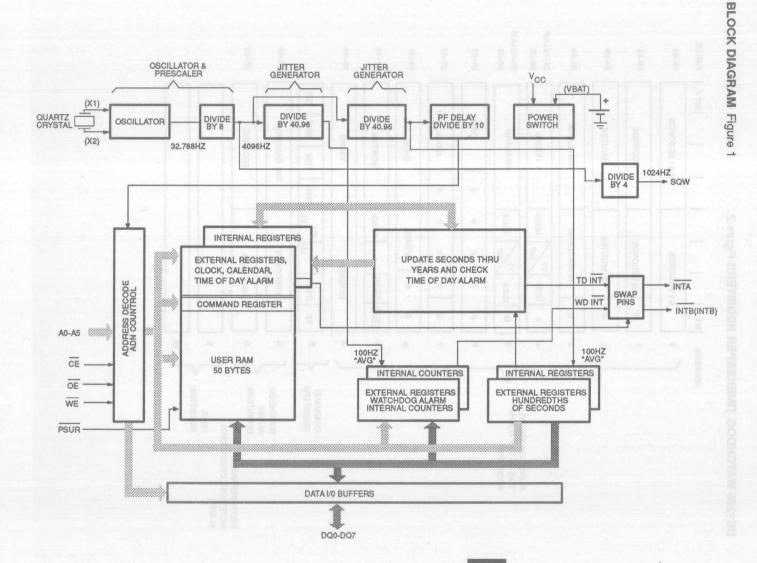
The Watchdog Timekeeper provides full functional capability when  $V_{CC}$  is greater than 4.5 volts and write pro-

tects the register contents at 4.25 volts typical. Data is maintained in the absence of V<sub>CC</sub> without any additional support circuitry. The DS1286 constantly monitors V<sub>CC</sub>. Should the supply voltage decay, the Watchdog Timekeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts INTA and INTB (INTB) and the internal clock and timers continue to run regardless of the level of V<sub>CC</sub>. As V<sub>CC</sub> falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V<sub>CC</sub> rises above approximately 3.0 volts, the power switching circuit connects external V<sub>CC</sub> and disconnects the internal lithium energy source. Normal operation can resume after V<sub>CC</sub> exceeds 4.5 volts for a period of 150 ms.

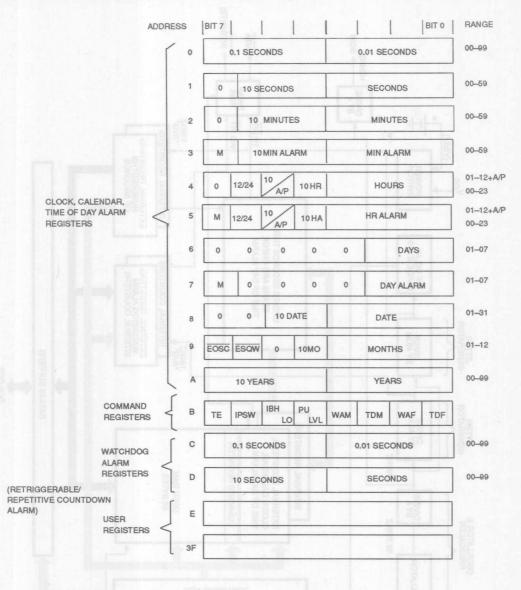
#### **WATCHDOG TIMEKEEPER REGISTERS**

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm, and Watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm registers and information which is stored in these two registers is in BCD. Registers E through 3F are user bytes and can be used to contain data at the user's discretion.

020692 3/12



## DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



# 6

#### TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, EOSC (bit 7) enables the Real Time Clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (Pin 23). When set to logic zero, the Square Wave Output pin will output a 1024 Hz Square Wave Signal. When set to logic one the Square Wave Output pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12- or 24- hour Select Bit. When set to logic one, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the real time clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen.

An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds read 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also

produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

#### TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm registers are written and read in the same format as the Time of Day registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm registers are read or written.

#### **WATCHDOG ALARM REGISTERS**

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Registers C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer countdown is interrupted and reinitialized back to the entered value every time either of the registers is accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm registers always read the entered value. The actual countdown register is internal and is not readable. Writing Registers C and D to zero will disable the Watchdog Alarm feature.

#### COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logic one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm registers. However, if the transfer enable bit is set to logic zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logic one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Watchdog Alarm registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logic one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logic zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask bit (WAM). When this bit is written to a logic one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins INTA and INTB (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and INTA will sink current for a minimum of 3 ms and then release. Output INTB (INTB) will either sink or source current for a minimum of 3 ms depending on the level of bit 5. When bit 5 is set to logic one, the B interrupt will source current. When bit 5 is set to logic zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins INTA or INTB(INTB). When set to logic one, INTA becomes the Time of Day Alarm Interrupt pin and INTB(INTB) becomes the Watchdog Interrupt pin. When bit 6 is set to logic zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on INTB(INTB) and the Watchdog Interrupt will be output on INTA. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day registers.

#### TIME OF DAY ALARM MASK BITS Figure 3

adl nis noc	REGISTER	Melgefi	sale months access to coour without day
(3)MINUTES	(5)HOURS	(7)DAYS	seque update. When the watch rugister
Pegiatas o	emalA <b>p</b> obelo	eWed	ALARM ONCE PER MINUTE
0	of malApol	Material Pod ba	ALARM WHEN MINUTES MATCH
0	0	tr wer bad 1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

6

## **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	10
Input Logic 1	V <sub>IH</sub>	2.2	trus!	V <sub>CC</sub> + 0.3	V	10
Input Logic 0	V <sub>IL</sub>	-0.3	T and	+0.8	V	10

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C TO }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	IIL	-1.0	accord	+1.0	μА	that buston
Output Leakage Current	ILO	-1.0	0.01	+1.0	μА	ole Seluc
I/O Leakage Current	ILIO	-1.0	v.ed	+1.0	μА	Think etc.
Output Current @ 2.4V	Гон	-1.0	- sand		mA	PER AT
Output Current @ 0.4V	loL	2.0			mA	13
Standby Current CE = 2.2V	I <sub>CCS1</sub>		3.0	7.0	mA	
Standby Current CE > V <sub>CC</sub> -0.5	I <sub>CCS2</sub>			4.0	mA	
Active Current	Icc			15	mA	
Write Protection Voltage	V <sub>TP</sub>		4.25		V	

#### CAPACITANCE

(tA=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		7	10	pF	
Output Capacitance	C <sub>OUT</sub>		7	10	pF	
Input/Output Capacitance	C <sub>VO</sub>		7	10	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

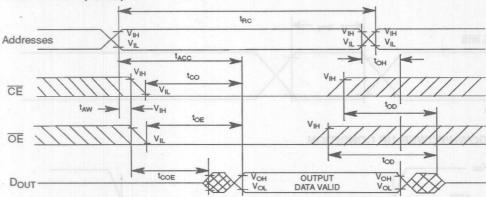
## AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \text{ TO } 70^{\circ} \text{ C}, V_{CC} = 4.5 \text{V TO } 5.5 \text{V})$ 

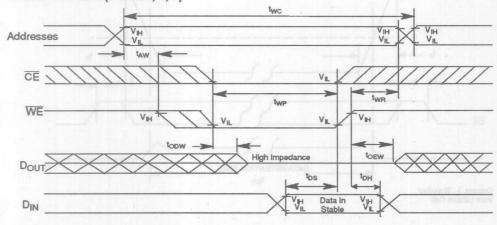
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	150	B-TE-B	386	ns	MISSE
Address Access Time	tACC			150	ns	
CE Access Time	tco	fion is not i	this specific	150	ns	i beissibi
OE Access Time	t <sub>OE</sub>	Anidalier	ne may affect	60	ns	shdilipho
OE or CE to Output Active	t <sub>COE</sub>	10	d contact	BITASES	ns	COMM
Output High Z from Deselect	top	l von	Lionwy	60	ns	THEATLE
Output Hold from Address Change	tон	10	Yea		ns	tiely viqqt
Write Cycle Time	twc	150	HIV.		ns	olgo.J tug
Write Pulse Width	t <sub>WP</sub>	140	T - TA		ns	3
Address Setup Time	t <sub>AW</sub>	0			ns	
Write Recovery Time	t <sub>WR</sub>	10		The state of	ns	North Street
Output High Z from WE	topw	804884	20 detre	50	ns	TORIAN
Output Active from WE	toew	10	II III		ns	1788U 1UC
Data Setup Time	t <sub>DS</sub>	45	0.3		ns	4
Data Hold Time	t <sub>DH</sub>	0	GIN		ns	4,5
INTA, INTB Pulse Width	t <sub>IPW</sub>	3	HOL		ms	11,12

			PARIAMETER
			Input Capacitance

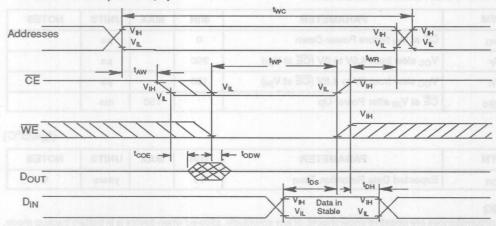




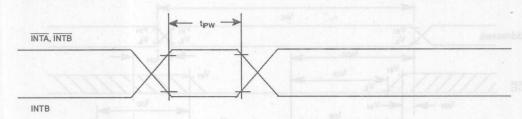
# WRITE CYCLE 1 (Notes 2, 6, 7)



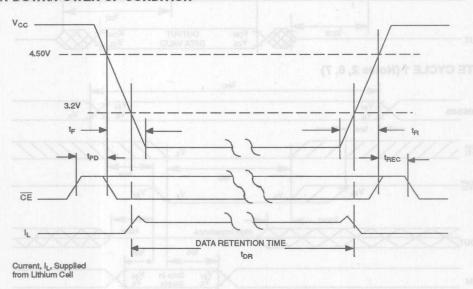
## WRITE CYCLE 2 (Notes 2, 8)



# TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



#### POWER-DOWN/POWER-UP CONDITION



# POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0	1	μѕ	coeas
t <sub>F</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	350		μs	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH</sub> )	100	1	μs	
†REC	CE at V <sub>IH</sub> after Power Up		150	ms	

(tA=25°C)

SYM	SYM PARAMETER		MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10		years	9

#### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES

- 1. WE is high for a read cycle.
- OE = V<sub>IH</sub> or V<sub>IL</sub>. If OE = V<sub>IH</sub> during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of the CE and WE. t<sub>WP</sub> is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
- t<sub>DS</sub> or t<sub>DH</sub> are measured from the earlier of CE or WE going high.
- t<sub>DH</sub> is measured from WE going high. If CE is used to terminate the write cycle, then t<sub>DH</sub> = 20 ns.
- If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition,

- the output buffers remain in a high impedance state during this period.
- Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- 10. All voltages are referenced to ground.
- Applies to both interrupt pins when the alarms are set to pulse.
- Interrupt output occurs within 100 ns on the alarm condition existing.
- Both INTA and INTB(INTB) are open drain outputs.

#### **AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0-3.0V

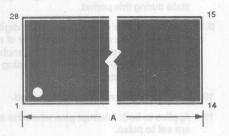
Timing Measurement Reference Levels

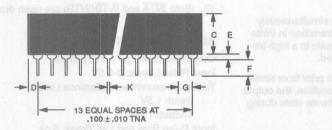
Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5 ns.

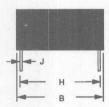


## **DS1286 WATCHDOG TIMEKEEPER**





PKG	28-F	PIN
DIM	. MIN	MAX
A IN.	1.520 38.61	1.540 39.12
B IN.	0.695 17.65	0.720 18.29
C IN.	0.350 8.89	0.375 9.52
D IN.	0.100 2.54	0.130 3.30
E IN.	0.015 0.38	0.030 0.76
F IN.	0.110 2.79	0.140 3.56
G IN.	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021 0.53



NOTE: PINS 2, 3, 21, 24 AND 25 ARE MISSING BY DESIGN.

# DALLAS

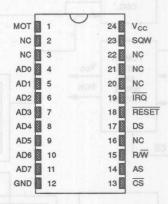
# FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
- Periodic rates from 122 µs to 500 ms
- End of clock update cycle

#### DESCRIPTION

The DS1287 Real Time Clock is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a

#### **PIN ASSIGNMENT**



24 PIN ENCAPSULATED PACKAGE

#### PIN DESCRIPTION

AD0-AD7	- Multiplexed address/data bus
NC	- No connection
MOT	- Bus type selection
CS	- Chip select
AS	- Address strobe
R/W	- Read/write input
DS	- Data strobe
RESET	- Reset input
ĪRQ	- Interrupt request output
SQW	- Square wave output
Vcc	- +5 volt supply
GND	- Ground

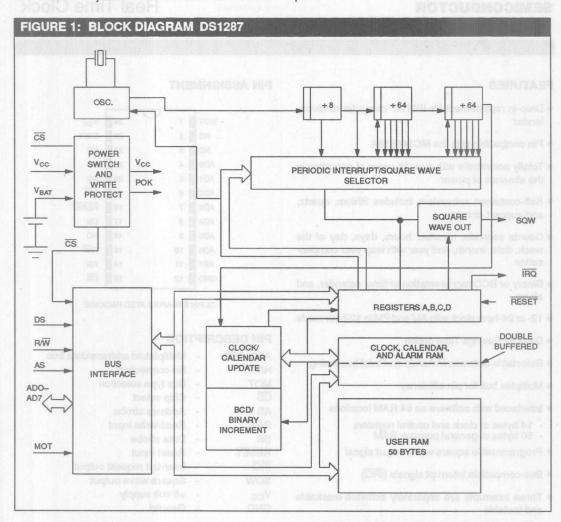
nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

6

#### **OPERATION**

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1287.

The following paragraphs describe the function of each



# POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V<sub>CC</sub> input. When V<sub>CC</sub> is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the

system to stabilize after power is applied. When  $V_{CC}$  falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of  $\overline{CS}$  at the input pin. The DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When  $V_{CC}$  falls below a level of approximately 3 volts, the external  $V_{CC}$  supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

#### SIGNAL DESCRIPTIONS

GND,  $V_{CC}$  - DC power is provided to the device on these pins.  $V_{CC}$  is the  $\pm 5$  volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When  $V_{CC}$  is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of  $\pm 1$  minute per month at 25°C regardless of the voltage input on the  $V_{CC}$  pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to

 $V_{\rm CC}$ , Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 K $\Omega$ .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when  $V_{CC}$  is less than 4.25 volts typical.

SE	LECT BITS	REGISTE	RA	t <sub>PI</sub> PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz
0	GILL Loide	0	but 1 and	488.281 μs	2.048 kHz
0	1	1	0	976.5625 μs	1.024 kHz
0	can be co	38.1H no	facility last	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1,000	0	es reti en	to dis <sup>1</sup> n assat	31.25 ms	32 Hz
1	u to falled	0	0	62.5 ms	16 Hz
di set	sau tan d	0	uol tha ,aa	125 ms	8 Hz
1	11/10/10/10	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be pres-

ent and held stable during the latter portion of the DS or WR pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

DS (Data Strobe or Read Input) - The DS/ $\overline{RD}$  pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to  $V_{CC}$ , Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read( $\overline{RD}$ ).  $\overline{RD}$  identifies the time period when the DS1287 drives the bus with read data. The  $\overline{RD}$  signal is the same definition as the Output Enable ( $\overline{OE}$ ) signal on a typical memory.

R/\overline{W} (Read/Write Input)-The R/\overline{W} pin also has two modes of operation. When the MOT pin is connected to V<sub>CC</sub> for Motorola timing, R/\overline{W} is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/\overline{W} while DS is high. A write cycle is indicated when R/\overline{W} is low during DS.

When the MOT pin is connected to GND for Intel timing, the  $R/\overline{W}$  signal is an active low signal called  $\overline{WR}$ . In this mode the  $R/\overline{W}$  pin has the same meaning as the Write Enable signal ( $\overline{WE}$ ) on generic RAMs.

 $\overline{\text{CS}}$  (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS1287 to be accessed.  $\overline{\text{CS}}$  must be kept in the active state during DS and AS for Motorola timing and during  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  for Intel timing. Bus cycles which take place without asserting  $\overline{\text{CS}}$  will latch addresses but no access will occur. When  $V_{\text{CC}}$  is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the  $\overline{\text{CS}}$  input. This action protects both the real time clock data and RAM data during power outages.

 $\overline{\textbf{IRQ}}$  (Interrupt Request Output) - The  $\overline{\textbf{IRQ}}$  pin is an active low output of the DS1287 that can be used as an interrupt input to a processor. The  $\overline{\textbf{IRQ}}$  output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the  $\overline{\textbf{IRQ}}$  pin the processor program normally reads the C register. The  $\overline{\textbf{RESET}}$  pin also clears pending interrupts.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The RESET pin has no effect on the clock, calendar, or RAM. On power-up the RE-

SET pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that RESET is held low is dependent on the application. However, if RESET is used on power-up, the time RESET is low should exceed 200 ms to make sure that the internal timer that controls the DS1287 on power-up has timed out. When RESET is low and V<sub>CC</sub> is above 4.25 volts, the follow ing occurs:

- Periodic Interrupt Enable (PIE) bit is cleared to zero.
- B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
- Update Ended Interrupt Flag (UF) bit is cleared to zero.
- Interrupt Request Status Flag (IRQF) bit is cleared to zero.
- E. Periodic Interrupt Flag (PF) bit is cleared to zero.
- The device is not accessible until RESET is returned high.
- G. Alarm Interrupt Flag (AF) bit is cleared to zero.
- H. IRQ pin is in the high impedance state.
- Square Wave Output Enable (SQWE) bit is cleared to zero.
- J. Update Ended Interrupt Enable (UIE) is cleared to zero.

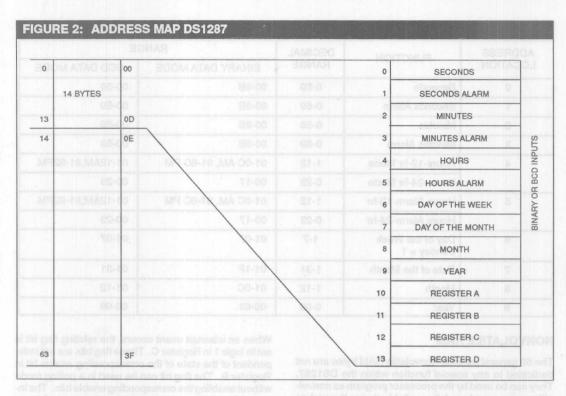
In a typical application  $\overline{\text{RESET}}$  can be connected to  $V_{CC}$ . This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

#### **ADDRESS MAP**

The address map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

- Registers C and D are read-only.
- Bit 7 of Register A is read-only.
- The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.



## TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one.

The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

ADDRESS	FUNCTION	DECIMAL	RANGE			
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE		
0	Seconds	0-59	00-3B	00-59		
1	Seconds Alarm	0-59	00-3B	00-59		
2	Minutes	0-59	00-3B	00-59		
3	Minutes Alarm	0-59	00-3B	00-59		
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM		
	Hours-24-hr Mode	0-23	00-17	00-23		
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM		
	Hours Alarm-24-hr	0-23	00-17	00-23		
6	Day of the Week Sunday = 1	1-7	01-07	01-07		
7	Date of the Month	1-31	01-1F	01-31		
8	Month	1-12	01-0C	01-12		
9	Year	0-99	00-63	00-99		

#### **NONVOLATILE RAM**

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

#### **INTERRUPTS**

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the  $\overline{IRQ}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{IRQ}$  is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{\rm IRQ}$  pin is asserted low.  $\overline{\rm IRQ}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{\rm IRQ}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

# 6

#### **OSCILLATOR CONTROL BITS**

When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

#### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

#### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{IRQ}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

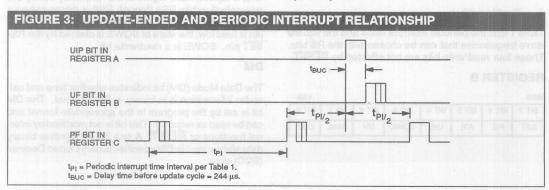
#### **UPDATE CYCLE**

The DS1287 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244  $\mu s$  later. If a low is read on the UIP bit, the user has at least 244  $\mu s$  before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244  $\mu s$ .

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ( $t_{Pl/2} + t_{BUC}$ ) to ensure that data is not read during the update cycle.



#### REGISTERS

The DS1287 has four control registers which are accessible at all times, even during the update cycle.

#### **REGISTER A**

MSB					off eac	update	LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DVO	RS3	RS2	RS1	RS0

#### UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RESET. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

#### DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

#### RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit;
- Enable both at the same time and the same rate; or

#### 4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by RESET.

#### REGISTER B

ASB BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

#### SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by RESET or internal functions of the DS1287.

#### PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{IRQ}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{IRQ}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{IRQ}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on  $\overline{RESET}$ .

#### AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The RESET pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

#### LHE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears to UIE bit.

#### SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

#### DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

# 6

#### 24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of RESET.

#### DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

#### REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

#### IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 AF = AIE = 1 UF = UIE = 1

That is, IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE).

Any time the IRQF bit is a one, the IRQ pin is driven low.

All flag bits are cleared after Register C is read by the program or when the RESET pin is low.

#### DE

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are

ones, the  $\overline{IRQ}$  signal is active and will set the IRQF bit. The PF bit is cleared by a  $\overline{RESET}$  or a software read of Register C.

#### AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the  $\overline{IRQ}$  pin will go low and a one will appear in the IRQF bit. A RESET or a read of Register C will clear AF.

#### UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ pin. UF is cleared by reading Register C or a RESET.

#### **BIT 0 THROUGH BIT 3**

These are unused bits of the status Register C. These bits always read zero and cannot be written.

#### **REGISTER D**

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

#### VRT

The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by RESET.

#### **BIT 6 THROUGH BIT 0**

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

#### ABSOLUTE MAXIMUM RATINGS\*

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES			
Power Supply Voltage	Vcc	4.5	5.0	5.5	Fl to Vitolo	nterpins fur			
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	REIT IO			
Input Logic 0	V <sub>IL</sub>	-0.3	ISI	+0.8	V	1			

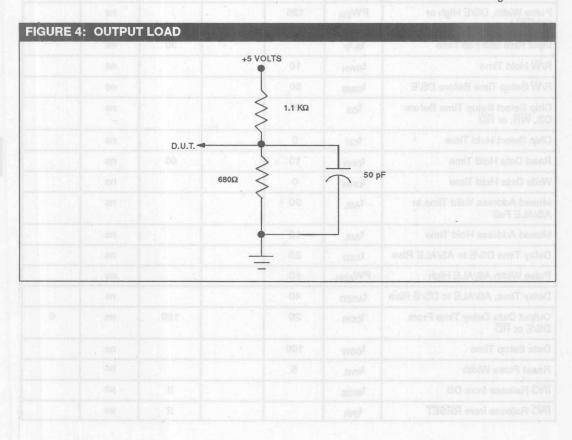
DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V <sub>CC</sub> = 4.5 TO 5.5V)									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES			
Power Supply Current	lcc1	761	7	15	mA	2			
Input Leakage	o I <sub>IL</sub> o	-1.0		+1.0	μА	3			
I/O Leakage	I <sub>LO</sub>	-1.0		+1.0	μА	4			
Input Current	I <sub>MOT</sub>	-1.0	to a medi	+500	μА	3			
Output @ 2.4V	Іон	-1.0			mA	1,5			
Output @ 0.4V	l <sub>OL</sub>	195 8	a read by t	4.0	mA	e stidge			

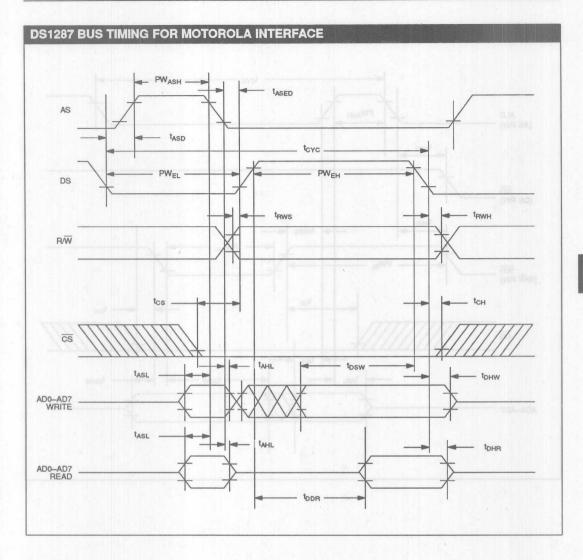
CAPACITANCE (t <sub>A</sub> = 25°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Input Capacitance	C <sub>IN</sub>	enT . a	ph ASO bits e	5.4	pF	vib esti lo		
Output Capacitance	C <sub>OUT</sub>	616S 6	is 319 bas 30	7	pF	o efeta orl		

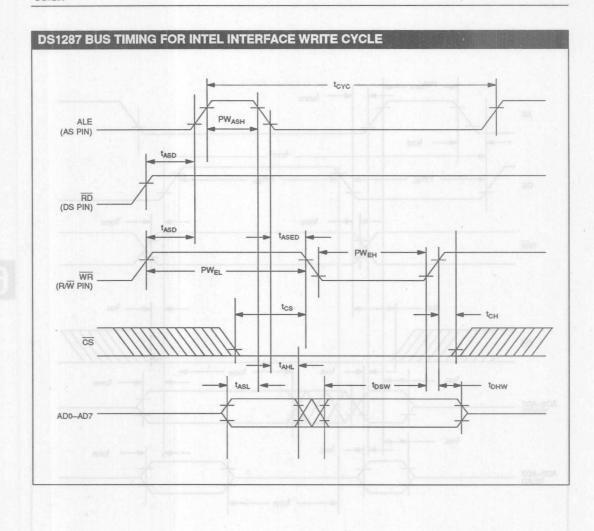
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	tcyc	385		DC	ns	CILLO IN
Pulse Width, DS/E Low or RD/WR High	PW <sub>EL</sub>	150	14 100	MICH WITHOUT	ns	20 KG.
Pulse Width, DS/E High or RD/WR Low	PW <sub>EH</sub>	125			ns	
Input Rise and Fall Time	t <sub>R</sub> ,t <sub>F</sub>			30	ns	
R/W Hold Time	t <sub>RWH</sub>	10	9		ns	
R/W Setup Time Before DS/E	t <sub>RWS</sub>	50			ns	
Chip Select Setup Time Before DS, WR, or RD	tcs	20			ns	
Chip Select Hold Time	t <sub>CH</sub>	0	0	10.0	ns	
Read Data Hold Time	t <sub>DHR</sub>	10		80	ns	
Write Data Hold Time	t <sub>DHW</sub>	0	Septem 1		ns	
Muxed Address Valid Time to AS/ALE Fall	tASL	30			ns	
Muxed Address Hold Time	t <sub>AHL</sub>	10	9		ns	
Delay Time DS/E to AS/ALE Rise	t <sub>ASD</sub>	25			ns	
Pulse Width AS/ALE High	PWASH	60			ns	
Delay Time, AS/ALE to DS/E Rise	tASED	40			ns	
Output Data Delay Time From DS/E or RD	t <sub>DDR</sub>	20		120	ns	6
Data Setup Time	t <sub>DSW</sub>	100			ns	
Reset Pulse Width	t <sub>RWL</sub>	5			μs	
IRQ Release from DS	t <sub>IRDS</sub>			2	μs	
IRQ Release from RESET	t <sub>IRR</sub>		Marillon,	2	μs	

#### NOTES

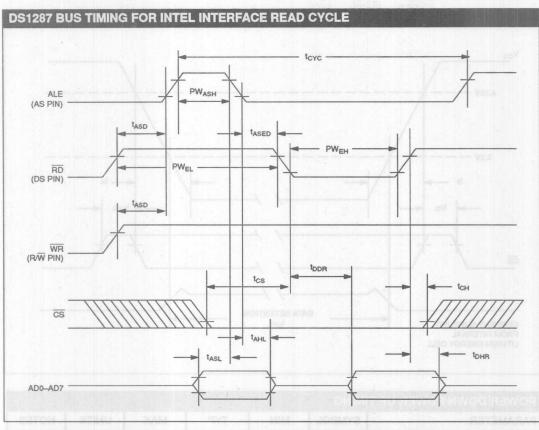
- 1. All voltages are referenced to ground.
- 2. All outputs are open.
- The MOT pin has an internal pulldown of 20 KΩ.
- Applies to the AD0-AD7 pins, the IRQ pin, and the SQW pin when each is in the high impedance state.
- 5. The IRQ pin is open drain.
- 6. Measured with a load as shown in Figure 4.

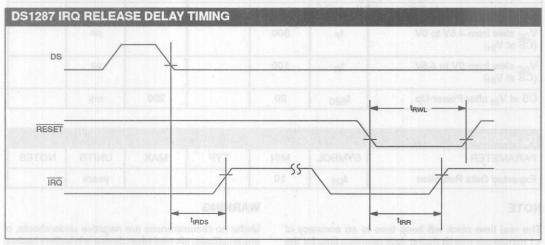


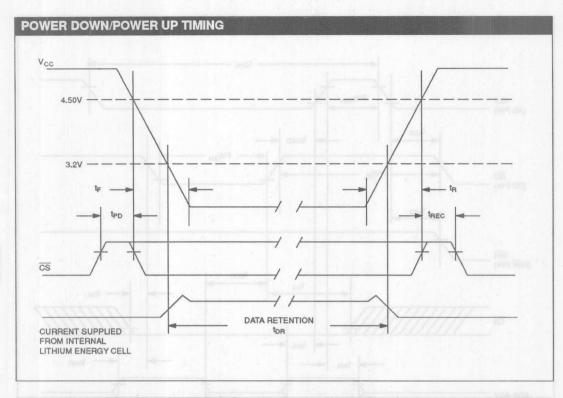












POWER DOWN/POWER UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CS at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0	IMING	VZ NEG E	μѕ	THE STATE
V <sub>CC</sub> slew from 4.5V to 0V (CS at V <sub>IH</sub> )	t <sub>F</sub>	300			μs	
V <sub>CC</sub> slew from 0V to 4.5V (CS at V <sub>IH</sub> )	t <sub>R</sub>	100		H	μs	
CS at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>	20		200	ms	

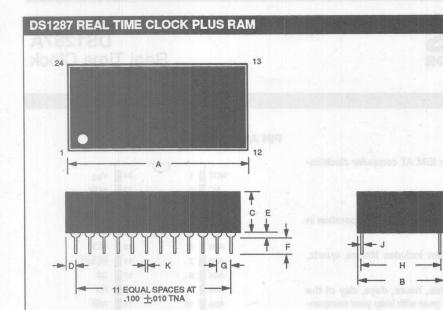
(t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t <sub>DR</sub>	10	T		years	<b>ENE</b>

### NOTE

The real time clock will keep time to an accuracy of  $\pm 1$  minute per month during data retention time for the period of  $t_{DR}$ .

### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.



PKG	24-	PIN
DIM	MIN	MAX
AIN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.345 8.76	0.370 9.40
D IN.	0.100	0.130
MM	2.54	3.30
EIN.	0.015	0.030
MM	0.38	0.76
FIN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008	0.012
MM	0.20	0.30
KIN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, 20, 21 AND 22 ARE MISSING BY



## DS1287A Real Time Clock

#### **FEATURES**

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
- Time-of-day alarm once/second to once/day
- Periodic rates from 122 µs to 500 ms
- End of clock update cycle

# PIN ASSIGNMENT

мот	1	24	Vcc
NC I	2	23	saw
NC I	3	22	NC
AD0	4	21	RCLR
AD1	5	20	NC
AD2	6	19	IRQ
AD3	7	18	RESET
AD4	8	17	DS
AD5	9	16	NC
AD6	10	15	R/W
AD7	11	14	AS
GND	12	13	CS

24 PIN ENCAPSULATED PACKAGE

#### **PIN DESCRIPTION**

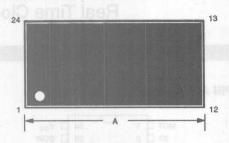
	1 0.67.0   U.S.O.   JANE 1 0.700
AD0-AD7	- Multiplexed address/data bus
NC	- No connection
MOT	- Bus type selection
CS	- Chip select
AS	- Address strobe
R/W	- Read/write input
DS	- Data strobe
RESET	- Reset input
ĪRQ	- Interrupt request output
SQW	- Square wave output
Vcc	- +5 volt supply
GND	- Ground
RCLR	- RAM clear

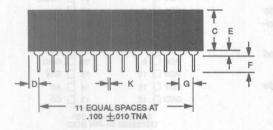
#### DESCRIPTION

The DS1287A is identical to the DS1287 with the addition of the RAM clear pin. The RCLR pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery

backup mode when  $V_{CC}$  is not applied. The  $\overline{RCLR}$  function is designed to be used via human interface (shorting to ground manually or by switch) an not to be driven with external buffers. All other operation, description and specification is identical to the DS1287.

### **DS1287A REAL TIME CLOCK PLUS RAM**





	NED DE	Meh
11-1		U
-	н -	
-	В	-

NOTE:

PINS 2, 3, 16, 20 AND 22 ARE MISSING BY DESIGN.

NOTE:

THIS DEVICE CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL WHICH WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

	PKG	24-	PIN
	DIM	MIN	MAX
	A IN.	1.320 33.53	1.335 33.91
	B IN. MM	0.675 17.15	0.700 17.78
B	C IN.	0.345 8.76	0.370 9.40
	D IN. MM	0.100 2.54	0.130 3.30
	E IN. MM	0.015 0.38	0.030 0.76
	F IN.	0.110 2.79	0.140 3.56
	G IN. MM	0.090 2.29	0.110 2.79
	H IN.	0.590 14.99	0.630 16.00
	J IN. MM	0.008 0.20	0.012 0.30
	K IN.	0.015 0.38	0.021 0.53



# DS12885, DS12885Q Real Time Clock

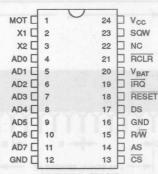
#### **FEATURES**

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818B and DS1285
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
- Time-of-day alarm once/second to once/day
- Periodic rates from 122 μA to 500 ms
- End of clock update cycle
- Optional 28-pin PLCC surface mount package

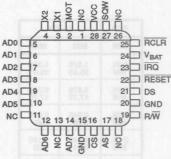
#### DESCRIPTION

The DS12885 Real Time Clock plus RAM is designed to be a direct replacement for the DS1285. The DS1285 is identical in form, fit, and function to the DS1285, and has an additional 114 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, VBAT, and RCLR, see the DS12887 data sheet.

#### PIN ASSIGNMENT



DS12885 24-PIN DIP DS12885S 24-PIN SOIC



DS12885Q 8-PIN PLCC

#### **PIN DESCRIPTION**

AD0-AD7 Multiplexed Address/Data Bus NC - No Connection MOT - Bus Type Selection CS - Chip Select AS Address Strobe R/W - Read/Write Input DS - Data Strobe RESET Reset Input

IRQ - Interrupt Request Output
SQW - Square Wave Output
Vcc +5 Volt Supply

GND - Ground X1,X2 - 32.768 kH

X1,X2 - 32.768 kHz Crystal Connections
VBAT - +3 volt Battery Input

RCLR - RAM Clear

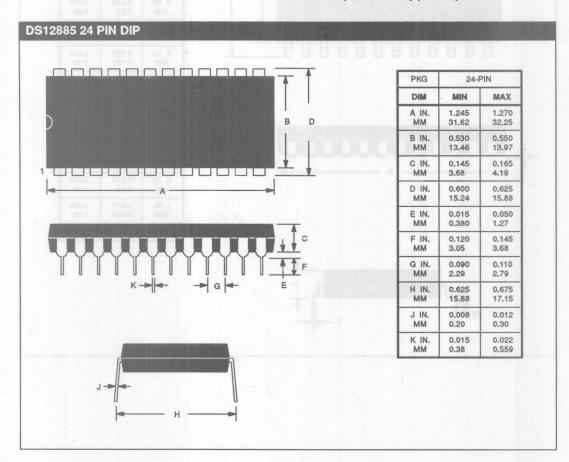
#### **PIN DESCRIPTION**

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S, Seiko part number DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. A variable trimming capacitor may be required for extremely high precision timekeeping applications. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

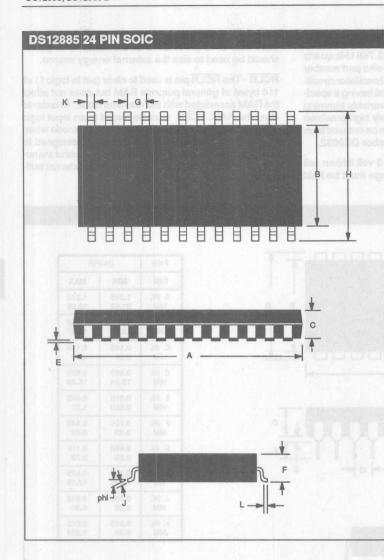
V<sub>BAT</sub> - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held

between 2.5 and 4 volts for proper operation. A maximum load of .5  $\mu$ A at 25°C in the absence of power should be used to size the external energy source.

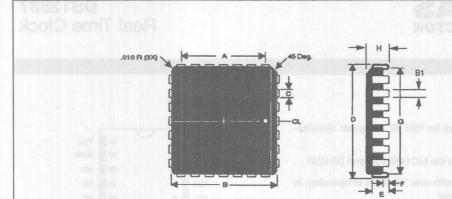
RCLR - The RCLR pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V<sub>CC</sub> is not applied. The RCLR function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.



6



PKG	24-1	PIN
DIM	MIN	MAX
A IN.	0.602	0.612
MM	15.29	15.54
B IN.	0.290	0.300
MM	7.37	7.65
C IN.	0.089	0.095
MM	2.26	2.41
E IN.	0.004	0.012
MM	0.102	0.30
F IN.	0.094	0.105
MM	2.38	2.68
G IN. MM	0.050 BS	
H IN.	0.398	0.416
MM	10.11	10.57
J IN.	0.009	0.013
MM	0.229	0.33
K IN.	0.013	0.019
MM	0.33	0.48
L IN. MM	0.016 0.406	0.040
phi	0°	8°



**DS12885Q 28 PIN PLCC** 

PKG	28-	NIC
DIM	MIN	MAX
AIN. MM	0.300 R 7.62	EF
B IN.	0.442	0.462
MM	17.68	11.73
B1 IN.	0.013	0.021
MM	0.33	0.53
C IN.	0.027	0.033
MM	0.68	0.84
D IN.	0.480	0.500
MM	12.2	12.7
E IN.	0.090	0.120
MM	2.29	3.05
FIN. MM	0.020 0.51	MIN
G IN.	0.390	0.430
MM	9.91	10.92
H IN.	0.165 4.19	0.180 4.57

#### **FEATURES**

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 μs to 500 ms
  - End of clock update cycle

#### DESCRIPTION

The DS12887 Real Time Clock plus RAM is designed to be a direct replacement for the DS1287. The DS12887 is identical in form, fit, and function to the DS1287, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such,

#### **PIN ASSIGNMENT**

мот	1	24	Vcc
NC	2	23	SQW
NC	3	22	NC
AD0	4	21	NC
AD1	5	20	NC
AD2	6	19	IRQ
AD3	7	18	RESET
AD4	8	17	DS
AD5	9	16	NC
AD6	10	15	RW
AD7	11	14	AS
GND	12	13	CS
-			

24 PIN ENCAPSULATED PACKAGE

#### PIN DESCRIPTION

I III DECO		
AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
CS	-	Chip Select
AS	-	Address Strobe
R/W	-	Read/Write Input
DS	-	Data Strobe
RESET	-	Reset Input
IRQ	-	Interrupt Request Output
SQW	-	Square Wave Output

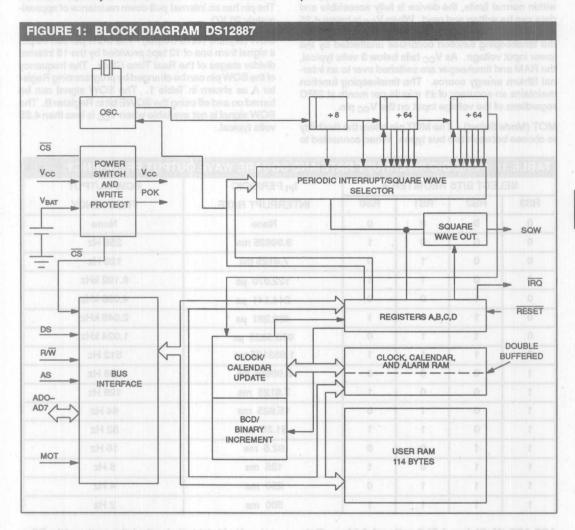
V<sub>CC</sub> - +5 Volt Supply GND - Ground

the DS12887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 114 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

#### **OPERATION**

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS12887.

The following paragraphs describe the function of each pin



# POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the  $V_{\rm CC}$  input. When  $V_{\rm CC}$  is applied to the DS12887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the

system to stabilize after power is applied. When  $V_{CC}$  falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of  $\overline{CS}$  at the input pin. The DS12887 is, therefore, write-protected. When the DS12887 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When  $V_{CC}$  falls below a level of approximately 3 volts, the external  $V_{CC}$  supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

#### SIGNAL DESCRIPTIONS

GND,  $V_{CC}$  - DC power is provided to the device on these pins.  $V_{CC}$  is the  $\pm 5$  volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When  $V_{CC}$  is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of  $\pm 1$  minute per month at 25°C regardless of the voltage input on the  $V_{CC}$  pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to

 $V_{\rm CC}$ , Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 K $\Omega$ .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when  $V_{\rm CC}$  is less than 4.25 volts typical.

SE	LECT BITS	REGISTE	RA	t <sub>PI</sub> PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz
0	1 0	0	DBR 1	488.281 μs	2.048 kHz
0	1	1	0	976.5625 μs	1.024 kHz
0	1	иска1 го х	0.50 1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS12887 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS12887 latches the address from AD0 to AD6. Valid write data must be pres-

ent and held stable during the latter portion of the DS or  $\overline{WR}$  pulses. In a read cycle the DS12887 outputs 8 bits of data during the latter portion of the DS or  $\overline{RD}$  pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as  $\overline{RD}$  transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS12887.

DS (Data Strobe or Read Input) - The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V<sub>CC</sub>, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS12887 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS12887 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read(RD). RD identifies the time period when the DS12887 drives the bus with read data. The RD signal is the same definition as the Output Enable (OE) signal on a typical memory.

R/\overline{W} (Read/Write Input)-The R/\overline{W} pin also has two modes of operation. When the MOT pin is connected to V<sub>CC</sub> for Motorola timing, R/\overline{W} is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/\overline{W} while DS is high. A write cycle is indicated when R/\overline{W} is low during DS.

When the MOT pin is connected to GND for Intel timing, the  $R/\overline{W}$  signal is an active low signal called  $\overline{WR}$ . In this mode the  $R/\overline{W}$  pin has the same meaning as the Write Enable signal ( $\overline{WE}$ ) on generic RAMs.

 $\overline{\text{CS}}$  (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS12887 to be accessed.  $\overline{\text{CS}}$  must be kept in the active state during DS and AS for Motorola timing and during  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  for Intel timing. Bus cycles which take place without asserting  $\overline{\text{CS}}$  will latch addresses but no access will occur. When  $V_{CC}$  is below 4.25 volts, the DS12887 internally inhibits access cycles by internally disabling the  $\overline{\text{CS}}$  input. This action protects both the real time clock data and RAM data during power outages.

 $\overline{\textbf{IRQ}}$  (Interrupt Request Output) - The  $\overline{\textbf{IRQ}}$  pin is an active low output of the DS12887 that can be used as an interrupt input to a processor. The  $\overline{\textbf{IRQ}}$  output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the  $\overline{\textbf{IRQ}}$  pin the processor program normally reads the C register. The  $\overline{\textbf{RESET}}$  pin also clears pending interrupts.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The RESET pin has no effect on the clock, calendar, or RAM. On power-up the RE-

SET pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that RESET is held low is dependent on the application. However, if RESET is used on power-up, the time RESET is low should exceed 200 ms to make sure that the internal timer that controls the DS12887 on power-up has timed out. When RESET is low and V<sub>CC</sub> is above 4.25 volts, the follow ing occurs:

- Periodic Interrupt Enable (PEI) bit is cleared to zero.
- B. Alarm Interrupt Enable (AIE) bit is cleared to
- Update Ended Interrupt Flag (UF) bit is cleared to zero.
- Interrupt Request Status Flag (IRQF) bit is cleared to zero.
- E. Periodic Interrupt Flag (PF) bit is cleared to zero.
- F. The device is not accessible until RESET is returned high.
- G. Alarm Interrupt Flag (AF) bit is cleared to zero.
- H. IRQ pin is in the high impedance state.
- Square Wave Output Enable (SQWE) bit is cleared to zero.
- Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application  $\overline{\text{RESET}}$  can be connected to  $V_{CC}$ . This connection will allow the DS12887 to go in and out of power fail without affecting any of the control registers.

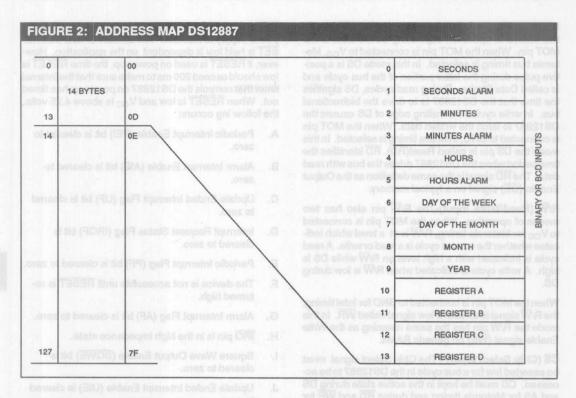
#### ADDRESS MAP

The address map of the DS12887 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

- Registers C and D are read-only.
- 2. Bit 7 of Register A is read-only.
- The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

6



#### TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The

time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

ADDRESS	d dishou na soluce xa T	DECIMAL	RANG	NGE	
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE	
0	Seconds	0-59	00-3B	00-59	
erli et 1 liquiot a	Seconds Alarm	0-59	00-3B	00-59	
2	Minutes	0-59	00-3B	00-59	
3	Minutes Alarm	0-59	00-3B	00-59	
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM	
	Hours-24-hr Mode	0-23	00-17	00-23	
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM	
	Hours Alarm-24-hr	0-23	00-17	00-23	
6	Day of the Week Sunday = 1	1-7	01-07	01-07	
7	Date of the Month	1-31	01-1F	01-31	
8	Month	1-12	01-0C	01-12	
9	Year	0-99	00-63	00-99	

#### **NONVOLATILE RAM**

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS12887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

#### **INTERRUPTS**

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the  $\overline{IRQ}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{IRQ}$  is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts a re lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{IRQ}$  pin is asserted low.  $\overline{IRQ}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{IRQ}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12887. The act of reading Register C clears all active flag bits and the IRQF bit.

#### OSCILLATOR CONTROL BITS

When the DS12887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

#### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

#### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{IRQ}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

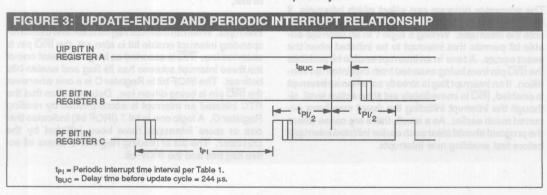
#### **UPDATE CYCLE**

The DS12887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ( $t_{Pl/2} + t_{BUC}$ ) to ensure that data is not read during the update cycle.



#### REGISTERS

The DS12887 has four control registers which are accessible at all times, even during the update cycle.

#### REGISTER A

MSB							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

#### UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RESET. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

#### **DV0, DV1, DV2**

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

#### RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- 1. Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit;
- Enable both at the same time and the same rate; or
- 4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by RESET.

#### REGISTER B

MSB LS							
				BIT 3			
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

#### SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by RESET or internal functions of the DS12887.

#### PIF

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{IRQ}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{IRQ}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{IRQ}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12887 functions, but is cleared to zero on  $\overline{RESET}$ .

#### AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The RESET pin clears AIE to zero. The internal functions of the DS12887 do not affect the AIE bit.

#### UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears to UIE bit.

#### SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

#### DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

#### 24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of RESET.

#### DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

#### REGISTER C

ASB BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1							
BIT 7	BIT 6	BIT 5	BIT 4	ВП 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

#### IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 AF = AIE = 1 UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a one, the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET pin is low.

#### PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are

ones, the IRQ signal is active and will set the IRQF bit. The PF bit is cleared by a RESET or a software read of Register C.

#### AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one will appear in the IRQF bit. A RESET or a read of Register C will clear AF.

#### UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ pin. UF is cleared by reading Register C or a RESET.

#### **BIT 0 THROUGH BIT 3**

These are unused bits of the status Register C. These bits always read zero and cannot be written.

#### REGISTER D

MSB	ASB of the resulting A. mindle munchthrope actification							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
VRT	0	0	0	0	0	0	0	

#### VRT

The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by RESET.

#### **BIT 6 THROUGH BIT 0**

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO +7.0V 0°C TO 70°C -40°C TO +70°C 260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	1		
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	10 .81		
Input Logic 0	V <sub>IL</sub>	-0.3	Hot	+0.8	em V biole	belog gir		

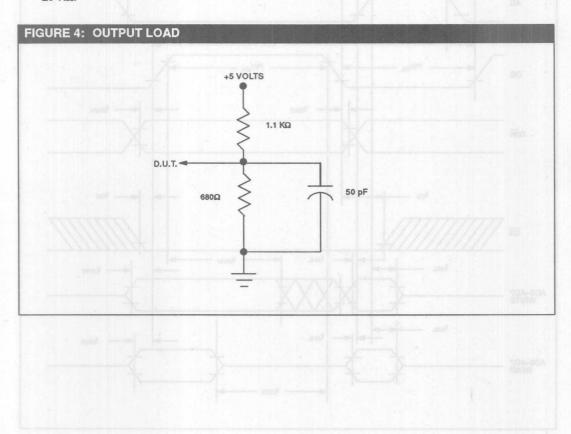
DC ELECTRICAL CHAR	ACTERISTICS (0	°C TO 70°	$^{\circ}$ C, $^{\circ}$ C <sub>C</sub> = 4.	.5 TO 5.5V)		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I <sub>CC1</sub>		7	15	mA	2
Input Leakage	IIL	-1.0		+1.0	μА	3
I/O Leakage	ILO	-1.0	1800	+1.0	μА	4
Input Current	I <sub>MOT</sub>	-1.0	HEAVY	+500	μА	3
Output @ 2.4V	Іон	-1.0	USKAP	0000000	mA	1,5
Output @ 0.4V	loL		HUID	4.0	mA	TH rales
Write Protect Voltage	V <sub>TP</sub>	4.0	4.25	4.5	V	da Setup

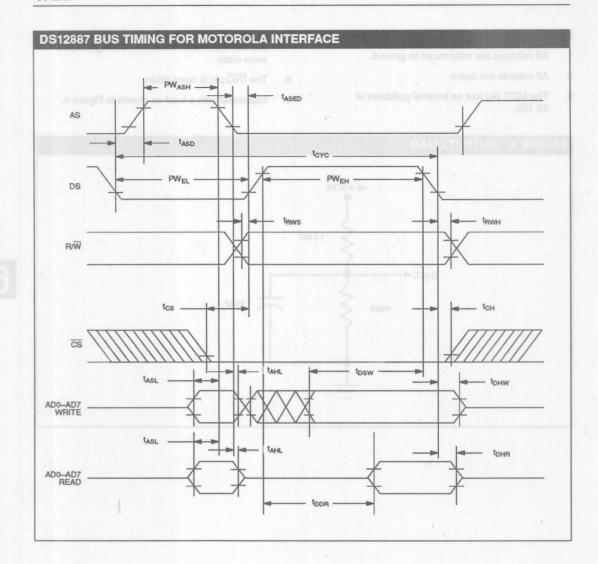
CAPACITANCE (t <sub>A</sub> = 25°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Input Capacitance	CIN			5	pF			
Output Capacitance	C <sub>OUT</sub>			7	pF			

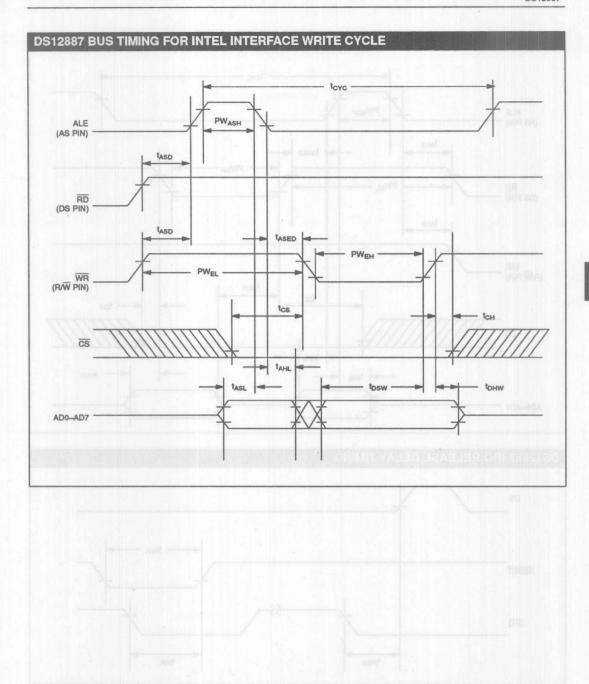
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	tcyc	385		DC	ns	TEBARC
Pulse Width, DS/E Low or RD/WR High	PW <sub>EL</sub>	150		380	ns	OMPIEC.
Pulse Width, DS/E High or RD/WR Low	PW <sub>EH</sub>	125	merego mez bilisega aldi belle vanser	y anotona y e ections e erlods of tit	ns	ne e eran I ni batso di anolib
Input Rise and Fall Time	t <sub>R</sub> ,t <sub>F</sub>			30	ns	
R/W Hold Time	t <sub>RWH</sub>	10		I E E	ns	ALL SEE
R/W Setup Time Before DS/E	t <sub>RWS</sub>	50	- AMBROT		ns	STSMAN,
Chip Select Setup Time Before DS, WR, or RD	t <sub>CS</sub>	20	1 50¥		ns	ligozi tuo
Chip Select Hold Time	t <sub>CH</sub>	0 8.0-	l <sub>a</sub> v		ns	olgo.I tue
Read Data Hold Time	t <sub>DHR</sub>	10		80	ns	
Write Data Hold Time	t <sub>DHW</sub>	0	o sens	LETOARA	ns	OBUBO
Muxed Address Valid Time to AS/ALE Fall	t <sub>ASL</sub>	30	TOBMA		ns	ETEMAR!
Muxed Address Hold Time	t <sub>AHL</sub>	10	190	-	ns	adon I had
Delay Time DS/E to AS/ALE Rise	tASD	25		-	ns	anadan ki
Pulse Width AS/ALE High	PWASH	60			ns	
Delay Time, AS/ALE to DS/E Rise	tASED	40	-		ns	
Output Data Delay Time From DS/E or RD	t <sub>DDR</sub>	20	l Jol	120	ns	0 @ Augn
Data Setup Time	t <sub>DSW</sub>	100	V <sub>TP</sub>		ns	teler9 eth
Reset Pulse Width	t <sub>RWL</sub>	5			μѕ	
IRQ Release from DS	tIRDS			2	μѕ	1107.57
IRQ Release from RESET	t <sub>IRR</sub>	NIM	JOSEMY	2	μs	TEMAR

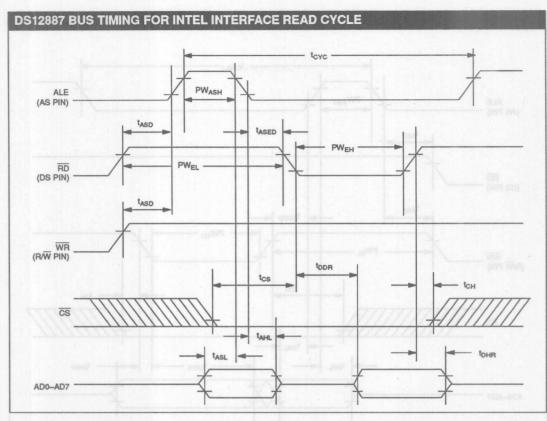
#### NOTES

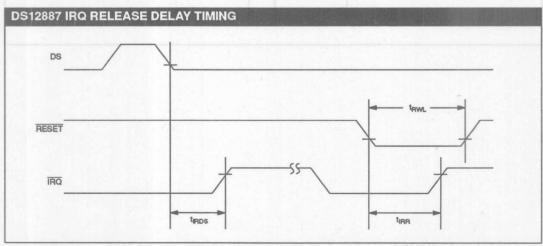
- 1. All voltages are referenced to ground.
- 2. All outputs are open.
- 3. The MOT pin has an internal pulldown of 20  $\,\mathrm{K}\Omega$ .
- Applies to the AD0-AD7 pins, the IRQ pin, and the SQW pin when each is in the high impedance state.
- 5. The IRQ pin is open drain.
- 6. Measured with a load as shown in Figure 4.



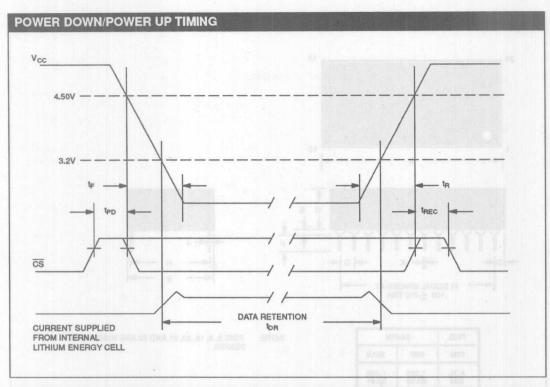












POWER DOWN/POWER UP TIMING								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
CS at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0		0.00 0.00	μѕ			
V <sub>CC</sub> slew from 4.5V to 0V (CS at V <sub>IH</sub> )	t <sub>F</sub>	300		00.6 AE.	μѕ			
V <sub>CC</sub> slew from 0V to 4.5V (CS at V <sub>IH</sub> )	t <sub>R</sub>	100		710 0,140 70 3.00	μѕ			
CS at V <sub>IH</sub> after Power-Up	tREC	20		200	ms			

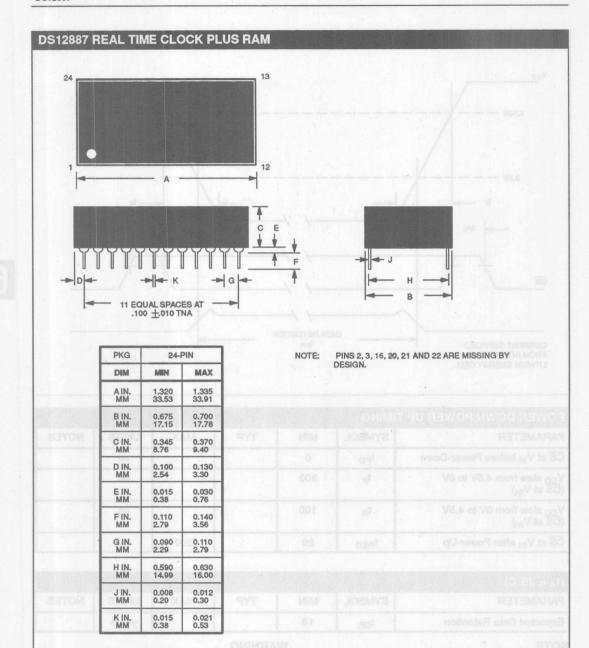
(t <sub>A</sub> = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t <sub>DR</sub>	10		100 L 300	years	

### NOTE

#### WARNING

The real time clock will keep time to an accuracy of  $\pm 1$  minute per month during data retention time for the period of  $t_{DR}$ .

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.



# DS12887A Real Time Clock

#### **FEATURES**

- Drop-in replacement for IBM AT computer clock/ca-
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- · Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- · Binary or BCD representation of time, calendar, and
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
- 14 bytes of clock and control registers
  114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
- End of clock update cycle

### PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

#### **PIN DESCRIPTION**

IRQ

SQW

Vcc

RCLR

GND

ADO-AD7 - Multiplexed Address/Data Bus NC No Connection MOT **Bus Type Selection** CS Chip Select AS - Address Strobe R/W Read/Write Input DS Data Strobe RESET

Reset Input

Interrupt Request Output Square Wave Output

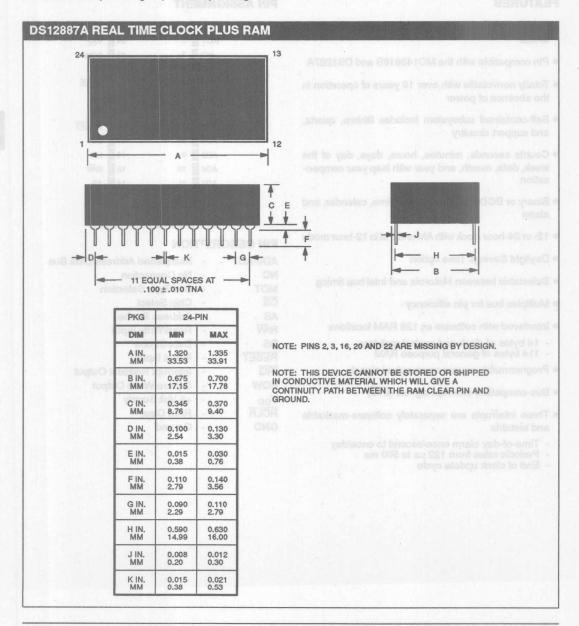
+5 Volt Supply **RAM Clear** 

Ground

#### DESCRIPTION

The DS12887A Real Time Clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The RCLR pin is used to clear (set to logic 1) all 114 bytes of general

purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery back-up mode when  $V_{\rm CC}$  is not applied. The RCLR function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operation, description and specification is identical to the DS12887.





## DS1385/DS1387 RAMified Real Time Clock 4K x 8

#### **FEATURES**

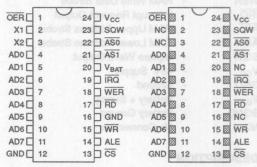
- Upgraded IBM AT computer clock/calendar with 4K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- 4K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 μs to 500 ms
- End-of-clock update cycle
- Available as chip (DS1385 or DS1385S) or stand alone module with embedded lithium battery and crystal (DS1387)

#### ORDERING INFORMATION

DS1385 DS1385S DS1387

RTC Chip; 24 pin DIP RTC Chip; 28 pin SOIC RTC Module; 24 pin DIP

#### **PIN ASSIGNMENT**



DS1385 24-PIN DIP (600 MIL) DS1387 24-PIN ENCAPSULATED PACKAGE (740 MIL FLUSH)



DS1385S 28-PIN SOIC (330 MIL)

#### PIN DESCRIPTION

OER **RAM Output Enable** X1 Crystal Input X2 Crystal Output AD0-AD7 Mux'ed Address/Data Bus CS RTC Chip Select Input ALE **RTC Address Strobe** WR RTC Write Data Strobe RD RTC Read Data Strobe WER RAM Write Data Strobe IRQ Interrupt Request Output AS1 RAM Upper Address Strobe AS0 - RAM Lower Address Strobe SOW Square Wave Output Vcc +5V Supply GND Ground Battery + Supply VBAT - Battery Ground **BGND** NC No Connection

#### DESCRIPTION

The DS1385/DS1387 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 4K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system  $V_{\rm CC}$  by a lithium battery.

The 4K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

#### **OPERATION**

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1385/DS1387. The following paragraphs describe the function of each pin.

#### SIGNAL DESCRIPTIONS

GND,  $V_{CC}$  - DC power is provided to the device on these pins.  $V_{CC}$  is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When  $V_{CC}$  is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the  $V_{BAT}$  pin in the case of the DS1385, or to the internal battery in the case of the DS1387. The timekeeping function maintains an accuracy of  $\pm 1$  minute per month at 25°C regardless of the voltage input on the  $V_{CC}$  pin.

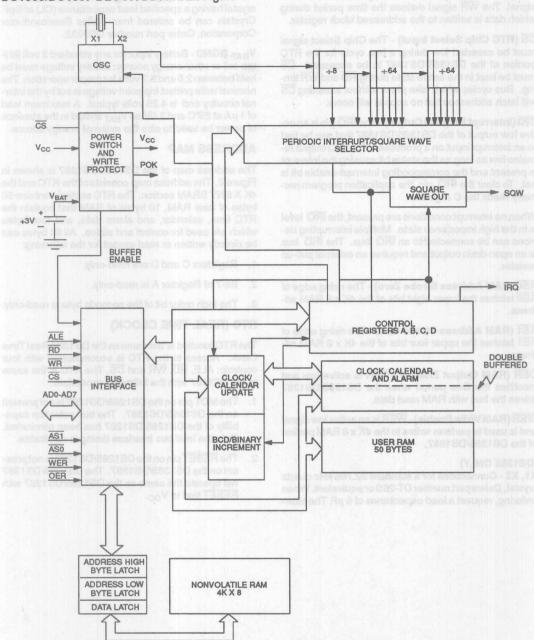
SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when  $V_{CC}$  is less than 4.25 volts typical.

ADO-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1385/DS1387 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, ASO, or AS1, at which time the DS1385/DS1387 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the WR or WER pulses. In a read cycle, the DS1385/DS1387 outputs 8 bits of data during the latter portion of the RD or OER pulses. The read cycle is terminated and the bus returns to a high impedance state as RD or OER transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1385/DS1387.

RD (RTC Read Input) - RD identifies the time period when the DS1385/DS1387 drives the bus with RTC read data. The RD signal is an enable signal for the output buffers of the clock.

## DS1385/DS1387 BLOCK DIAGRAM Figure 1



WR (RTC Write Input) -The WR signal is an active low signal. The WR signal defines the time period during which data is written to the addressed clock register.

CS (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1385/DS1387 to be accessed. CS must be kept in the active state during RD and WR timing. Bus cycles which take place without asserting CS will latch addresses but no access will occur.

 $\overline{\textbf{IRQ}}$  (Interrupt Request Output) - The  $\overline{\textbf{IRQ}}$  pin is an active low output of the DS1385/DS1387 that can be tied to an interrupt input on a processor. The  $\overline{\textbf{IRQ}}$  output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the  $\overline{\textbf{IRQ}}$  pin, the application program normally reads the C register.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  bus is an open drain output and requires an external pull-up resistor.

ASO (RAM Address Strobe Zero) - The rising edge of ASO latches the lower eight bits of the 4K x 8 RAM address.

AST (RAM Address Strobe One) - The rising edge of AST latches the upper four bits of the 4K x 8 RAM address.

OER (RAM Output Enable) - OER is active low and identifies the time period when the DS1385/DS1387 drives the bus with RAM read data.

WER (RAM Write Enable) - WER is an active low signal and is used to perform writes to the 4K x 8 RAM portion of the DS1385/DS1387.

#### (DS1385 ONLY)

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor Corporation. Order part number DS9032.

 $V_{BAT}$ , BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1  $\mu$ A at 25°C and 3.0V on  $V_{BAT}$  should in the absence of power be used to size the external energy source.

#### ADDRESS MAP

The address map of the DS1385/DS1387 is shown in Figure 2. The address map consists of the RTC and the 4K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

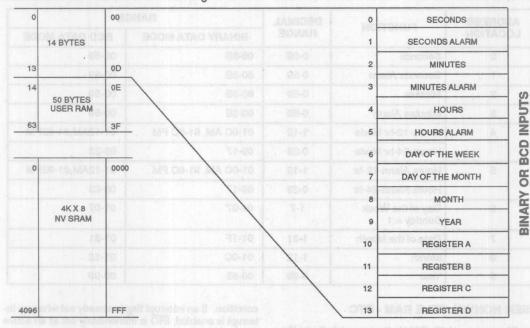
- 1. Registers C and D are read-only.
- 2. Bit-7 of Register A is read-only.
- 3. The high order bit of the seconds byte is read-only.

#### RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, RD, WR and CS. The RTC is the same in the DS1287 with the following exceptions:

- The MOT pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
- The RESET pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The DS1385/DS1387 will operate the same as the DS1285/DS1287 with RESET tied to V<sub>CC</sub>.

### ADDRESS MAP DS1385/DS1387 Figure 2



#### TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected,

the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS	FUNCTION	DECIMAL	RANG	GE
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07 × ×
7 AR	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

#### **USER NONVOLATILE RAM - RTC**

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1385/DS1387. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

#### INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the  $\overline{\mbox{RQ}}$  pin from being asserted from that interrupt

condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{IRQ}$  is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{IRQ}$  pin is asserted low.  $\overline{IRQ}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{IRQ}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

#### **OSCILLATOR CONTROL BITS**

When the DS1385/DS1387 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register

A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off

#### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

### PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t <sub>Pl</sub> PERIODIC INTERRUPT RATE	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	riskly plasting togethed of n	3.90625 ms	256 Hz
0	mee 0 d	uoria 1 straet	0	7.8125 ms	128 Hz
0	0	. 1	is cycle.	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz
0	1	1	0	976.5625 μs	1.024 kHz
0	1 .	1	1	1.953125 ms	512 Hz
1	0	0	cus IO	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

#### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{IRQ}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

#### **UPDATE CYCLE**

The DS1385/DS1387 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an

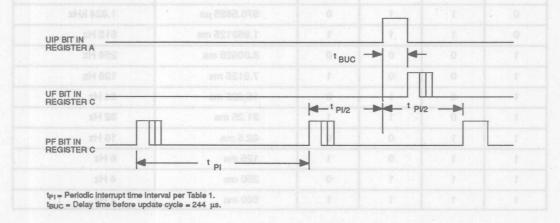
alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t<sub>BUC</sub> allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t<sub>P</sub>/2+t<sub>BUC</sub>) to ensure that data is not read during the update cycle.





#### 

The DS1385/DS1387 has four control registers which are accessible at all times, even during the update cycle.

#### **REGISTER A**

MSE	3						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

- 1. Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit;
- 3. Enable both at the same time and the same rate; or
- 4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

#### **REGISTER B**

MSB							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BITO
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the

time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1385/DS1387.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the IRQ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the IRQ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1385/DS1387 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The internal functions of the DS1385/DS1387 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag (UF) bit in Register C to assert IRQ. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/ write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

### REGISTER Commented in the state of the series of the serie

MSE	1						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 AF = AIE = 1 UF = UIE = 1

i.e., IRQF = (PF · PIE) + (AF · ALE) + (UF · UIE)

Any time the IRQF bit is a one, the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the  $\overline{\mbox{IRQ}}$  signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the  $\overline{\text{IRQ}}$  pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

#### REGISTER D

MSE	30mmile						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the

contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0** - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

### **4K X 8 RAM**

The D\$1385/D\$1387 provides 4K x 8 of on-chip \$RAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 4K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to FFFH.

Four control signals,  $\overline{AS0}$ ,  $\overline{AS1}$ ,  $\overline{OER}$ , and  $\overline{WER}$ , are used to access the 4K x 8 SRAM. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ( $\overline{AS0}$ ) and Address Strobe 1 (AS1) signals.  $\overline{AS0}$  is used to latch the lower 8-bits of address, and  $\overline{AS1}$  is used to latch the upper 4-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM (WER) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM (OER) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The WER and OER signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via CS) must not be attempted when the 4K x 8 RAM is being accessed. The RAM is enabled when either WER or OER is active. CS is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 50 bytes of user RAM.

6

### ABSOLUTE MAXIMUM RATINGS\*

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature

-0.3V to +7.0V 0°C to 70°C -40°C to +70°C 260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	- 1
Input Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1
Battery Voltage	V <sub>BAT</sub>	2.5		3.7	/ V / /	9

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	Icc1		35	50	mA	2
Standby Current CS, OER, and WER = V <sub>CC</sub> -0.3V	I <sub>CC2</sub>		1	5.0	mA	6
Input Leakage	I <sub>IL</sub>	-1.0	GARRAD	+1.0	μА	3
I/O Leakage	ILO	-1.0		+1.0	μА	3
Output @ 2.4V	Іон	-1.0			mA	1,4
Output @ 0.4V	loL		/	4.0	mA	1

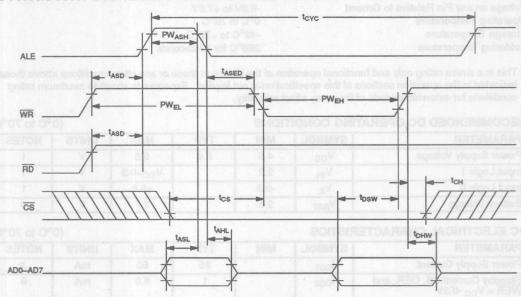
### RTC AC TIMING CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 4.5V to 5.5V)

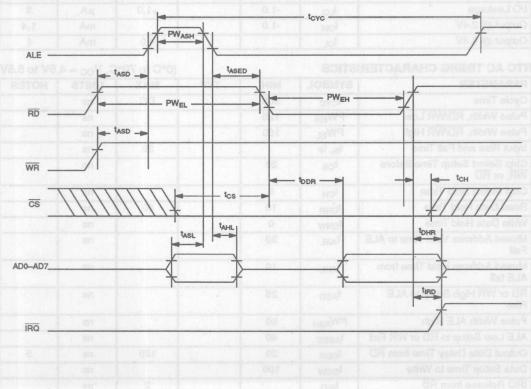
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	tcyc	305		DC	ns	
Pulse Width, RD/WR Low	PWEH	125			ns	- 51
Pulse Width, RD/WR High	PW <sub>EL</sub>	150		- leb- 170	ns	
Input Rise and Fall Time	t <sub>R</sub> , t <sub>F</sub>			30	ns	
Chip Select Setup Time Before WR, or RD	tcs	20			ns	FINE
Chip Select Hold Time	t <sub>CH</sub>	0	150	1777	ns	
Read Data Hold Time	tDHR	10		80	ns	90
Write Data Hold Time	t <sub>DHW</sub>	0	not l		ns	
Muxed Address Valid Time to ALE Fall	t <sub>ASL</sub>	30	/		ns	
Muxed Address Hold Time from ALE fall	t <sub>AHL</sub>	10		2	ns	_508-008
RD or WR High Setup to ALE Rise	tASD	25			ns	
Pulse Width ALE High	PWASH	60			ns	200
ALE Low Setup to RD or WR Fall	tased	40			ns	
Output Data Delay Time from RD	t <sub>DDR</sub>	20		120	ns	5
Data Setup Time to Write	t <sub>DSW</sub>	100			ns	
IRQ Release from RD	t <sub>IRD</sub>			2	μѕ	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### DS1385/DS1387 BUS TIMING FOR WRITE CYCLE TO RTC



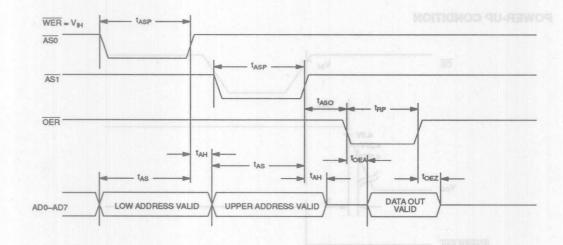
### DS1385/DS1387 BUS TIMING FOR READ CYCLE TO RTC



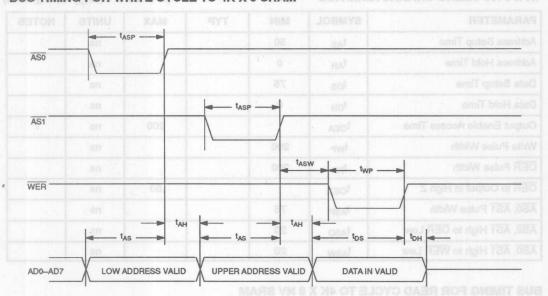
4K X 8 AC TIMING CHARACTERISTICS (0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t <sub>AS</sub>	50		parties of	ns	
Address Hold Time	t <sub>AH</sub>	0			ns	CSA.
Data Setup Time	t <sub>DS</sub>	75			ns	
Data Hold Time	t <sub>DH</sub>	0	testest		ns	
Output Enable Access Time	toea	1	1	200	ns	7
Write Pulse Width	t <sub>WP</sub>	200			ns	
OER Pulse Width	t <sub>RP</sub>	200			ns	
OER to Output in High Z	†OEZ			.50	ns	naw.
AS0, AS1 Pulse Width	t <sub>ASP</sub>	75			ns	
AS0, AS1 High to OER Low	t <sub>ASO</sub>	20	ns!		ns	
AS0, AS1 High to WER Low	t <sub>ASW</sub>	20			ns	

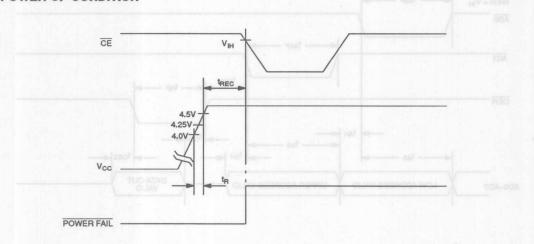
### **BUS TIMING FOR READ CYCLE TO 4K X 8 NV SRAM**



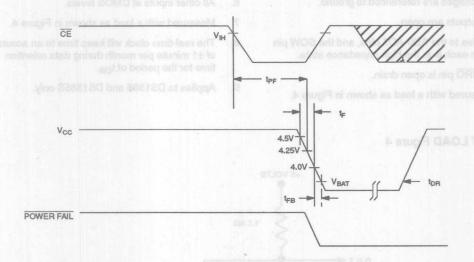
### **BUS TIMING FOR WRITE CYCLE TO 4K X 8 SRAM**



### **POWER-UP CONDITION**



### **POWER-DOWN CONDITION**



POWER-UP POWER-DOWN TIMING

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE High to Power Fail	tpF		H	0	ns	
Recovery at Power Up	t <sub>REC</sub>		150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤V <sub>CC</sub> ≤ 4.5V	300			μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤V <sub>CC</sub> ≤ 4.0V	10			μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC≥</sub> 4.0V	0			μѕ	
Expected Data Retention	t <sub>DR</sub>	10			years	8

### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			12	pF	
Output Capacitance	C <sub>OUT</sub>			12	pF	

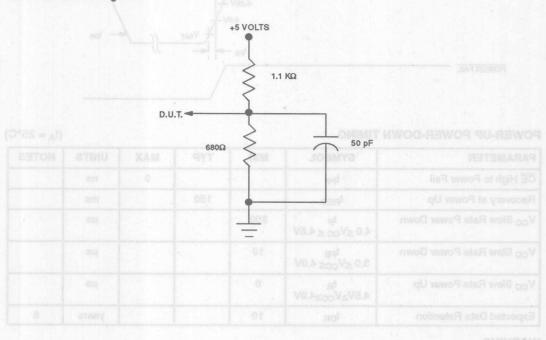
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### NOTES

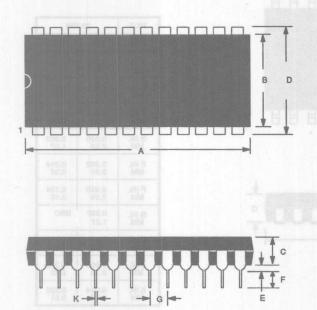
- 1. All voltages are referenced to ground.
- 2. All outputs are open.
- Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
- 4. The IRQ pin is open drain.
- 5. Measured with a load as shown in Figure 4.

- 6. All other inputs at CMOS levels.
- 7. Measured with a load as shown in Figure 4.
- The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t<sub>DR</sub>.
- 9. Applies to DS1385 and DS1385S only.

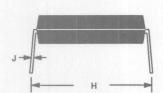
### **OUTPUT LOAD Figure 4**



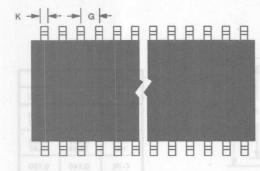




PKG	24-	PIN
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.26
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
EIN.	0.015	0.050
MM	0.38	1.27
FIN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
KIN.	0.015 0.38	0.022



### **DS1385S 28 PIN SOIC**



		<b>1</b>	AIN.	0.706 17.93	0.728 18.49
			B IN.	0.338 8.58	0.350 8.89
			C IN.	0.086 2.18	0.110 2.79
			D IN.	0.020 0.58	0.050 1.27
			E IN.	0.002 0.05	0.014 0.36
050.0	aro.o	<u>↓</u>	F IN.	0.090 2.29	0.124 3.15
	JUU	00 000000°	G IN.	0.050 1.27	BSC
anta eva	0.090	A	H IN.	0.460 11.68	0.480 12.19
			JIN.	0.006 0.15	0.013 0.33
			KIN.	0.014	0.020

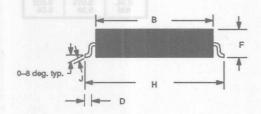
PKG

DIM

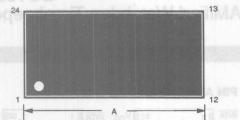
28-PIN

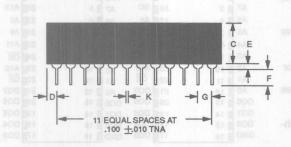
MAX

MIN



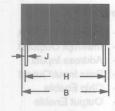
### DS1387 24 PIN 740 MIL FLUSH ENCAPSULATED







PKG	24-PIN			
DIM	MIN	MAX		
AIN.	1.320	1.335		
MM	33.53	33.91		
B IN.	0.720	0.740		
MM	18.29	18.80		
C IN.	0.345 8.76	0.370 9.40		
D IN.	0.100	0.130		
MM	2.54	3.30		
E IN.	0.015 0.38	0.030 0.89		
FIN.	0.110	0.140		
MM	2.79	3.56		
G IN.	0.090	0.110		
MM	2.29	2.79		
H IN.	0.590 14.99	0.630 16.00		
J IN.	0.008	0.012		
MM	0.20	0.30		
KIN.	0.015 0.38	0.021 0.53		



NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

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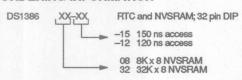


## DS1386 RAMified Watchdog Timekeeper

#### **FEATURES**

- 8K or 32K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 28-pin JEDEC footprint when lower justified
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave output
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V<sub>CC</sub>
- Interrupt signals are active in power-down mode

### **ORDERING INFORMATION**



### **PIN ASSIGNMENT**

INTA	8 1	32 🛭 V <sub>C</sub>	C INTA I 1	325 VCC
INTE	3 8 2	31 8 80		318 SQW
NO	33	30 B VC		308 V <sub>CC</sub>
A1:	2 8 4	29 W		298 WE
A	7 8 5	28 NO		288 A13
A	6 8 6	27 A8		278 A8
A	5 0 7	26 A9		268 A9
A	4 8 8	25 A1		258 A11
A	3 9 9	248 0		248 OE
A	2 8 10	23 A1	0 A2 3 10	23g A10
A	1 8 11	22 C		228 CE
A	0 12	21 DC	27 A0 3 12	21g DQ7
DQ	0 3 13	20 DC	26 DQ0 3 13	20g DQ6
DQ	1 1 14	198 DC	25 DQ1 3 14	198 DQ5
DQ	2 15	18 DC	24 DQ2 3 15	18g DQ4
GN	D 🛭 16	17 DC	33 GND 3 16	17g DQ3

DS1386 8K x 8 32-Pin Encapsulated Package DS1386 32K x 8 32-Pin Encapsulated Package

#### PIN DESCRIPTION

INTA - Interrupt Output A INTB(INTB) Interrupt Output B A0-A14 Address Inputs DQ0-DQ7 Data Input/Output CE Chip Enable OE **Output Enable** WE Write Enable +5 Volts Vcc GND Ground

SQW - Square Wave Output NC - No Connection

#### DESCRIPTION

The DS1386 RAMified Watchdog Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1386 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 8K or 32K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide

static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of  $V_{CC}$  and write protects memory when  $V_{CC}$  is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of  $V_{CC}$ . Timekeeper information includes hundredths of seconds, seconds, minutes,

6

hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AMVPM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

### **OPERATION - READ REGISTERS**

The DS1386 executes a read cycle whenever WE (Write Enable) is inactive (High) and  $\overline{\text{CE}}$  (Chip Enable) and  $\overline{\text{OE}}$  (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A14) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t<sub>ACC</sub> (Access Time) after the last address input signal is stable, providing that  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  access times are also satisfied. If  $\overline{\text{OE}}$  and  $\overline{\text{CE}}$  access times are not satisfied, then data access must be measured from the latter occurring signal ( $\overline{\text{CE}}$  or  $\overline{\text{OE}}$ ) and the limiting parameter is either  $t_{\text{CO}}$  for  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  for  $\overline{\text{OE}}$  rather than address access.

#### **OPERATION - WRITE REGISTERS**

The DS1386 is in the write mode whenever the WE (Write Enable) and CE (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery state (twn) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t<sub>DS</sub>) and Data Hold Time (t<sub>DH</sub>) with respect to the earlier rising edge of CE or WE. The OE control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active), then WE will disable the outputs in topw from its falling edge.

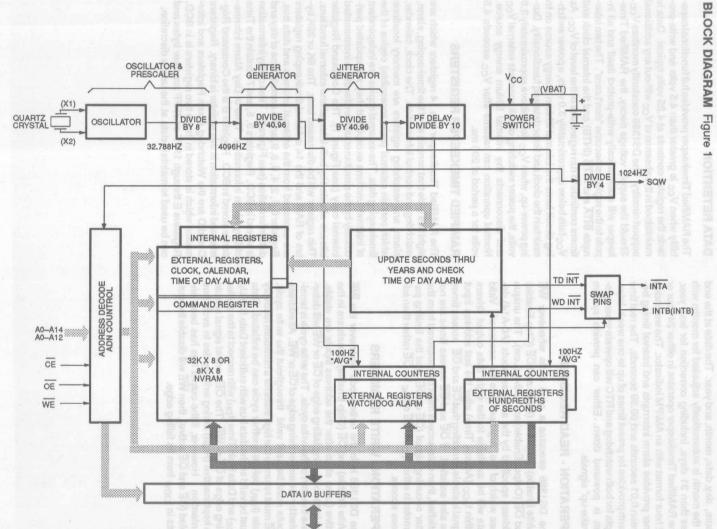
### DATA RETENTION STUDE MARIOARD MOOJE

The RAMified Timekeeper provides full functional capability when V<sub>CC</sub> is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of V<sub>CC</sub> without any additional support circuitry. The DS1386 constantly monitors V<sub>CC</sub>. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts INTA and INTB (INTB) and the internal clock and timers continue to run regardless of the level of V<sub>CC</sub>. As V<sub>CC</sub> falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V<sub>CC</sub> rises above approximately 3.0 volts, the power switching circuit connects external V<sub>CC</sub> and disconnects the internal lithium energy source. Normal operation can resume after V<sub>CC</sub> exceeds 4.5 volts for a period of 200 ms.

### **RAMIFIED TIMEKEEPER REGISTERS**

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) copies of the timekeeping data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 8K or 32K bytes of RAM and the 14 external timekeeping registers are accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Registers E through 1FFF or 7FFF are user bytes and can be used to maintain data at the user's discretion.

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DQ0-DQ7

#### TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic 0, EOSC (Bit 7) enables the Real Time Clock oscillator. This bit is set to logic 1 as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 31). When set to logic 0, the Square Wave Output Pin will output a 1024 Hz Square Wave Signal. When set to logic 1 the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic 1, the 12 Hour Format is selected. In the 12 Hour Format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24 Hour Mode, bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic 0. This will freeze the External Time of Day Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic 1, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the

same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

#### TIME OF DAY ALARM REGISTERS

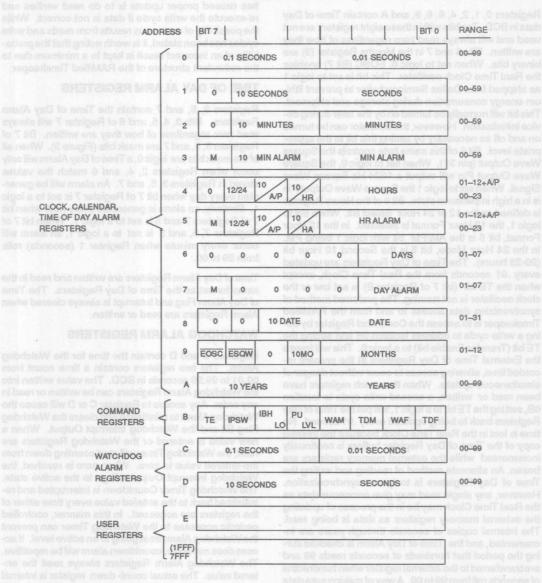
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic 0, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic 1. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

### **WATCHDOG ALARM REGISTERS**

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count-down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

### DS1386 RAMIFIED WATCHDOG TIMEKEEPER REGISTERS Figure 2



# 6

### TIME OF DAY ALARM MASK BITS Figure 3

REGISTER		no non	EMPERATURE APERATURE
(3)MINUTES	(5)HOURS	(7)DAYS	EMPERATURE
1	1	1	ALARM ONCE PER MINUTE
edul Oede of	id. Exposure	igmi ton air	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

#### **COMMAND REGISTER**

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, INTA is the Time of Day Alarm and INTB/(INTB) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. INTA is now the Watchdog Alarm output and INTB/(INTB) is the Time of Day Alarm output.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V<sub>CC</sub> is applied, INTB/(INTB) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, INTA and INTB/(INTB) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and INTA will sink current for a minimum of 3 ms and then release. INTB/(INTB) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be acti-

vated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF-Bit 0 Time of Day Flag-This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO +7.0V 0°C TO 70°C -40°C TO + 70°C 260°C FOR 10 SECONDS

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	٧	10
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	V	10
Input Logic 0	i etale berevitoViLniT	-0.3	egister whe	+0.8	on O'Vn is ti	10

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

to a logic 0, the Watchdog Interrupt output will be acti-

PARAMETER - MANAGEMENT AND A VISCO	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	i adijetos i	-1.0	de or writes w	+1.0	μА	sk register
Output Leakage Current	lo	-1.0	or also we belon	+1.0	μА	c 1 to allo
I/O Leakage Current	ILIO	-1.0	o a logic 1, IN	+1.0	μА	W-Biteld
Output Current @ 2.4V	loh	-1.0	ovavy em ar (e vo erif semay	o nu respon o O, this bit n	mA	ie rime or Alarm. W
Output Current @ 0.4V	loL	en al b	is fuquo mas	4.0	mA	13
Standby Current CE = 2.2V	I <sub>CCS1</sub>	The last	3.0	7.0	mA	BIE-ON
Standby Current CE = V <sub>CC</sub> -0,5	I <sub>CCS2</sub>	ortW (	2.0	4.0	mA	of the sittle
Active Current	Icc	(not) 0	airent (see D	85	MA Is	bit is set !
Write Protection Voltage	V <sub>TP</sub>		4.25		V	PERMISSIN

### CAPACITANCE

bas ATVI, 0 oigol a of les nadW Jangle (tA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	selloV -b	eceb 7 nemu	15	pF	(STIVITS)
Output Capacitance	C <sub>OUT</sub>	(noli lin	7	15	pF	on me ou
Input/Output Capacitance	C <sub>VO</sub>	10	al sid Zidt ner	15	pF	V 8 118 - MJ

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to } +70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 10\%)$ 

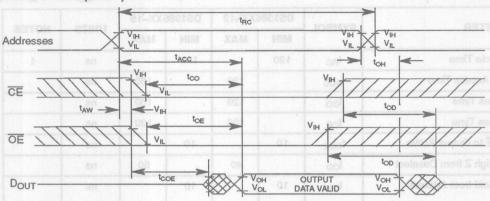
	OVIMBOL	DS1386XX-12		DS1386XX-15		LINUTO	MATTE
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120	-45-	150		ns	1
Address Access Time	tACC		120	co) .	150	ns	7
CE Access Time	tco		120	1	150	ns	
OE Access Time	toE		100	30	120	ns	
OE or CE to Output Active	tcoe	10		10	N KK	ns	ZZ 3
Output High Z from Deselect	top		40		50	ns	
Output Hold from Address Change	t <sub>OH</sub>	10		10		ns	Tuo
Write Cycle Time	twc	120		150	les 2, 6,	ns	YO STIP
Write Pulse Width	t <sub>WP</sub>	110		140		ns	3
Address Setup Time	t <sub>AW</sub>	0		0	30	ns	gestaenb
Write Recovery Time	t <sub>WR</sub>	10		15	1000	ns	
Output High Z from WE	topw		40	11/1	50	ns	CE N
Output Active from WE	toew	10		10		ns	4977
Data Setup Time	t <sub>DS</sub>	85	J.V	110	7187	ns	4
Data Hold Time	t <sub>DH</sub>	10		15		ns	4,5
INTA, INTB Pulse Width	t <sub>IPW</sub>	3		3	00	ms	11,12

### **AC TEST CONDITIONS**

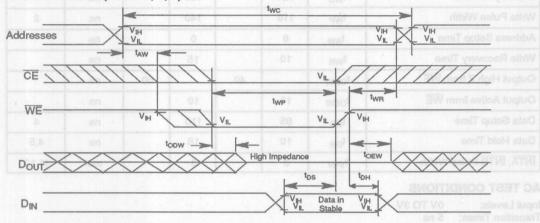
OV TO 3V

Input Levels: 0V To Transition Times: 5 ns

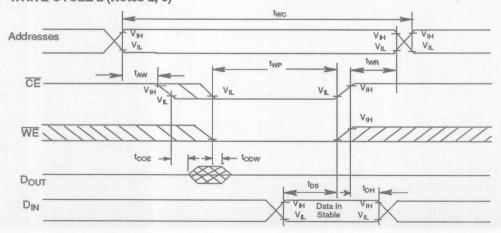
### READ CYCLE (Note1)



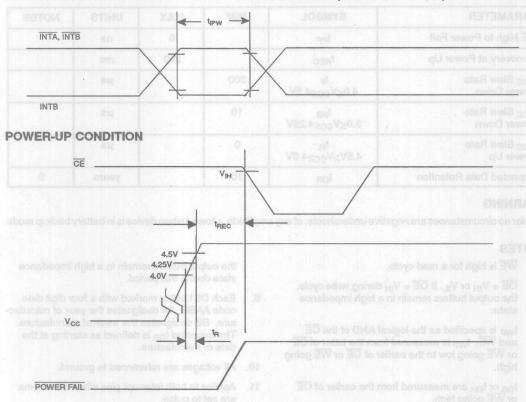
### WRITE CYCLE 1 (Notes 2, 6, 7)



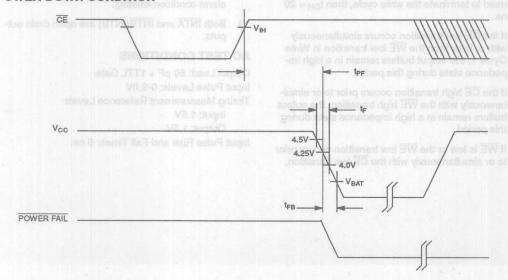
### WRITE CYCLE 2 (Notes 2, 8)



### TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



### **POWER-DOWN CONDITION**



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### AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
CE High to Power Fail	t <sub>PF</sub>		0	ns	THE ATTE
Recovery at Power Up	tREC	7	200	ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0≤V <sub>CC</sub> ≤4.5V	300	4	μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0≤V <sub>CC≤</sub> 4.25V	10		μs	6131
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC</sub> ≥4.0V	0		μѕ	
Expected Data Retention	t <sub>DR</sub>	10		years	9

### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

#### NOTES

- WE is high for a read cycle.
- OE = VIH or VIL. If OE = VIH during write cycle, the output buffers remain in a high impedance
- two is specified as the logical AND of the CE and WE. twp is measured from the latter of CE or WE going low to the earlier of CE or WE going
- t<sub>DS</sub> or t<sub>DH</sub> are measured from the earlier of CE or WE going high.
- t<sub>DH</sub> is measured from WE going high. If CE is used to terminate the write cycle, then tDH = 20
- If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition,

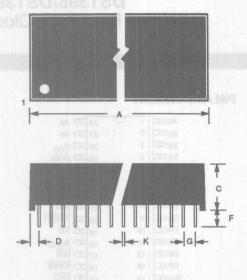
- the output buffers remain in a high impedance state during this period.
- Each DS1386 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DR</sub> is defined as starting at the date of manufacture.
- 10. All voltages are referenced to ground.
- 11. Applies to both interrupt pins when the alarms are set to pulse.
- 12. Interrupt output occurs within 100 ns on the alarm condition existing.
- 13. Both INTA and INTB(INTB) are open drain outputs.

### **AC TEST CONDITIONS**

Output Load: 50 pF + 1TTL Gate Input Pulse Levels: 0-3.0V Timing Measurement Reference Levels Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5 ns.

### **DS1386 32 PIN 740 MIL MODULE**



PKG	32-F	PIN
DIM	MIN	MAX
A IN.	1.720 43.69	1.740 44.20
B IN. MM	0.720 18.29	0.740 18.80
C IN.	0.395 10.03	0.415 10.54
D IN.	0.090 2.29	0.120 3.05
E IN. MM	0.017 0.43	0.030 0.76
F IN.	0.120 3.05	0.160 4.06
G IN.	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021 0.53





Time-of-day alarm once/second to once/day
Periodic rates from 122 µs to 500 ms
End-of-clock update cycle
8-pin VEDEO footprint
valiable as chip (DS1395/OS1395S) onstand alo
valiable with embodded lithium battery and crystal
DERING INFORMATION
1395
RTC Chip; 28 pin DIP



## DS1395/DS1397 **RAMified Real Time Clock**

### **FEATURES**

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 kHz
- Totally nonvolatile with over 10 years of operation in the absence of power
- · Self-contained subsystem includes lithium, quartz, and support circuitry
- · Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- · Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 register/RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general and control registers Separate 4K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
- Time-of-day alarm once/second to once/day
- Periodic rates from 122 µs to 500 ms
- End-of-clock update cycle
- 28-pin JEDEC footprint
- Available as chip (DS1395/DS1395S) or stand alone module with embedded lithium battery and crystal

#### **ORDERING INFORMATION**

DS1395	RTC Chip; 28 pin DIP
DS1395S	RTC Chip; 28 pin SOIC
DS1397	RTC Module; 28 pin DIP

#### **PIN ASSIGNMENT**

A0 III	1	28 III A2
A1 CC	2	27 D A3
Х2Ш	3	26 VDD
X1 🗆	4	25 1 SQW
STBY	5	24 III A4
DO CIL	6	23 III A5
D1	7	22 VBAT
D2CIC	8	21 IRQ
D3CIC	9	20 RESET
D4OC	10	19 🔟 RD
D5 CCC	11	18 BGND
D6 CIC	12	17 - WR
D7 🗆	13	16 XRAM
VSS	14	15 TO RTC

### DS1395S 28-Pin SOIC (330 mil)

				_
A0 [	1	~	28	] A2
A1 [	2		27	] A3
X2[	3		26	VDD
X1 [	4		25	sow
STBY	5		24	] A4
Do	6		23	] A5
D1 [	7			VBAT
D2[	8		21	IRQ
D3[	9		20	RESE
D4[	10		19	RD
D5 [	11		18	BGND
D6			17	WR
D7 [	13		16	XRAM
VSS	14		15	RTC

#### DS1395 28-Pin DIP (600 mil)

AO	₫ 1	28	A2
A1	2	27 🛭	АЗ
NC	3	26 🛭	VDD
NC	3 4	25 🛭	SQW
STBY	3 5	24	
D0	9 6	23	
D1	3 7	22 🛭	NC
D2	8 8	21 🛭	IRQ
D3	9	20 🛭	RESE
D4	☑ 10	19 🛭	RD
D5	3 11	18 🛭	NC
D6	12		WR
D7	13		XRAM
Vss	3 14	15 🛭	RTC

DS1397 28-Pin Encapsulated Package (720 mil)

### PIN DESCRIPTIONS

V<sub>DD</sub>, V<sub>SS</sub> – Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 – Data Bus (bidirectional): Data is written into the device from the data bus if either  $\overline{XRAM}$  or  $\overline{RTC}$  is asserted during a write cycle at the rising edge of a  $\overline{WR}$  pulse. Data is read from the device and driven onto the data bus if either  $\overline{XRAM}$  or  $\overline{RTC}$  is asserted during a read cycle when the  $\overline{RD}$  signal is low.

A0-A5 – Address Bus (input): Various internal registers of the device are selected by these lines. When RTC is asserted, A0 selects between the indirect address register and RTC data register. When the XRAM is asserted, A0-A5 addresses a 32-byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

RD - Read Strobe (Input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either RTC or XRAM is asserted.

WR - Write Strobe (Input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the XRAM or RTC signals.

STBY - Standby (Input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the  $\overline{\text{STBY}}$  signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition ( $V_{DD}$  is 4.25 volts, typical) is negated, whichever occurs first.

RTC - Real Time Clock Select (Input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when RD is low. Data is received from the bus when WR is pulsed low and then high.

**SQW - Square Wave (output):** Frequency selectable output. Frequency is selected by setting register A bits RS0-RS3. See Table 2 for frequencies that can be selected

XRAM - Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are accessible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM pointed to by the page register. Data is driven onto the data bus when RD is low. Data is received from the bus when WR is pulsed low and then high.

IRQ - Interrupt Request (output): The IRQ signal is an active low, open drain output that is used as a processor interrupt request. The IRQ output follows the state of the IRQF bit (bit 7) in status register C. IRQ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

RESET - Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When RESET is low, the following occurs.

- 1. The following register bits are cleared:
  - a. Periodic interrupt (PIE)
  - b. Alarm interrupt enable (AIE)
  - c. Update ended interrupt (UF)
  - d. Interrupt request flag (IRQF)
  - e. Periodic interrupt flag (PF)
  - f. Alarm interrupt flag (AF)
  - g. Square wave output enable (SQWE)
  - h. Update ended interrupt enable (UIE)
- 2. The IRQ pin is in the high impedance state.
- 3. The RTC is not processor accessible.

#### ADDITIONAL PIN DESCRIPTION

(FOR DS1395, DS1395S)

**X1, X2** – Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance ( $C_L$ ) of 6pF.

 $V_{BAT}$ — Battery input for any standard +3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x  $V_{BAT}$ . A maximum load of 1  $\mu$ A at 25°C and 3.0V on  $V_{BAT}$  in the absence of power should be used to size the external energy source.

B<sub>GND</sub> – Battery ground: This pin or pin 14 can be used for the battery ground return.

### **OPERATION**

Power-Down/Power-Up: The real time clock will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V<sub>DD</sub>. When the voltage level applied to the V<sub>DD</sub> input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When  $V_{DD}$  falls below the CE<sub>THR</sub> (4.25 volts typical), the chip select inputs  $\overline{\text{RTC}}$  and  $\overline{\text{XRAM}}$  are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When  $V_{DD}$  falls below 3.2 volts (typical), the module is switched over to an internal power source in the case of the DS1397, or to an external battery connected to the  $V_{BAT}$  and BGND pins in the case of the DS1395 and DS1395S, so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when RTC is asserted low and represents the real time clock. The second set of registers is active when XRAM is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

- Registers C and D are Read Only (status information)
- 2. Bit 7 of register A is Read Only
- 3. Bit 7 of the "Seconds" byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 128 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 128 pages of nonvolatile memory available. The address of

the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/O spaces. (See Figure 3.)

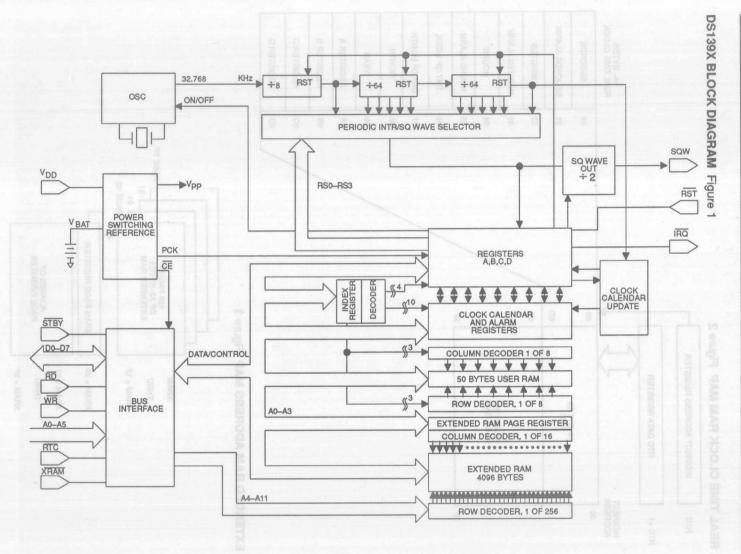
### TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.



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### **REAL TIME CLOCK RAM MAP** Figure 2 INDIRECT ADDRESS REGISTER RTC RTC +1 RTC DATA REGISTER 14-BYTES REAL TIME CLOCK INDIRECT 00 00 00 SECONDS 14-BYTES RTC SECONDS ALARM 01 0D 02 MINUTES 0E MINUTES ALARM 03 50-BYTES USER RAM 04 HOURS HOURS ALARM 05 3F 06 DAY OF WEEK DAY OF MONTH 07 08 MONTH YEAR 09 OA REGISTER A OB REGISTER B 0C REGISTER C OD REGISTER D **EXTENDED RAM ADDRESS MAP** Figure 3 XRAM 128 PAGES PAGE 7F OF 32-BYTES THRU EXTENDED RAM 02 01 XRAM + 1F PAGE 00 XRAM + 20 XRAM PAGE REGISTER XRAM + 21 ALIASES OF PAGE REGISTER THRU XRAM + 3F

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS	FUNCTION	DECIMAL	mobal en mon begg RANGE (30 30 2130 en ne			
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE		
0 0	Seconds	0-59	00-3B	00-59		
e eorp of am	Seconds Alarm	0-59	00-3B atallogs and must lis	00-59		
2	Minutes	0-59	00-3B	00-59		
3	Minutes Alarm	0-59	00-3B	00-59		
nd A 4 mice A	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM		
	Hours-24-hr Mode	0-23	00-17	00-23		
5 14 3	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM		
	Hours Alarm-24-hr	0-23	00-17	00-23		
en ken eit ti	Day of the Week Sunday = 1	1-7 1 eno aluq	01-07 off residence A netal	01-07		
7	Date of the Month	1-31	01-1F	01-31		
8	Month	1-12	01-0C	01-12		
9	Year	0-99	00-63	00-99		

### USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1395/DS1397. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

#### INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the IRQ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, IRQ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{\mbox{IRQ}}$  pin is asserted low.  $\overline{\mbox{IRQ}}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{\mbox{IRQ}}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1395/DS1397. The act of reading Register C clears all active flag bits and the IRQF bit.

### **OSCILLATOR CONTROL BITS**

When the DS1395/DS1397 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

#### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator.

Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{\text{IRQ}}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

### PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

S	ELECT BITS	REGISTER	A	t <sub>PI</sub> PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0 100	0	of to O observe	None	None
0	0	0	Idane Luoritte	3.90625 ms	256 Hz
0	0	indication is	0	7.8125 ms	128 Hz
0	0	itioris <b>t</b> raso ,	ead, Howeve	122.070 µs	8.192 kHz
0	aFiriti1/bebu	0	0	244.141 μs	4.096 kHz
0	ens. (noiri) so	0	wole. All bit	488.281 μs	2.048 kHz
0	high art pend	w alqtmetrii	0	976.5625 μs	1.024 kHz
0	o setvlnen ro	dnes <b>1</b> ideer	One, tula, or ti	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
Sult ristor	borlom eg	seur fio <sup>0</sup> pal7 e	ritemative aff	7.8125 ms	128 Hz
negles sid	0	ins replW .s	0	15.625 ms	64 Hz
24 <b>1</b> 00 ga	as b0 reses	llow. IRQ is	enes <b>1</b> s el nic	31.25 ms	32 Hz
w Ino a s	Orate Day	0	0	62.5 ms	16 Hz
1 de l'imi	ven low. Det	0	OAI gremey	125 ms	8 Hz
1 (fid	ORI) 1 tid ni	no ci <b>t</b> ol A .	net Oeff po	250 ms	4 Hz
1	of reading Re	105 all 70	racivies rac	500 ms	2 Hz

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### UPDATE CYCLE

The DS1395/DS1397 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

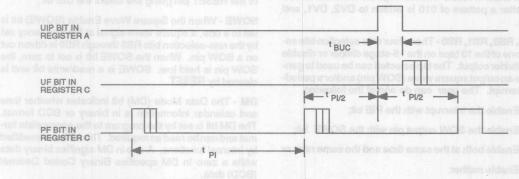
There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date in-

formation. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt rou-

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244  $\mu s$  later. If a low is read on the UIP bit, the user has at least 244  $\mu s$  before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244  $\mu s$ .

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within  $(t_{PV}/2+t_{BUC})$  to ensure that data is not read during the update cycle.

### UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



 $t_{Pl}$  = Periodic interrupt time interval per Table 1.  $t_{BUC}$  = Delay time before update cycle = 244  $\mu$ s.

### REGISTERS

The DS1395/DS1397 has four control registers which are accessible at all times, even during the update cycle.

#### **REGISTER A**

MSE	MSB As arrows referred at a product of the Book							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BITO	
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

- Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit;
- 3. Enable both at the same time and the same rate; or
- 4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

### REGISTER B

	MSE							LSB
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in

a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1395/DS1397.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{IRQ}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{IRQ}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{IRQ}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1395/DS1397 functions but is cleared by the hardware  $\overline{RESET}$  signal.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The internal functions of the DS1395/DS1397 do not affect the AIE bit but is cleared by RESET.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert IRQ. The SET bit going high or the RESET pin going low clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit and is cleared by RESET.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/ write.

DSE - The Daylight Savings Enable (DSE) bit is a read/ write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

MSE	MSB							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BITO	
IRQF	PF	AF	UF	0	0	0	0	

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 AF = AIE = 1

UF = UIE = 1 i.e., IRQF = (PF ● PIE) + (AF ● AIE) + (UF ● UIE)

Any time the IRQF bit is a one, the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET pin is low.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the IRQ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C or by RESET.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one

will appear in the IRQF bit. A read of Register C or a RE-SET will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ pin. UF is cleared by reading Register C or by RESET.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

### REGISTER D

MSE	3						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0** - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.



### **ABSOLUTE MAXIMUM RATINGS\***

V<sub>DD</sub> Pin Potential to Ground Pin Input Voltage Power Dissipation Storage Temperature Ambient Temperature Soldering Temperature -0.3V to +7.0V V<sub>SS</sub> - 0.3 to V<sub>DD</sub> + 0.3V 500 mW -40°C to +70°C 0°C to +70°C 260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage	0 0 0 00	Vcc	4.5	5.5	٧	o mango
Input High Voltage	Recognized as a High Signal Over Recommended V <sub>DD</sub> and t <sub>A</sub> Range	V <sub>IH</sub>	2.2	V <sub>DD</sub> + 0.3	V	is al dold
Input Low Voltage	Recognized as a Low Signal Over Recommended V <sub>DD</sub> and t <sub>A</sub> Range	V <sub>IL</sub>	-0.3	0.8	٧	o mebre
Battery Voltage	and of contents of the RTC data aged	V <sub>BAT</sub>	2.5	3.5	V	did ROF

### DC ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 5.0V \pm 10\%, V_{SS} = 0V, t_A = 0^{\circ} C \text{ to } 70^{\circ}C)$ 

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Input Leakage V <sub>IL</sub> =0V, V <sub>IH</sub> =V <sub>DD</sub>	For any Single Pin: D0-7, RD, WR, A0-5, XRAM, RTC, RESET	lı		±1	μА	
Output High Voltage	e V <sub>DD</sub> =5.0V I <sub>LOAD</sub> =1 mA		2.4		٧	
Output Low Voltage	V <sub>DD</sub> = 5.0V I <sub>LOAD</sub> = 4 mA	V <sub>OL</sub>		0.4	٧	
Power Supply Current	Outputs Unloaded	I <sub>DD</sub>		50	mA	
STBY pin Input Current	STBY=V <sub>DD</sub>	I <sub>STBY</sub>		+500	μА	
STBY pin Input Current	STBY=V <sub>SS</sub>	ISTBY		-1	μА	

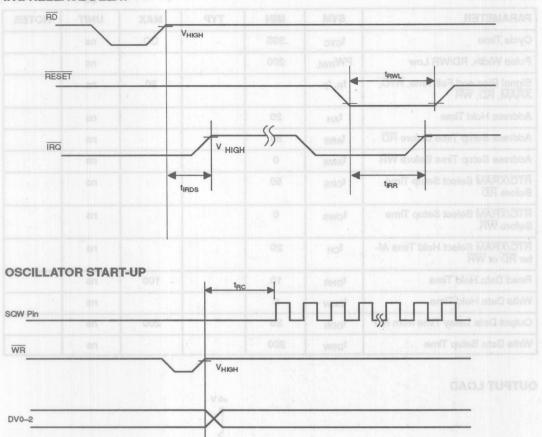
### **AC SWITCHING CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{DD} = 4.5\text{V to }5.5\text{V})$ 

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Reset Pulse Width		t <sub>RWL</sub>	5		μs	
Oscillator Startup	From Software Enable Via DV Bits	t <sub>RC</sub>		1	s	
IRQ Release from RD High		tIRDS		2	μѕ	
IRQ Release from RESET Low		t <sub>IRR</sub>		2	μѕ	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### IRQ RELEASE DELAY



NOTE

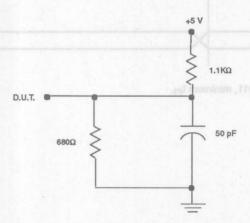
Timing assumes RS3-0 Bits = 0011, minimum tpl.

### **BUS TIMING**

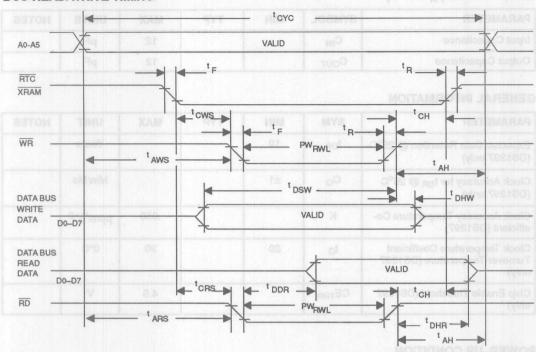
 $(0^{\circ} \text{ to } 70^{\circ}\text{C}, V_{DD} = 4.5\text{V to } 5.5\text{V})$ 

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Cycle Time	tcyc	395	MENNY	DC	ns	
Pulse Width, RD/WR Low	PWRWL	200			ns	
Signal Rise and Fall Time, RTC, XRAM, RD, WR	t <sub>R</sub> , t <sub>F</sub>			30	ns	
Address Hold Time	t <sub>AH</sub>	20			ns	
Address Setup Time Before RD	tARS	50			ns	DEI)
Address Setup Time Before WR	t <sub>AWS</sub>	0			ns	
RTC/XRAM Select Setup Time Before RD	t <sub>CRS</sub>	50	00%		ns	
RTC/XRAM Select Setup Time Before WR	tcws	0			ns	
RTC/XRAM Select Hold Time After RD or WR	t <sub>CH</sub>	20			ns	
Read Data Hold Time	t <sub>DHR</sub>	10	of Call	100	ns	Plumido
Write Data Hold Time	t <sub>DHW</sub>	0	139.71		ns	
Output Data Delay Time from RD	t <sub>DDR</sub>	20		200	ns	
Write Data Setup Time	t <sub>DSW</sub>	200			ns	700

### **OUTPUT LOAD**



#### **BUS READ/WRITE TIMING**



### POWER-DOWN/ POWER-UP TIMING (t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE High to Power Fail	t <sub>PF</sub>	a surf.		0	ns	
Recovery at Power Up	tREC		150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤V <sub>CC</sub> ≤ 4.5V	300	4.00x		μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤V <sub>CC</sub> ≤ 4.0V	10	光	50 <sup>1</sup>	μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC≥</sub> 4.0V	0			μs	
Expected Data Retention	t <sub>DR</sub>	10		- 3X	years	

### NOTE

 $\overline{\text{CE}}$  is chip enabled for access, an internal signal which is defined by  $(\overline{\text{RD}} + \overline{\text{WR}})$   $(\overline{\text{XRAM}} + \overline{\text{RTC}})$ .

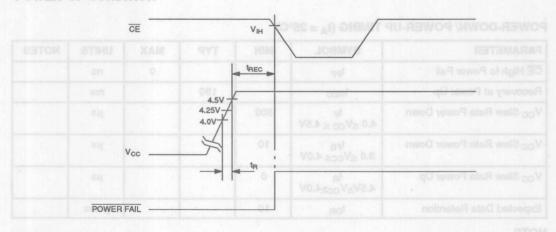
### CAPACITANCE (t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	GLIAV		12	pF	Ap-AS
Output Capacitance	C <sub>OUT</sub>	RE LLE	- 1	12	pF	

### **GENERAL INFORMATION**

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Expected Data Retention @ 25°C (DS1397 only)	t <sub>DR</sub>	10	1	- awa -	Years	- AM
Clock Accuracy for t <sub>DR</sub> @ 25°C (DS1397 only)	CQ	±1			Min/Mo	BUE ATAD
Clock Accuracy Temperature Co- efficient (DS1397)	K			.050	ppm/°C2	ATAG
Clock Temperature Coefficient Turnover Temperature (DS1397 only)	to	20		30	0°C	DATA BUS READ DATA
Chip Enable Threshold (DS1397 only)	CE <sub>THR</sub>	— яаа' —b	- SHO"	4.5	V	- 85

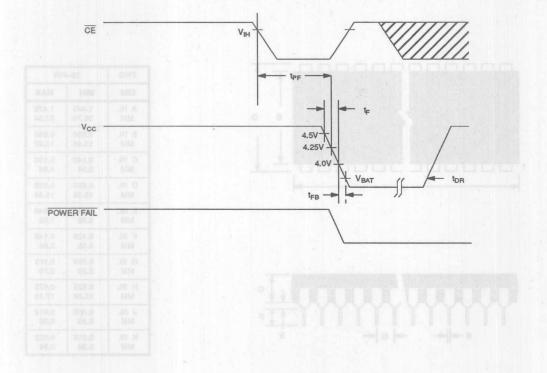
### POWER-UP CONDITION



#### NOTE

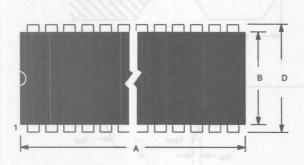
 $\overline{\text{CE}}$  is an internal signal generated by the power switching reference in the DS139X products.

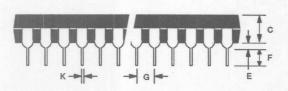
### POWER-DOWN CONDITION

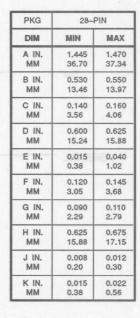


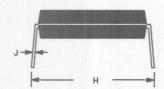
6

### **DS1395 28 PIN DIP**

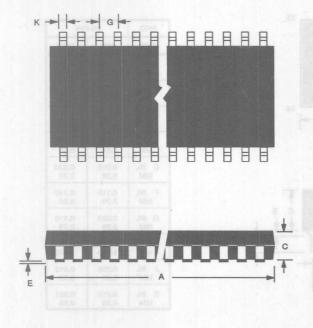




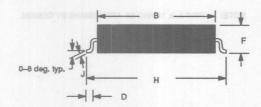




### **DS1395S 28 PIN SOIC**

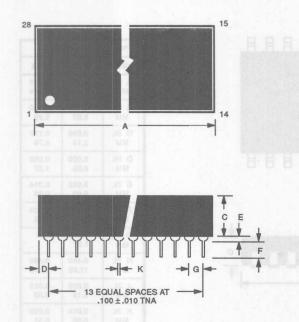


PKG	28-P	IN
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050
E IN. MM	0.002 0.05	0.014
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480
J IN. MM	0.006 0.15	0.013
K IN. MM	0.014 0.36	0.020

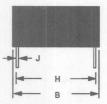


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### DS1397 28 PIN 720 MIL FLUSH ENCAPSULATED



PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.520 38.61	1.540 39.12
B IN. MM	0.695 17.65	0.720 18.29
C IN.	0.350 8.89	0.375 9.52
D IN.	0.100 2.54	0.130 3.30
E IN.	0.015 0.38	0.030 0.76
F IN.	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021 0.53



NOTE: PINS 3, 4, 18 AND 22 ARE MISSING BY DESIGN.

# DS1485/DS1488 RAMified Real Time Clock 8K x 8

#### **FEATURES**

- Upgraded IBM AT computer clock/calendar with 8K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- · Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- · Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 8K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
     8K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- Available as chip (DS1485) or stand alone module with embedded lithium battery and crystal (DS1488)

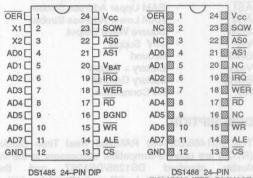
#### ORDERING INFORMATION

DS1485 DS1485S RTC Chip; 24 pin DIP RTC Chip; 28 pin SOIC

DS1488

RTC Module; 24 pin DIP

### PIN ASSIGNMENT



(600 MIL)

DS1488 24-PIN ENCAPSULATED PACKAGE (740 MIL FLUSH)



**DS1485S 28-PIN SOIC** 

### PIN DESCRIPTION

OER - RAM Output Enable X1 Crystal Input X2 - Crystal Output AD0-AD7 - Mux'ed Address/Data Bus CS - RTC Chip Select Input ALE RTC Address Strobe WR RTC Write Data Strobe RD - RTC Read Data Strobe WER - RAM Write Data Strobe IRQ - Interrupt Request Output AS1 RAM Upper Address Strobe AS0 RAM Lower Address Strobe SQW Square Wave Output - +5V Supply Vcc GND - Ground Battery + Supply VBAT BGND **Battery Ground** NC No Connection

#### DESCRIPTION

The DS1485/DS1488 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 and the DS1385/DS1387 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 8K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system  $V_{\rm CC}$  by a lithium battery.

The 8K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

### **OPERATION**

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1485/DS1488. The following paragraphs describe the function of each pin.

#### SIGNAL DESCRIPTIONS

GND,  $V_{CC}$  - DC power is provided to the device on these pins.  $V_{CC}$  is the +5 volt input. When 5 volts are applied

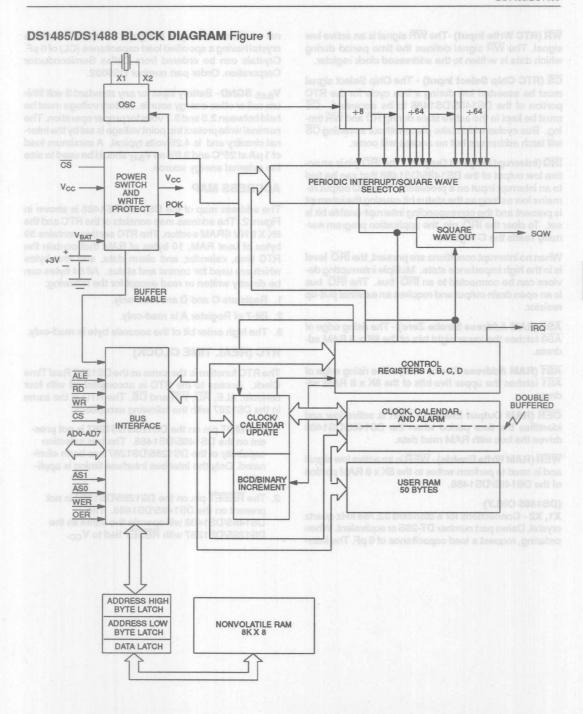
within normal limits, the device is fully accessible and data can be written and read. When  $V_{\rm CC}$  is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{\rm CC}$  falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the  $V_{\rm BAT}$  pin in the case of the DS1485, or to the internal battery in the case of the DS1488. The timekeeping function maintains an accuracy of  $\pm 1$  minute per month at 25°C regardless of the voltage input on the  $V_{\rm CC}$  pin.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when  $V_{CC}$  is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1485/DS1488 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, ASO, or AS1, at which time the DS1485/DS1488 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the WR or WER pulses. In a read cycle, the DS1485/DS1488 outputs 8 bits of data during the latter portion of the RD or OER pulses. The read cycle is terminated and the bus returns to a high impedance state as RD or OER transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1485/DS1488.

RD (RTC Read Input) - RD identifies the time period when the DS1485/DS1488 drives the bus with RTC read data. The RD signal is an enable signal for the output buffers of the clock.



WR (RTC Write Input) -The WR signal is an active low signal. The WR signal defines the time period during which data is written to the addressed clock register.

CS (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1485/DS1488 to be accessed. CS must be kept in the active state during RD and WR timing. Bus cycles which take place without asserting CS will latch addresses but no access will occur.

IRQ (Interrupt Request Output) - The IRQ pin is an active low output of the DS1485/DS1488 that can be tied to an interrupt input on a processor. The IRQ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ pin, the application program normally reads the C register.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  bus is an open drain output and requires an external pull-up resistor.

ASO (RAM Address Strobe Zero) - The rising edge of ASO latches the lower eight bits of the 8K x 8 RAM address.

AS1 (RAM Address Strobe One) - The rising edge of AS1 latches the upper five bits of the 8K x 8 RAM address.

OER (RAM Output Enable) - OER is active low and identifies the time period when the DS1485/DS1488 drives the bus with RAM read data.

WER (RAM Write Enable) - WER is an active low signal and is used to perform writes to the 8K x 8 RAM portion of the DS1485/DS1488.

#### (DS1485 ONLY)

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor Corporation. Order part number DS9032.

V<sub>BAT</sub>, BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V<sub>BAT</sub> should be used to size the external energy source.

### ADDRESS MAP

The address map of the DS1485/DS1488 is shown in Figure 2. The address map consists of the RTC and the 8K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

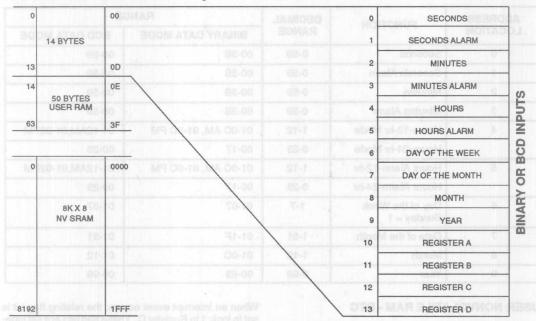
- 1. Registers C and D are read-only.
- 2. Bit-7 of Register A is read-only.
- 3. The high order bit of the seconds byte is read-only.

### RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, RD, WR and CS. The RTC is the same in the DS1287 with the following exceptions:

- The MOT pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
- The RESET pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The DS1485/DS1488 will operate the same as the DS1285/DS1287 with RESET tied to V<sub>CC</sub>.

### ADDRESS MAP DS1485/DS1488 Figure 2



#### TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected,

the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1 and 1 and

ADDRESS	FUNCTION	DECIMAL	RANGE		
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE	
0	Seconds	0-59	00-3B	00-59	
1	Seconds Alarm	0-59	00-3B	00-59	
2	Minutes	0-59	00-3B	00-59	
3	Minutes Alarm	0-59	00-3B	00-59	
4 14	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM	
	Hours-24-hr Mode	0-23	00-17	00-23	
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM	
	Hours Alarm-24-hr	0-23	00-17	00-23	
6	Day of the Week Sunday = 1	1-7	01-07	01-07 X XX	
7	Date of the Month	1-31	01-1F	01-31	
8	Month	1-12	01-0C	01-12	
9	Year	0-99	00-63	00-99	

#### **USER NONVOLATILE RAM - RTC**

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1485/DS1488. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

#### **INTERRUPTS**

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the  $\overline{\mbox{lRQ}}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{\mbox{lRQ}}$  is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{IRQ}$  pin is asserted low.  $\overline{IRQ}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{IRQ}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1485/DS1488. The act of reading Register C clears all active flag bits and the IRQF bit.

# 6

#### OSCILLATOR CONTROL BITS

When the DS1485/DS1488 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator of

#### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

#### PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

1	SELECT BITS	REGISTER	A wol a li	t <sub>Pl</sub> PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	rebridector	3.90625 ms	256 Hz
0	0	son a January	0	7.8125 ms	128 Hz
0	0	regord hi al els	yo etabgu wa	122.070 μs	8.192 kHz
0	HIS of the Eur	0	0	244.141 μs	4.096 kHz
0	bres short bill	0	1	488.281 μs	2.048 kHz
0	drio achienue	od at dech od	0	976.5625 μs	1.024 kHz
0	nco 1d b	lone paser	911 1 James	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1 /	0	15.625 ms	64 Hz
1	0	8 educH	matorra	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1 1	. 1	500 ms	2 Hz

### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{\text{IRQ}}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

#### **UPDATE CYCLE**

The DS1485/DS1488 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an

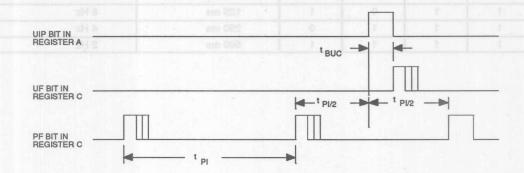
alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within  $(t_P/2+t_{BUC})$  to ensure that data is not read during the update cycle.

### **UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP** Figure 3



 $t_{\text{PI}}$  = Periodic interrupt time interval per Table 1.  $t_{\text{BUC}}$  = Delay time before update cycle = 244  $\,\mu \text{s}$ .

#### REGISTERS MAR been stab OTH and to attraction

The DS1485/DS1488 has four control registers which are accessible at all times, even during the update cycle.

#### REGISTER A

MSE	3						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BITO
UIP	DV2	DV1	DVO	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- 1. Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit:
- 3. Enable both at the same time and the same rate; or
- 4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

#### REGISTER B and believe a stud ord no blink

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in

the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1485/DS1488.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{IRQ}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{IRQ}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{IRQ}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1485/DS1488 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The internal functions of the DS1485/DS1488 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert IRQ. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

#### REGISTER C

	MSB								
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
į	IRQF	PF	AF	UF	0	0	0	0	

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1 UF = UIE = 1

i.e., IRQF = (PF . PIE) + (AF . ALE) + (UF . UIE)

Any time the IRQF bit is a one, the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the  $\overline{\mbox{IRQ}}$  signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

#### **REGISTER D**

MSE	d airi						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the

contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0** - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

#### 8K X 8 RAM

The DS1485/DS1488 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM is supported.

Four control signals,  $\overline{AS0}$ ,  $\overline{AS1}$ ,  $\overline{OER}$ , and  $\overline{WER}$ , are used to access the 8K x 8 SRAM. This access mode is identical to that supported by the DS1385/DS1387. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ( $\overline{AS0}$ ) and Address Strobe 1 ( $\overline{AS1}$ ) signals.  $\overline{AS0}$  is used to latch the lower 8-bits of address, and  $\overline{AS1}$  is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM (WER) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM (OER) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The WER and OER signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via CS) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either WER or OER is active. CS is only used for the access of the clock calendar registers and the 50 bytes of user RAM.

### ABSOLUTE MAXIMUM RATINGS\* OTA OT ELICYO ETTAW ACT AMMIT 2UE ABAREGIZBATEG

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature

Soldering Temperature

-0.3V to +7.0V 0°C to 70°C -40°C to +70°C 260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	٧	1
Input Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	٧	1
Input Logic 0	V <sub>IL</sub>	-0.3		+0.8	// V//	1
Battery Voltage	V <sub>BAT</sub>	2.5		3.7	//V//	9

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I <sub>CC1</sub>		35	50	mA	2
Standby Current $\overline{CS}$ , $\overline{OER}$ , and $\overline{WER} = V_{CC}$ -0.3V	I <sub>CC2</sub>		1	5.0	mA	6
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μА	3
I/O Leakage	ILO	-1.0	AHH HO	+1.0	μА	3
Output @ 2.4V	I <sub>OH</sub>	-1.0		- tel	mA	1,4
Output @ 0.4V	loL		10/- 100	4.0	mA	1

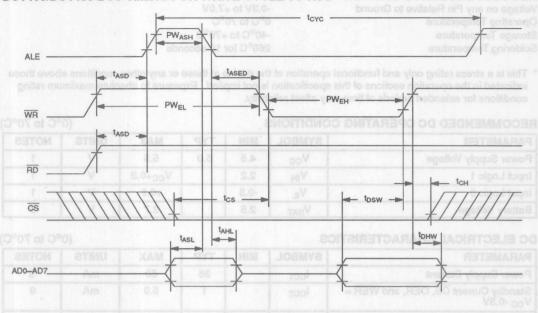
#### RTC AC TIMING CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 4.5\text{V to }5.5\text{V})$ 

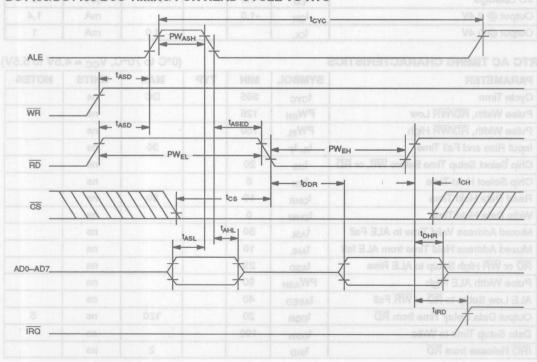
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	tcyc	305		DC	ns	
Pulse Width, RD/WR Low	PWEH	125			ns	RW
Pulse Width, RD/WR High	PW <sub>EL</sub>	150		(a- 4)	ns	
Input Rise and Fall Time	t <sub>R</sub> , t <sub>F</sub>	术		30	ns	
Chip Select Setup Time Before WR, or RD	tcs	20			ns	— āā
Chip Select Hold Time	tcH	0			ns	
Read Data Hold Time	tDHR	10		80	ns	1
Write Data Hold Time	t <sub>DHW</sub>	0		*1111	ns	
Muxed Address Valid Time to ALE Fall	tASL	30			ns	
Muxed Address Hold Time from ALE fall	tAHL	10	48	0-	ns	
RD or WR High Setup to ALE Rise	tASD	25	Halle	1	ns	TOA-GOA
Pulse Width ALE High	PWASH	60		21	ns	
ALE Low Setup to RD or WR Fall	tASED	40			ns	
Output Data Delay Time from RD	t <sub>DDR</sub>	20		120	ns	5
Data Setup Time to Write	t <sub>DSW</sub>	100			ns	DRI -
IRQ Release from RD	t <sub>IRD</sub>			2	μs	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DS1485/DS1488 BUS TIMING FOR WRITE CYCLE TO RTC \*\*EDMITAR MUMDIAM ETGLICERA



### DS1485/DS1488 BUS TIMING FOR READ CYCLE TO RTC

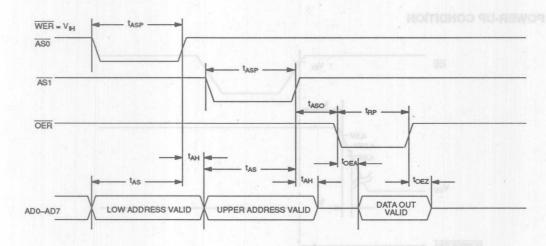


### **8K X 8 AC TIMING CHARACTERISTICS**

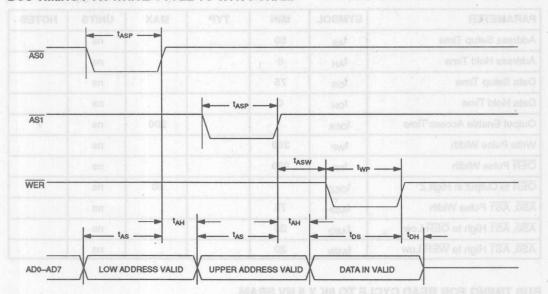
 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} + 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t <sub>AS</sub>	50			ns	
Address Hold Time	t <sub>AH</sub>	0			ns	964
Data Setup Time	t <sub>DS</sub>	75			ns	
Data Hold Time	t <sub>DH</sub>	0	esayes		ns	
Output Enable Access Time	tOEA			200	ns	7
Write Pulse Width	t <sub>WP</sub>	200			ns	
OER Pulse Width	t <sub>RP</sub>	200			ns	
OER to Output in High Z	toez			50	ns	R3W
AS0, AS1 Pulse Width	t <sub>ASP</sub>	75			ns	
AS0, AS1 High to OER Low	t <sub>ASO</sub>	20		I I	ns	
AS0, AS1 High to WER Low	t <sub>ASW</sub>	20			ns	

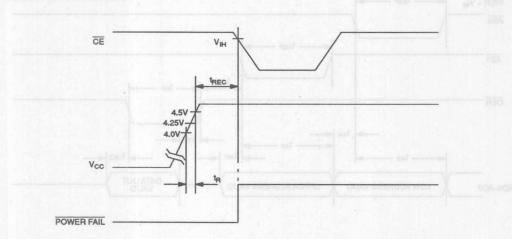
### **BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM**



### **BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM**

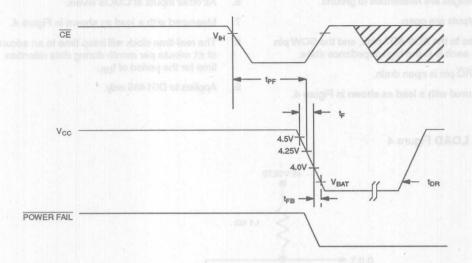


### **POWER-UP CONDITION**



# 6

### **POWER-DOWN CONDITION**



### **POWER-UP POWER-DOWN TIMING**

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE High to Power Fail	tpF		1000	0	ns	
Recovery at Power Up	tREC		150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤V <sub>CC</sub> ≤ 4.5V	300			μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤V <sub>CC</sub> ≤ 4.0V	10			μs	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC</sub> ≥4.0V	0			μѕ	
Expected Data Retention	t <sub>DR</sub>	10			years	8

### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

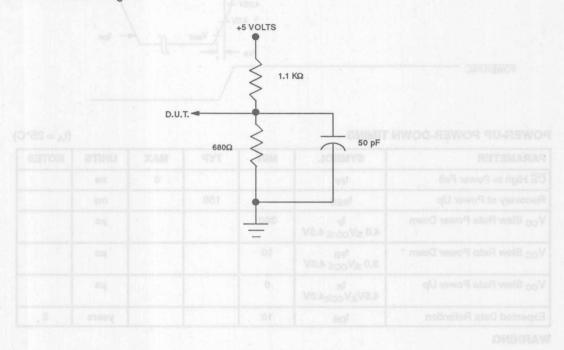
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	1		12	pF	
Output Capacitance	C <sub>OUT</sub>			12	pF	

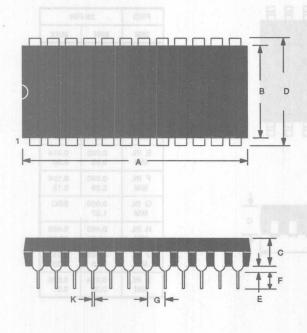
#### NOTES

- 1. All voltages are referenced to ground.
- 2. All outputs are open.
- Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
- 4. The IRQ pin is open drain.
- 5. Measured with a load as shown in Figure 4.

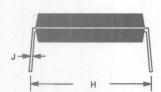
- 6. All other inputs at CMOS levels.
- 7. Measured with a load as shown in Figure 4.
- The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t<sub>DB</sub>.
- Applies to DS1485 only.

### **OUTPUT LOAD Figure 4**

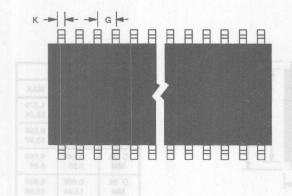




PKG	24-P	IN	
DIM	MIN	MAX	
A IN. MM	1.245 31.62	1.270 32.26	
B IN. MM	0.530 13.46	0.550 13.97	
O IN.	0.140 3.56	0.160 4.06	
D IN. MM	0.600 15.24	0.625 15.88	
E IN. MM	0.015 0.38	0.050	
F IN. MM	0.120 3.05	0.145 3.68	
G IN. MM	0.090 2.29	0.110	
H IN. MM	0.625 15.88	0.675 17.15	
J IN. MM	0.008 0.20	0.012	
K IN. MM	0.015 0.38	0.022	



### **DS1485S 28 PIN SOIC**



A IN.	0.706 17.93	0.728 18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN. MM	0.050 1.27	BSC
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

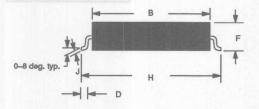
28-PIN

MAX

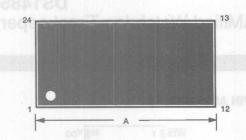
PKG

DIM

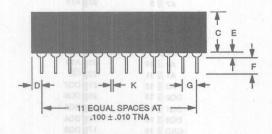


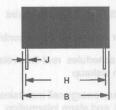


### **DS1488 24 PIN 740 MIL FLUSH ENCAPSULATED**









NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

PKG	24-1	PIN
DIM	MIN	MAX
A IN.	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN.	0.015 0.38	0.030
F IN.	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021

sircultry. Dinta confained within 128K by 3-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The time-coaping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMiffed memory space by intelligent control dirouting which detects he status of Voc. and write protects memory when Voc.

6

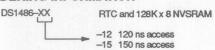


# DS1486 RAMified Watchdog Timekeeper

#### **FEATURES**

- 128K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 32-pin JEDEC footprint
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V<sub>CC</sub> @ 25%
- Interrupt signals active in power-down mode

### **ORDERING INFORMATION**



### DESCRIPTION

The DS1486 RAMified Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1486 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 128K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMiffied Timekeeper by intelligent control circuitry which detects the status of V<sub>CC</sub> and write protects memory when V<sub>CC</sub> is out of tolerance. The lithium energy source can main-

#### PIN ASSIGNMENT

INTB	≅ 1	32	Vcc
A16	2	31	A15
A14		308	INTA/SQV
A12		29	WE
	5	28	A13
	6	27	A8
	7	26	A9
	8		A11
	9	100	OE
	3 10		A10
11 11 2 32	11		CE
	12		DQ7
	13	208	DQ6
	14	198	DQ5
	3 15	188	DQ4
	₫ 16	178	DQ3

DS1486 128K x 8 32-Pin Encapsulated Package

### PIN DESCRIPTION

INTB(INTB)	- Int	errupt Output B
A0-A16	- Ad	dress Inputs
DQ0-DQ7	- Da	ta Input/Output
CE	- Ch	ip Enable
ŌĒ	- Ou	tput Enable
WE	- Wr	ite Enable
Vcc	- +5	Volts
GND	- Gr	ound
<b>INTA/SQW</b>	- Int	errupt Output A/Squar
	Wa	ave Output

tain data and real time for over ten years in the absence of  $V_{CC}.$  Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/ PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

#### **OPERATION - READ REGISTERS**

The DS1486 executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (High) and  $\overline{CE}$  (Chip Enable) and  $\overline{OE}$  (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A16) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the latter occurring signal  $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

### **OPERATION - WRITE REGISTERS**

The DS1486 is in the write mode whenever the WE (Write Enable) and CE (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery state (twn) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (tDS) and Data Hold Time (tDH) with respect to the earlier rising edge of CE or WE. The OE control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active), then WE will disable the outputs in topw from its falling edge.

#### **DATA RETENTION**

The RAMiffied Timekeeper provides full functional capability when  $V_{CC}$  is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is

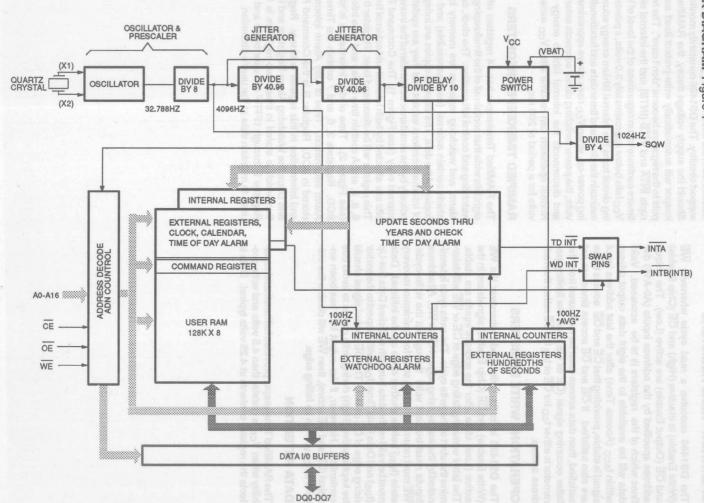
maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1486 constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAMified Time-keeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts  $\overline{\text{INTA}}$  and  $\overline{\text{INTB}}$  (INTB) and the internal clock and timers continue to run regardless of the level of  $V_{CC}$ . As  $V_{CC}$  falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  and disconnects the internal lithium energy source. Normal operation can resume after  $V_{CC}$  exceeds 4.5 volts for a period of 200 ms.

### **RAMIFIED TIMEKEEPER REGISTERS**

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register E through 1FFFF are user bytes and can be used to maintain data at the user's discretion.

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uata in DOD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, EOSC (Bit 7) enables the real time clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the INTA/Square Wave Output (pin 30). When set to logic zero, the INTA/Square Wave Output pin will output a 1024 Hz square wave signal. When set to logic one the Square Wave Output pin is available for interrupt A output (INTA) only. Bit 6 of the Hours register is defined as the 12 or 24 hour select bit. When set to logic one, the 12 hour format is selected. In the 12 hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24 hour mode, bit 5 is the second 10 hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce er-

roneous results for the same reasons. A way of making

from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RA-Mified Timekeeper.

### TIME OF DAY ALARM REGISTERS

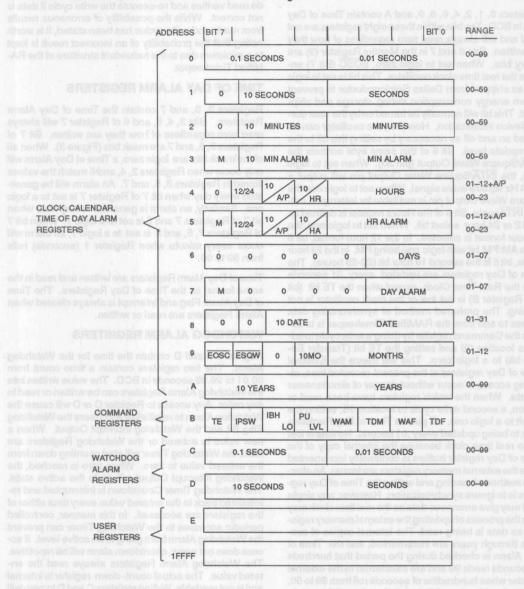
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7, 5, and 3 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

#### **WATCHDOG ALARM REGISTERS**

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count-down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

### **DS1486 RAMIFIED TIMEKEEPER REGISTERS** Figure 2



### TIME OF DAY ALARM MASK BITS Figure 3

REGISTER		non miles	EMPERATURE
(3) MINUTES	(5) HOURS	(7) DAYS	SHOTAGIST TO STANKE
1	1	1	ALARM ONCE PER MINUTE
to shoolide	at mess of an	e ore device n is n <b>t</b> t impli	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0 84	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

#### **COMMAND REGISTER**

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW-Bit 6 Interrupt switch - When set to a logic 1, INTA is the Time of Day Alarm and INTB/(INTB) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. INTA is now the Watchdog Alarm output and INTB/(INTB) is the Time of Day Alarm output. The INTA/SQW output pin shares both the interrupt A and square wave output function. When INTA is active, the square wave function is automatically disabled.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and  $V_{\rm CC}$  is applied, INTB/(INTB) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, INTA and INTB/(INTB) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and INTA will sink current for a minimum of 3 ms and then release. INTB/(INTB) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF-Bit 0 Time of Day Flag-This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

6

ABSOLUTE MAXIMUM RATINGS\*

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO +7.0V 0°C TO 70°C -40°C TO + 70°C 260°C FOR 10 SECONDS

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	٧	10
Input Logic 1	V <sub>IH</sub>	2.2	whw notelinal	V <sub>CC</sub> + 0.3	V	10
Input Logic 0	goodstall en V <sub>IL</sub> sign	-0.3	e, The ope	+0.8	ns al <b>V</b> loste	10

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	ett ,0 qpol s d	-1.0	nust be set t	+1.0	μА	be affecte
Output Leakage Current	a lo	-1.0	OI halosto e	+1.0	μА	inan un
I/O Leakage Current	ILIO	-1.0	B) is the Wat	+1.0	μΑ	lo amiT ed
Output Current @ 2.4V	Іон	-1.0	paru zaznavi arm output a	A pobriotaW	mA	Dri enig
Output Current @ 0.4V	loL	igol er	f dugluo n	4.0	mA	13
Standby Current CE = 2.2V	I <sub>CCS1</sub>	ort or	3.0	7.0	mA	avew ener
Standby Current CE = V <sub>CC</sub> -0.5	I <sub>CCS2</sub>	ters	-Monabell	4.0	mA	SARAK GARA
Active Current	Icc	odW (8	TATE (SATER )	85	mA	tes ettid
Write Protection Voltage	V <sub>TP</sub>	amid me	4.25	enancionario	V	to estude

### CAPACITANCE COMIT & restor holgolar of hea side

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	all Alar	7	15	pF	(BITVII) I
Output Capacitance	C <sub>OUT</sub>	dW e	selet <b>7</b> erlî b	s an 15 ho n	pF	Inemen a
Input/Output Capacitance	C <sub>VO</sub>	now br	em 7o mu	15	pF	po edi no i

### **AC ELECTRICAL CHARACTERISTICS**

(0°C to +70°C,  $V_{CC} = 5.0V \pm 10\%$ )

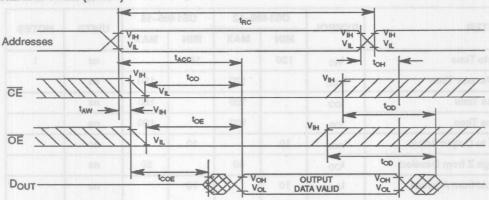
PARAMETER		DS1486-12		DS1486-15			
	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120	[eg	150		ns	1
Address Access Time	tACC		120	Op!	150	ns	77
CE Access Time	tco		120		150	ns	
OE Access Time	t <sub>OE</sub>		100	101	120	ns	
OE or CE to Output Active	tcoe	10		10	AT K	ns	44 3
Output High Z from Deselect	top		40		50	ns	
Output Hold from Address Change	tон	10	14. P&S	10		ns	700
Write Cycle Time	twc	120		150	88 2, 6,	ns	TO BUT
Write Pulse Width	t <sub>WP</sub>	110		140		ns	3
Address Setup Time	t <sub>AW</sub>	0		0	# V	ns	3000010
Write Recovery Time	t <sub>WR</sub>	10		15	Day MA	ns	
Output High Z from WE	topw		40	KA	50	ns	CZ 30
Output Active from WE	toew	10		10		ns	PHILIP
Data Setup Time	t <sub>DS</sub>	85	10/1	110	100	ns	4
Data Hold Time	t <sub>DH</sub>	10		15	pl .	ns	4,5
INTA, INTB Pulse Width	t <sub>IPW</sub>	3	100	3	6	ms	11,12

### **AC TEST CONDITIONS**

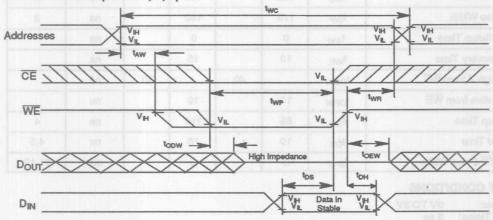
OV TO 3V

Input Levels: 0V Transition Times: 5 ns

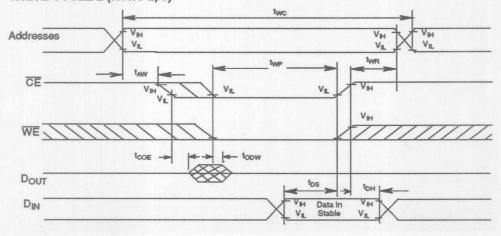
## READ CYCLE (Note1)



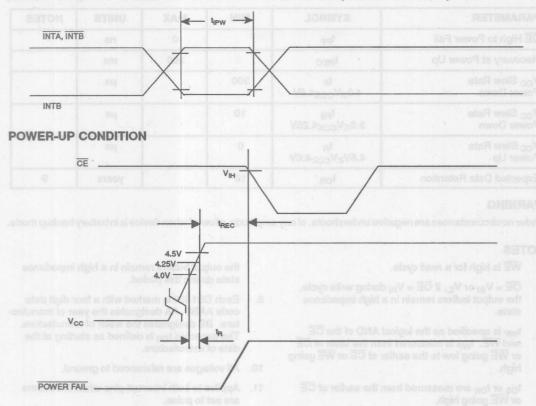
### WRITE CYCLE 1 (Notes 2, 6, 7)



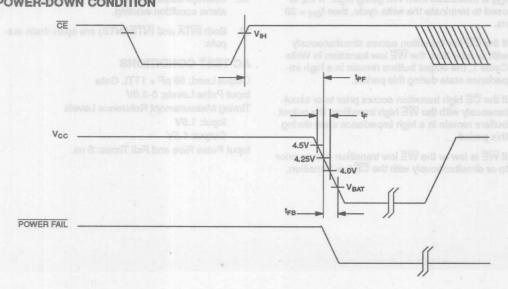
### WRITE CYCLE 2 (Notes 2, 8)



### TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



### POWER-DOWN CONDITION



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#### AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
CE High to Power Fail	tpF		0	ns	W.ADM
Recovery at Power Up	tREC	A	200	ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0≤V <sub>CC</sub> ≤4.5V	300	4	μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0≤V <sub>CC≤</sub> 4.25V	10		μѕ	057H
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC</sub> ≥4.0V	0		μѕ	
Expected Data Retention	t <sub>DR</sub>	10		years	9

#### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

- WE is high for a read cycle.
- OE = VIH or VIL. If OE = VIH during write cycle, the output buffers remain in a high impedance
- twp is specified as the logical AND of the CE and WE. twp is measured from the latter of CE or WE going low to the earlier of CE or WE going
- t<sub>DS</sub> or t<sub>DH</sub> are measured from the earlier of CE or WE going high.
- t<sub>DH</sub> is measured from WE going high. If CE is used to terminate the write cycle, then tDH = 20
- 6. If the CE low transition occurs simultaneously with or later than the WE low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition,

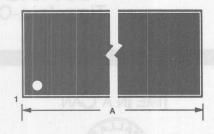
- the output buffers remain in a high impedance state during this period.
- Each DS1486 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected ton is defined as starting at the date of manufacture.
- 10. All voltages are referenced to ground.
- 11. Applies to both interrupt pins when the alarms are set to pulse.
- 12. Interrupt output occurs within 100 ns on the alarm condition existing.
- 13. Both INTA and INTB(INTB) are open drain outputs.

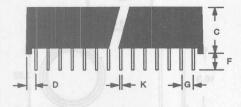
#### **AC TEST CONDITIONS**

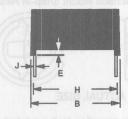
Output Load: 50 pF + 1TTL Gate Input Pulse Levels: 0-3.0V Timing Measurement Reference Levels Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5 ns.

### **DS1486 32 PIN 740 MIL MODULE**







PKG	32-F	PIN
DIM	MIN	MAX
A IN. MM	1.720 43.69	1.740 44.20
B IN. MM	0.720 18.29	0.740 18.80
C IN.	0.395 10.03	0.415 10.54
D IN.	0.090 2.29	0.120 3.05
E IN. MM	0.017 0.43	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090	0.110 2.79
H IN. MM	0.590 14.99	0.630
J IN. MM	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021

6

# **DALLAS**SEMICONDUCTOR

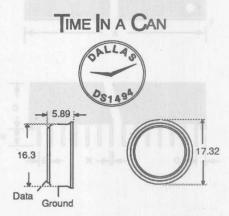
DS1494L-F5 Time-In-a-Can

### **FEATURES**

- Miniature timekeeping system sealed in a 16mm MicroCan
- Snaps into a surface-mounted printed circuit board retainer
- Self-powered with greater than 10 years of lithium
- Keeps precise time in 1/256 second increments
- Quartz accuracy to ± 2 minutes per month
- Interval timer measures duration of an activity
- Number of power on/off cycles detected and stored in cycle counter
- Programmable alarms generate interrupts for real time, interval timer and/or cycle count
- 4096 bits of nonvolatile SRAM organized in 16 pages of 256 bits
- Data integrity assured by verifying data in a scratchpad before transferring to memory
- 1-wire interface shares only one I/O pin for 16K bits per second communication
- Unique 48-bit, factory-lasered serial number for identification and traceability
- Tamper-proof lock bits prevent alteration of timers and cycle counter
- Operating temperature range -20 to 70°C
- Applications include computer real-time clock, run time meter, sequence timer, event recorder, warranty information, maintenance records, configuration, and calibration data

### DESCRIPTION

The DS1494L-F5 Time-In-a-Can (TIC) supplies accurate time-of-day information, measures run time, schedules activities, and records vital data. Its one and only signal communicates through the lid of a sealed Micro-Can. Dallas Semiconductor's development of this minimal signalling technique for integrated circuits, called 1-wire, made it possible to seal a silicon chip, quartz, and a lithium energy source in an inexpensive stainless steel enclosure, not significantly larger than the battery would have been by itself. Furthermore, the solo data



DS9098 Surface Mount Snap-In Retainer



signal simplifies mounting to the printed circuit board and lowers the cost of electrical interface. TIC is a full-feature timekeeping system including a unique, lasered serial number, real-time clock, run-time meter, cycle counter, programmable interrupts, 256-bit scratchpad, and 4096 bits of nonvolatile SRAM.

The unalterable serial number is registered for absolute traceability. TIC surface mounts to a printed circuit board by a snap-in retainer (DS9098) or thru-hole mount (DS9094F). Using a contact probe, data can be read or written even when the printed circuit board is without power. All data is nonvolatile for greater than 10 years.

The DS1494L-F5 shares electrical and mechanical specifications with the DS1994L-F5 Touch Memory Plus Time which is used in Automatic Identification applications (see DS1994 data sheet in Section 12, "Automatic Identification").

## DS1495/DS1497 **RAMified Real Time Clock**

### **FEATURES**

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 kHz
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- · Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 register/RAM locations plus 8K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general and control registers
     Separate 8K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
- Periodic rates from 122 µs to 500 ms
- End-of-clock update cycle
- 28-pin JEDEC footprint
- Available as chip (DS1495/DS1495S) or stand alone module with embedded lithium battery and crystal

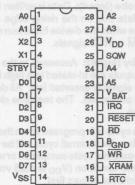
### ORDERING INFORMATION

DS1495 RTC Chip; 28 pin DIP DS1495S RTC Chip; 28 pin SOIC DS1497 RTC Module; 28 pin DIP

### **PIN ASSIGNMENT**

AO	1	V	28	III A2
A1 CIL	2		27	III A3
Х2Ш	3		26	DO VDD
X1 🗆	4			D SQW
STBY	5		24	III A4
Doc	6		23	DD A5
D1 CC	7		22	D VBAT
D2	8		21	IRQ
D3 🗆	9		20	TO RESET
D4CIC	10		19	III RD
D5 CIC	11		18	BGND
D6CCC	12			WR WR
D7 🗆	13		16	XRAM
VSS	14		15	RTC

DS1495S 28-Pin SOIC (330 mil)



DS1495 28-Pin DIP (600 mil)

AO	3 1	do senia la	28	A2
A1	3 2	l Belooles	27 🛭	A3
NC	3	in nertwa	26 🛭	VDD
NC	8 4	a AW o		SQW
STBY	8 5		24 🛭	
D0	3 6	to extremely		A5
D1	8 7	or turn! Interest	22	NC
D2	3 8	and treated we	21 🛭	IRQ
D3	3		20 🛭	RESET
D4	8 1	0	19 🛭	RD
D5	2 1	1) tooled	18 🛭	NC
D6	1 1	2	17 🛭	WR
D7	3 1	3		XRAM
VSS	3 1	4	15	RTC

DS1497 28-Pin Encapsulated Package (720 mil)

### **PIN DESCRIPTIONS**

V<sub>DD</sub>, V<sub>SS</sub> – Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 – Data Bus (bidirectional): Data is written into the device from the data bus if either  $\overline{XRAM}$  or  $\overline{RTC}$  is asserted during a write cycle at the rising edge of a  $\overline{WR}$  pulse. Data is read from the device and driven onto the data bus if either  $\overline{XRAM}$  or  $\overline{RTC}$  is asserted during a read cycle when the  $\overline{RD}$  signal is low.

A0-A5 – Address Bus (Input): Various internal registers of the device are selected by these lines. When RTC is asserted, A0 selects between the indirect address register and RTC data register. When the XRAM is asserted, A0-A5 addresses a 32-byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

RD – Read Strobe (Input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either RTC or XRAM is asserted.

WR – Write Strobe (input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the XRAM or RTC signals.

STBY – Standby (Input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the  $\overline{\text{STBY}}$  signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition ( $V_{DD}$  is 4.25 volts, typical) is negated, whichever occurs first.

RTC – Real Time Clock Select (Input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when RD is low. Data is received from the bus when WR is pulsed low and then high.

SQW – Square Wave (output): Frequency selectable output. Frequency is selected by setting register A bits RSO-RS3. See Table 2 for frequencies that can be selected.

XRAM – Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are acces-

sible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM pointed to by the page register. Data is driven onto the data bus when  $\overline{\text{RD}}$  is low. Data is received from the bus when  $\overline{\text{WR}}$  is pulsed low and then high.

IRQ – Interrupt Request (output): The IRQ signal is an active low, open drain output that is used as a processor interrupt request. The IRQ output follows the state of the IRQF bit (bit 7) in status register C. IRQ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

RESET – Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When RESET is low, the following occurs

- 1. The following register bits are cleared:
  - a. Periodic interrupt (PIE)
  - b. Alarm interrupt enable (AIE)
  - c. Update ended interrupt (UF)
  - d. Interrupt request flag (IRQF)
  - e. Periodic interrupt flag (PF)
  - f. Alarm interrupt flag (AF)
  - g. Square wave output enable (SQWE)
  - h. Update ended interrupt enable (UIE)
- 2. The IRQ pin is in the high impedance state.
- 3. The RTC is not processor accessible.

### **ADDITIONAL PIN DESCRIPTION**

### (FOR DS1495, DS1495S)

X1, X2 – Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C<sub>L</sub>) of 6pF.

 $V_{BAT}-$  Battery input for any standard +3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry at 4.25 volts typical. A maximum load of 1  $\mu A$  at 25°C and 3.0V on  $V_{BAT}$  in the absence of power should be used to size the external energy source.

 ${\bf B_{GND}}$  – Battery ground: This pin or pin 14 can be used for the battery ground return.

# 6

### **OPERATION**

Power-Down/Power-Up: The real time clock will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V<sub>DD</sub>. When the voltage level applied to the V<sub>DD</sub> input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When  $V_{DD}$  falls below the CE<sub>THR</sub> (4.25 volts typical), the chip select inputs  $\overline{\text{RTC}}$  and  $\overline{\text{XRAM}}$  are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When  $V_{DD}$  falls below 3.2 volts (typical), the module is switched over to an internal power source in the case of the DS1497, or to an external battery connected to the  $V_{BAT}$  and BGND pins in the case of the DS1495 and DS1495S, so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when RTC is asserted low and represents the real time clock. The second set of registers is active when RAM is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

- Registers C and D are Read Only (status information)
- 2. Bit 7 of register A is Read Only
- 3. Bit 7 of the "Seconds" byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 256 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 256 pages of nonvolatile memory available. The address of

the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/O spaces. (See Figure 3.)

### TIME, CALENDAR AND ALARM LOCATIONS

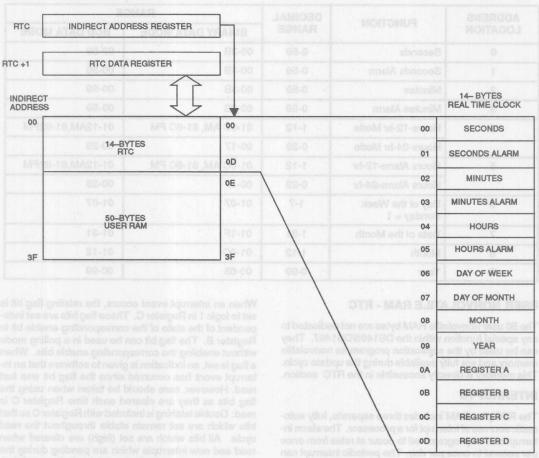
The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

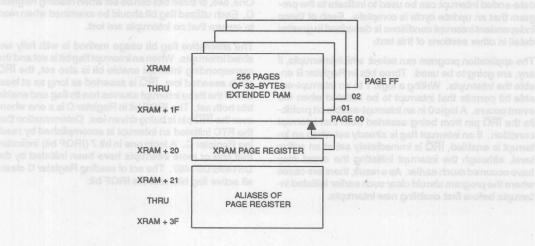
Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

### REAL TIME CLOCK RAM MAP Figure 2 | edst 2300M ATAG MEAJA GHA RAGMEJAO 3881



### EXTENDED RAM ADDRESS MAP Figure 3



020692 5/18

TIME, CALENDAR AND ALARM DATA MODES Table 1 Security SAME MARE MODES TABLE 1

ADDRESS	FUNCTION	DECIMAL	RANG	GE
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

### **USER NONVOLATILE RAM - RTC**

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1495/DS1497. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

### INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the  $\overline{\mbox{lRQ}}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{\mbox{lRQ}}$  is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the  $\overline{IRQ}$  pin is asserted low.  $\overline{IRQ}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the  $\overline{IRQ}$  pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1495/DS1497. The act of reading Register C clears all active flag bits and the IRQF bit.

### **OSCILLATOR CONTROL BITS**

When the DS1495/DS1497 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

### SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator.

Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{\text{IRQ}}$  pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

### PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

S	ELECT BITS	REGISTER	A	t <sub>PI</sub> PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	t <sub>Pl</sub> PERIODIC INTERRUPT RATE  None 3.90625 ms 7.8125 ms 122.070 μs 244.141 μs 488.281 μs 976.5625 μs 1.953125 ms	FREQUENCY
0	0	0	0	None	None
0	0	0	man 1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1_1	11	122.070 µs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz
0	1	1	0	976.5625 μs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

### **UPDATE CYCLE**

The DS1495/DS1497 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

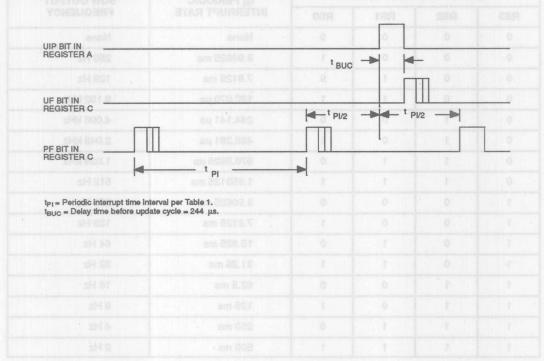
There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date in-

formation. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than  $t_{BUC}$  allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within  $(t_{P}/2+t_{BUC})$  to ensure that data is not read during the update cycle.

### UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



### REGISTERS

The DS1495/DS1497 has four control registers which are accessible at all times, even during the update cycle.

### **REGISTER A**

	MSB BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

- 1. Enable the interrupt with the PIE bit;
- 2. Enable the SQW output pin with the SQWE bit;
- 3. Enable both at the same time and the same rate; or
- 4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

### REGISTER B

MSE	MSB							
				BIT 3				
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in

a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1495/DS1497.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{IRQ}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{IRQ}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{IRQ}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1495/DS1497 functions but is cleared by the hardware  $\overline{RESET}$  signal.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The internal functions of the DS1495/DS1497 do not affect the AIE bit but is cleared by RESET.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert IRQ. The SET bit going high or the RESET pin going low clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit and is cleared by RESET.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/ write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

### REGISTER C

MSE	3						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF – The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 AF = AIE = 1 UF = UIE = 1 i.e., IRQF = (PF ● PIE) + (AF ● AIE) + (UF ● UIE)

Any time the IRQF bit is a one, the  $\overline{IRQ}$  pin is driven low. All flag bits are cleared after Register C is read by the program or when the  $\overline{RESET}$  pin is low.

PF – The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the IRQ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C or by RESET.

AF – A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one

will appear in the IRQF bit. A read of Register C or a RE-SET will clear AF.

**UF**—The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ pin. UF is cleared by reading Register C or by RESET.

BIT 0 THROUGH BIT 3 — These are reserved bits of the status Register C. These bits always read zero and cannot be written.

### REGISTER D

MSE	3						LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0**—The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

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### **ABSOLUTE MAXIMUM RATINGS\***

V<sub>DD</sub> Pin Potential to Ground Pin Input Voltage Power Dissipation Storage Temperature Ambient Temperature Soldering Temperature -0.3V to +7.0V V<sub>SS</sub> - 0.3 to V<sub>DD</sub> + 0.3V 500 mW -40°C to +70°C 0°C to +70°C 260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage	aps <sup>1</sup>	Vcc	4.5	5.5	٧	
Input High Voltage	Recognized as a High Signal Over Recommended V <sub>DD</sub> and t <sub>A</sub> Range	V <sub>IH</sub>	2.2	V <sub>DD</sub> + 0.3	V	
Input Low Voltage	Recognized as a Low Signal Over Recommended V <sub>DD</sub> and t <sub>A</sub> Range	V <sub>IL</sub>	-0.3	0.8	V	
Battery Voltage		V <sub>BAT</sub>	2.5	3.7	V	LLHOR

### DC ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 5.0V \pm 10\%, V_{SS} = 0V, t_A = 0^{\circ} C \text{ to } 70^{\circ}C)$ 

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Input Leakage V <sub>IL</sub> =0V, V <sub>IH</sub> =V <sub>DD</sub>	For any Single Pin: D0-7, RD, WR, A0-5, XRAM, RTC, RESET	lı		±1	μА	西南
Output High Voltage	V <sub>DD</sub> =5.0V I <sub>LOAD</sub> =1 mA	VoH	2.4		٧	
Output Low Voltage	V <sub>DD</sub> = 5.0V I <sub>LOAD</sub> = 4 mA	V <sub>OL</sub>		0.4	٧	
Power Supply Current	Outputs Unloaded	I <sub>DD</sub>		50	mA	S-6VI
STBY pin Input Current	STBY=V <sub>DD</sub>	ISTBY		+500	μА	
STBY pin Input Current	STBY=V <sub>SS</sub>	ISTBY		-1	μА	

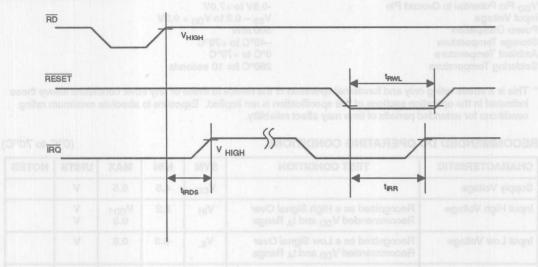
### **AC SWITCHING CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{DD} = 4.5\text{V to }5.5\text{V})$ 

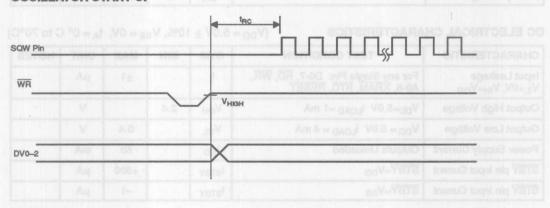
CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Reset Pulse Width		t <sub>RWL</sub>	5		μѕ	
Oscillator Startup	From Software Enable Via DV Bits	t <sub>RC</sub>		1	s	
IRQ Release from RD High		t <sub>IRDS</sub>		2	μs	
IRQ Release from RESET Low		t <sub>IRR</sub>		2	μѕ	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### IRQ RELEASE DELAY



### **OSCILLATOR START-UP**



### NOTE

Timing assumes RS3-0 Bits = 0011, minimum tpl.

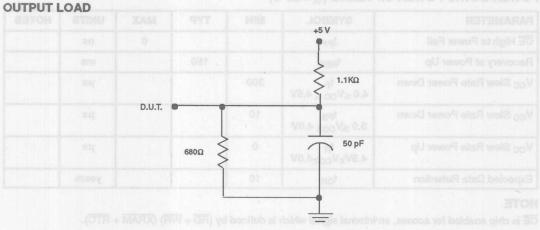


### **BUS TIMING**

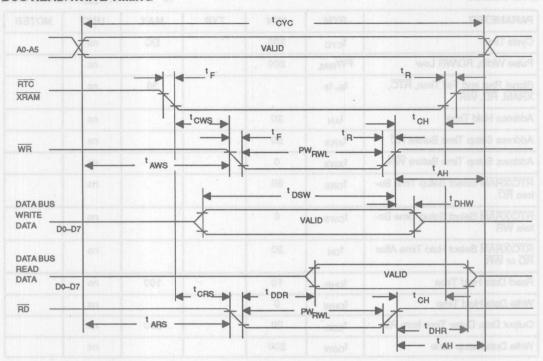
 $(0^{\circ} \text{ to } 70^{\circ}\text{C}, V_{DD} = 4.5\text{V to } 5.5\text{V})$ 

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Cycle Time	tcyc	395		DC	ns	24-04
Pulse Width, RD/WR Low	PWRWL	200			ns	
Signal Rise and Fall Time, RTC, XRAM, RD, WR	t <sub>R</sub> , t <sub>F</sub>			30	ns	OTR MARK
Address Hold Time	t <sub>AH</sub>	20	lug8wo1	Saul I	ns	
Address Setup Time Before RD	tARS	50	4		ns	200
Address Setup Time Before WR	t <sub>AWS</sub>	0	Ve-	- care	ns	
RTC/XRAM Select Setup Time Before RD	tcrs	50			ns	BUBATAN
RTC/XRAM Select Setup Time Before WR	tcws	0	1		ns	STIRW ATAG
RTC/XRAM Select Hold Time After RD or WR	t <sub>CH</sub>	20			ns	SUG ATAG
Read Data Hold Time	tDHR	10		100	ns	G ATAG
Write Data Hold Time	t <sub>DHW</sub>	0			ns	_ 88
Output Data Delay Time from RD	t <sub>DDR</sub>	20	14	200	ns	
Write Data Setup Time	t <sub>DSW</sub>	200			ns	





### **BUS READ/WRITE TIMING**



## POWER-DOWN/ POWER-UP TIMING (t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE High to Power Fail	tpF			0	ns	
Recovery at Power Up	tREC		150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤V <sub>CC</sub> ≤ 4.5V	300			μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤V <sub>CC</sub> ≤ 4.0V	10		- HAUAG	μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V≥V <sub>CC≥</sub> 4.0V	0	\$ 5550		μѕ	
Expected Data Retention	t <sub>DR</sub>	10			years	

### NOTE

 $\overline{\text{CE}}$  is chip enabled for access, an internal signal which is defined by  $(\overline{\text{RD}} + \overline{\text{WR}})$   $(\overline{\text{XRAM}} + \overline{\text{RTC}})$ .

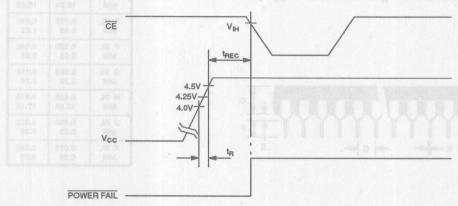
## CAPACITANCE (t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			12	pF	
Output Capacitance	C <sub>OUT</sub>			12	pF	

### **GENERAL INFORMATION**

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Expected Data Retention @ 25°C (DS1497 only)	t <sub>DR</sub>	10			Years	
Clock Accuracy for t <sub>DR</sub> @ 25°C (DS1497 only)	CQ	±1	non	aoo	Min/Mo	
Clock Accuracy Temperature Coefficient (DS1497)	К			.050	ppm/°C2	
Clock Temperature Coefficient Turnover Temperature (DS1497 only)	t <sub>O</sub>	20		30	0°C	
Chip Enable Threshold (DS1497 only)	CETHR			4.5	V	

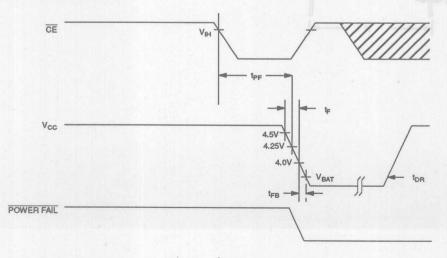
### **POWER-UP CONDITION**



### NOTE

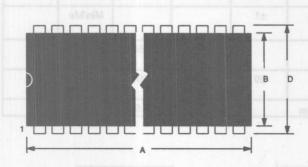
CE is an internal signal generated by the power switching reference in the DS149X products.

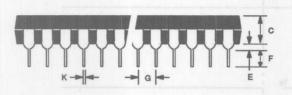
### **POWER-DOWN CONDITION**



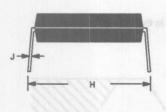
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### **DS1495 28 PIN DIP**

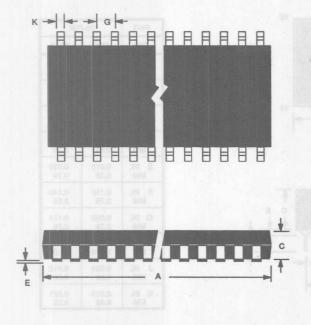




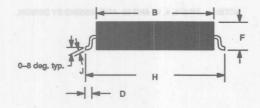
PKG	28-	PIN
DIM	MIN	MAX
A IN.	1.445 36.70	1.470 37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625 15.88	0.675 17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56



### **DS1495S 28 PIN SOIC**

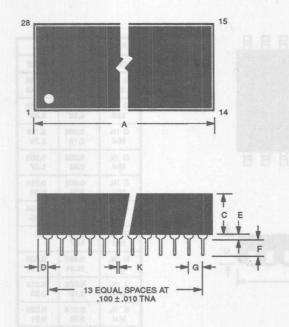


PKG	28-PIN			
DIM	MIN	MAX		
A IN. MM	0.706 17.93	0.728 18.49		
B IN. MM	0.338 8.58	0.350 8.89		
C IN. MM	0.086 2.18	0.110 2.79		
D IN. MM	0.020 0.58	0.050		
E IN. MM	0.002 0.05	0.014		
F IN. MM	0.090 2.29	0.124 3.15		
G IN. MM	0.050	BSC		
H IN. MM	0.460 11.68	0.480		
J IN. MM	0.006 0.15	0.013		
K IN. MM	0.014 0.36	0.020		

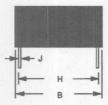


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### **DS1497 28 PIN 720 MIL FLUSH ENCAPSULATED**



PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.520 38.61	1.540 39.12
B IN. MM	0.695 17.65	0.720 18.29
C IN.	0.350 8.89	0.375 9.52
D IN.	0.100 2.54	0.130 3.30
E IN.	0.015 0.38	0.030 0.76
F IN.	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008 0.20	0.012 0.30
K IN.	0.015 0.38	0.021 0.53



NOTE: PINS 3, 4, 18 AND 22 ARE MISSING BY DESIGN.



## DS1585/DS1587 Serialized Real Time Clocks

### **FEATURES**

Incorporates industry standard DS1287 PC clock plus enhanced features:

- 64-bit Silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 114 bytes user NVRAM
- 8K bytes additional NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 kHz output for power management

Supports Intel timing mode

Compatible with existing BIOS for original DS1287 functions

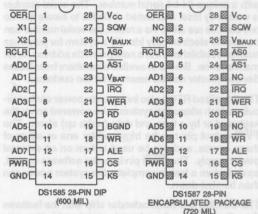
Available as chip (DS1585) or stand-alone module (DS1587) with embedded lithium battery and crystal

### PIN DESCRIPTION

OER RAM output enable X1 Crystal input Crystal output RCLR RAM clear input AD0-AD7 Mux'ed address/data bus PWR Power on interrupt output KS Kickstart input CS RTC Chip select input ALE RTC address strobe WR RTC write data strobe RD RTC read data strobe WER RAM write data strobe IRQ Interrupt request output AS1 RAM upper address strobe AS0 RAM lower address strobe SQW Square wave output

+5V supply Vcc GND Ground VBAT Battery + supply VBAUX Auxiliary battery supply BGND Battery ground

### **PIN ASSIGNMENT**



(720 MIL)



### ORDERING INFORMATION

DS1585	RTC Chip; 28 pin DIP
DS1585S	RTC Chip; 28 pin SOIC
DS1587	RTC Module; 28 pin DIP

### DESCRIPTION

The DS1585 and DS1587 are RAMified real time clocks (RTC's) designed as upward-compatible successors to the industry standard DS1287, DS1387, DS1487, and DS1488 PC real time clocks. As such, these devices incorporate a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, and 8K bytes of additional NVSRAM.

Each DS1585/DS1587 is individually manufactured with a unique 64-bit serial number. The serial number is written by laser and tested at Dallas to insure that no two devices are alike. As a result, the serial number can be used to electronically identify a system for purposes such as establishment of a network node address, or for maintenance. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The Serialized RTC's also incorporate power control circuitry which allows the system to be powered on via the keyboard or by a time and date (wake up) alarm. The PWR output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The PWR pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1585 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1587 incorporates the DS1585 chip, a 32.768 kHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas such that a minimum of 10 years of timekeeping and data retention in the absence of V<sub>CC</sub> is guaranteed.

### **OPERATION**

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1585/DS1587. The following paragraphs describe the function of each pin.

### SIGNAL DESCRIPTIONS

GND,  $V_{CC}$  - DC power is provided to the device on these pins.  $V_{CC}$  is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When  $V_{CC}$  is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below 3 volts typical, the RAM and timekeeper are switched over to lithium battery connected either to the  $V_{BAT}$  pin or  $V_{BAUX}$  pin in

the case of the DS1585, or to the internal lithium battery in the case of the DS1587. The timekeeping function maintains an accuracy of  $\pm 1$  minute per month at 25°C regardless of the voltage input on the  $V_{CC}$  pin.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32 kHz SQW signal is output when SQWE=1 and the Enable 32 kHz (E32K) in extended register 04BH and V<sub>CC</sub> is above 4.25V. A 32 kHz square wave is also available when V<sub>CC</sub> is less than 4.25 volts typical if E32K=1, ABE=1, and voltage applied to V<sub>BAUX</sub>.

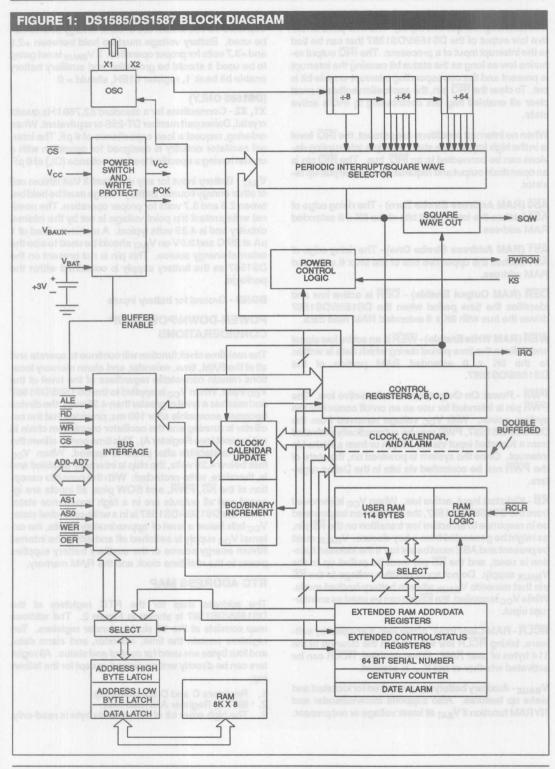
AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1585/DS1587 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, ASO, or AS1, at which time the DS1585/DS1587 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the WR or WER pulses. In a read cycle the DS1585/DS1587 outputs 8 bits of data during the latter portion of the RD or OER pulses. The read cycle is terminated and the bus returns to a high impedance state as RD or OER transitions high.

ALE (RTC Address Strobe Input) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1585/DS1587.

RD (RTC Read Input) - RD identifies the time period when the DS1585/DS1587 drives the bus with RTC read data. The RD signal is an enable signal for the output buffers of the clock.

WR (RTC Write Input) -The WR signal is an active low signal. The WR signal defines the time period during which data is written to the addressed clock register.

CS (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1585/DS1587 to be accessed. CS must be kept in the active state during RD and WR timing. Bus cycles which take place with ALE asserted but without asserting CS will latch addresses. However, no data transfer will occur.



 $\overline{\textbf{IRQ}}$  (Interrupt Request Output) - The  $\overline{\textbf{IRQ}}$  pin is an active low output of the DS1585/DS1587 that can be tied to the interrupt input of a processor. The  $\overline{\textbf{IRQ}}$  output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the  $\overline{\textbf{IRQ}}$  pin, the application software must clear all enabled flag bits contributing to IRQ's active state.

When no interrupt conditions are present, the  $\overline{IRQ}$  level is in the high impedance state. Multiple interrupting devices can be connected to an  $\overline{IRQ}$  bus. The  $\overline{IRQ}$  pin is an open drain output and requires an external pull-up resistor.

ASO (RAM Address Strobe Zero) - The rising edge of ASO latches the lower eight bits of the 8K x 8 extended RAM address.

AS1 (RAM Address Strobe One) - The rising edge of AS1 latches the upper five bits of the 8K x 8 extended RAM address.

OER (RAM Output Enable) - OER is active low and identifies the time period when the DS1585/DS1587 drives the bus with 8K x 8 extended RAM read data.

WER (RAM Write Enable) - WER is an active low signal and defines the time period during which data is written to the 8K x 8 extended RAM portion of the DS1585/DS1587.

PWR - Power On Output; open drain; active low. The PWR pin is intended for use as an on/off control for the system power. With V<sub>CC</sub> voltage removed from the DS1585/DS1587, PWR may be automatically activated from a Kickstart input via the KS pin or from a Wake Up interrupt. Once the system is powered on, the state of the PWR can be controlled via bits in the Dallas registers.

 $\overline{\text{KS}}$  - Kickstart input, active low. When  $V_{CC}$  is removed from the DS1585/DS1587, the system can be powered on in response to an active low transition on the  $\overline{\text{KS}}$  pin, as might be generated from a key closure.  $V_{BAUX}$  must be present and ABE must be set to 1 if the kickstart function is used, and the  $\overline{\text{KS}}$  pin must be pulled up to the  $V_{BAUX}$  supply. Do not apply positive voltage to the  $\overline{\text{KS}}$  pin that exceeds  $V_{BAUX}$  while in battery-backed mode. While  $V_{CC}$  is applied, the  $\overline{\text{KS}}$  pin can be used as an interrupt input.

RCLR - RAM Clear Input; active low. If enabled by software, taking RCLR low will result in the clearing of the 114 bytes of user RAM. When enabled, RCLR can be activated whether or not V<sub>CC</sub> is present.

V<sub>BAUX</sub> - Auxiliary battery input required for kickstart and wake up features. Also supports clock/calendar and NVRAM function if V<sub>BAT</sub> at lower voltage or not present.

Standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V<sub>BAUX</sub> is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 01BH, should = 0.

### (DS1585 ONLY)

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF.

 $V_{BAT}$  - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1  $\mu A$  at 25°C and 3.0V on  $V_{BAT}$  should be used to size the external energy source. This pin is not present on the DS1587 as the battery supply is contained within the package.

**BGND** - Ground for battery inputs

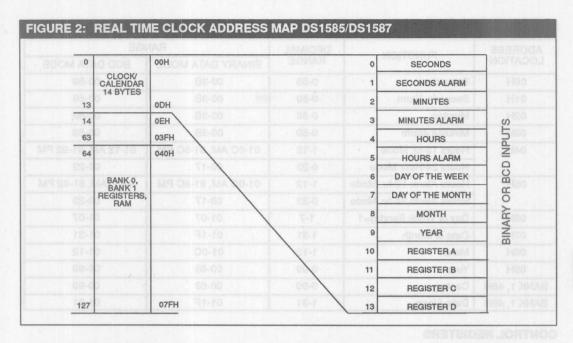
# POWER-DOWN/POWER-UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V<sub>CC</sub> input. When V<sub>CC</sub> is applied to the DS1585/DS1587 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When Vcc falls below 4.25 volts, the chip is internally disabled and is, therefore, write-protected. With the possible exception of the KS, PWR, and SQW pins, all inputs are ignored and all outputs are in a high impedance state. When the DS1585/DS1587 is in a write-protected state, V<sub>CC</sub> falls below a level of 'approximately 3 volts, the external V<sub>CC</sub> supply is switched off and either the internal lithium energy source or the auxiliary battery supplies power to the real-time clock and the RAM memory.

### RTC ADDRESS MAP

The address map for the RTC registers of the DS1585/DS1587 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

- 1. Registers C and D are read-only.
- 2. Bit-7 of Register A is read-only.
- 3. The high order bit of the seconds byte is read-only.



### TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when

it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

ADDRESS	FUNCTION	DECIMAL	RANGE		
LOCATION	FUNCTION	RANGE	BINARY DATA MODE	BCD DATA MODE	
00H	Seconds	0-59	00-3B	00-59	
01H	Seconds Alarm	0-59	00-3B	00-59	
02H	Minutes	0-59	00-3B	00-59	
03H	Minutes Alarm	0-59	00-3B	00-59	
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM	
	Hours 24-Hour Mode	0-23	00-17	00-23	
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM	
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23	
06H	Day of Week Sunday=1	1-7	01-07	01-07	
07H	Date of Month	1-31	01-1F	01-31	
08H	Month	1-12	01-0C	01-12	
09H	Year	0-99	00-63	00-99	
BANK 1, 48H	Century	0-99	00-63	00-99	
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31	

### **CONTROL REGISTERS**

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

### **NONVOLATILE RAM - RTC**

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1585/DS1587. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

#### INTERRUPT CONTROL

The DS1585/DS1587 includes six separate, fully automatic sources of interrupt for a processor:

- 1. Alarm interrupt
- 2. Periodic interrupt
- Update-ended interrupt
- 4. Wake up interrupt
- Kickstart interrupt
- 6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended regis-

ter locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the  $\overline{IRQ}$  pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled,  $\overline{IRQ}$  will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

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The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the  $\overline{IRQ}$  line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set.  $\overline{IRQ}$  will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the  $\overline{IRQ}$  pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1585/DS1587 initiated an interrupt is accomplished by reading Register C and finding IRQF =1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

### SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 kHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled (SQWE = 1), then the output frequency will be determined by the settings of the E32K bit in Extended Register B and by the RS3-0 bits in Register A. If the E32K = 1, then a 32.768 kHz square wave will be output on the SQW pin regardless of the settings of RS3-0.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 kHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If SQWE1, E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to  $V_{\rm BAUX}$  then the 32 kHz square wave output signal will be output on the SQW pin in the absence of  $V_{\rm CC}$ . This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of  $V_{\rm CC}$ .

### **OSCILLATOR CONTROL BITS**

When the DS1587 timekeeping module with crystal and lithium battery is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the count-down chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

### PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the  $\overline{\text{IRQ}}$  pin to go to an active state from once every 500 ms to once every 122  $\mu s$ . This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

### **UPDATE CYCLE**

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

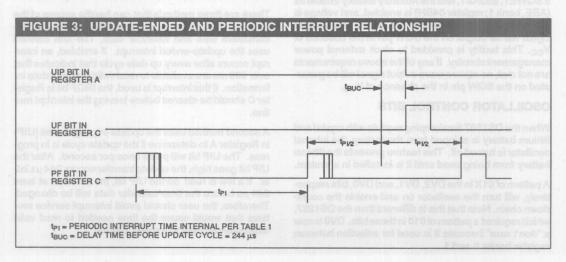
A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

XT. REG. B	SE	LECT BITS	REGISTE	RA	t <sub>PI</sub> PERIODIC	SQW OUTPUT	
E32K	RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY	
0	0	0	0	0	None	None	
0	0	o lingiquali	0	9011	3.90625 ms	256 Hz	
0	0	0	Stand did	0	7.8125 ms	128 Hz	
0	0	0	o soften	1 0	122.070 µs	8.192 kHz	
0	0	daig 1st mis	0	0	244.141 μs	4.096 kHz	
0	0	1	0	1	488.281 μs	2.048 kHz	
0	0	do as 1 uven	tott Juglus	0	976.5625 μs	1.024 kHz	
0	0	1	1	1	1.953125 ms	512 Hz	
0	The perio	0	0	0	3.90625 ms	256 Hz	
0	1	0	0	1 1	7.8125 ms	128 Hz	
0	1	0	.molfonst	0	15.625 ms	64 Hz	
0	1	0	PYO ETA	QU1 h	31.25 ms	32 Hz	
0	abolina a	200 to 01	0	0	62.5 ms	16 Hz	
0	8 of 1d Ta	as offine a	0	1 0	125 ms	8 Hz	
0	us "Ibneli	1 200	and Labor	0	250 ms	4 Hz	
old regiments. Ho	X	X	X	X		32.768 Hz	

<sup>\*</sup>RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t<sub>BUC</sub> allow valid time and date informa-

tion to be reached at each occurrence of the periodic interrupt. The reads should be complete within ( $t_{Pl}$  /  $2+t_{BUC}$ ) to ensure that data is not read during the update cycle.



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### REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DVO	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 - These bits are defined as follows:

DV2 = Countdown Chain

1 - resets countdown chain only if DV1=1

0 - countdown chain enabled

DV1 = Oscillator Enable

0 - oscillator off

1 - oscillator on

DV0 = Bank Select

0 - original bank

1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE bit;

Enable both at the same time and the same rate; or

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

#### REGISTER B

Enable neither.

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per

second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1585/DS1587.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the  $\overline{\mbox{IRQ}}$  pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the  $\overline{\mbox{IRQ}}$  pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the  $\overline{\mbox{IRQ}}$  output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1585/DS1587 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The internal functions of the DS1585/DS1587 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert IRQ. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/ write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

### REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1	WF=	WIE=	1
AF = AIE = 1	KF =	KSE=	1
HE-HE-1	RF =	RIF -	1

Any time the IRQF bit is a one, the IRQ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the IRQ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the  $\overline{\mbox{IRQ}}$  pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

#### **REGISTER D**

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the internal battery (the battery connected to the  $V_{BAT}$  pin in the case of the DS1585) or the battery connected to  $V_{BAUX}$ , whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

**BIT 6 THROUGH BIT 0** - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

### **EXTENDED FUNCTIONS**

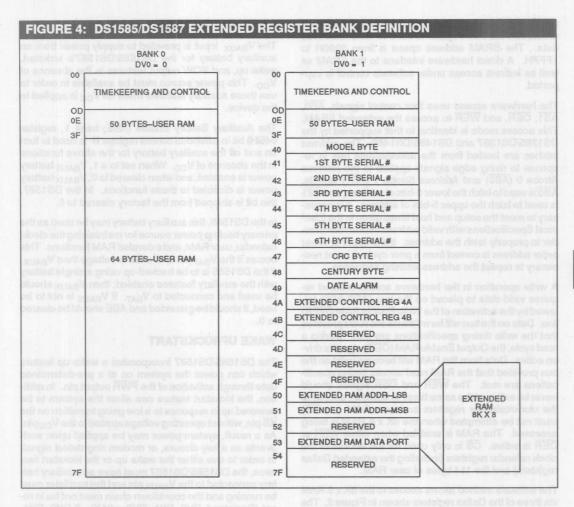
The extended functions provided by the DS1585/DS1587 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1585/DS1587 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

- 1. Silicon Revision byte
- 2. Serial Number
- 3. Century counter
- 4. 8 Kbyte Extended RAM access
- 5. Auxiliary Battery Control/Status
- 6. Wake Up
- 7. Kickstart
- 8. RAM Clear Control/Status

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.





### SILICON SERIAL NUMBER

A unique 64-bit lasered serial number is located in bank 1 registers 40H - 47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1585/DS1587. Registers 41H-46H contain a unique binary number. Registers 47H contains a CRC byte used to validate the data in registers 40H-46H. All 8 bytes of the serial number are read only registers.

The DS1585/DS1587 is manufactured such that no two devices will contain an identical number in locations 41H-48H. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1585/DS1587's with reserved blocks of serial numbers.

### **CENTURY COUNTER**

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

### 8KX8RAM

The DS1585/DS1587 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM as well as indirect access under software control is supported.

The hardware access uses four control signals, AS0, AS1, OER, and WER to access the extended SRAM. This access mode is identical to that supported by the DS1385/DS1387 and DS1485/DS1488. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 (AS0) and Address Strobe 1 (AS1) signals. AS0 is used to latch the lower 8-bits of address, and AS1 is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation in the hardware access method requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM (WER) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM (OER) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The WER and OER signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via CS) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either WER or OER is active. CS is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 114 bytes of user RAM.

The software method allows access to the 8K x 8 RAM via three of the Dallas registers shown in Figure 2. The Dallas registers in bank 1 must first be selected by setting the DV0 to 1 in Register A. The 13-bit address of the RAM location to be accessed must first be loaded into the two RAM address registers located at 50H and 51H. The least significant address byte should be written to location 50H, and the most significant 5 bits (rightjustified) should be loaded in location 51H. Data in the addressed location may be read by performing a read operation from location 53H, or written by performing a write operation to location 53H. Data in any addressed location may be read or written repeatedly without changing the address in locations 50H, 51H.

With the software method, the extended RAM may be accessed using only the control signals assigned to the clock/calendar and 114 byte user RAM; namely, ALE, CS, WR, and RD. As a result, the RAM control signals (AS1, AS0, WER, and OER) do not have to be used and should be tied to their inactive levels.

### **AUXILIARY BATTERY**

The  $V_{BAUX}$  input is provided to supply power from an auxiliary battery for the DS1585/DS1587's kickstart, wake up, and SQW output features in the absence of  $V_{CC}$ . This power source must be available in order to use these auxiliary features when no  $V_{CC}$  is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of  $V_{CC}$ . When set to a 1,  $V_{BAUX}$  battery power is enabled, and when cleared to 0,  $V_{BAUX}$  battery power is disabled to these functions. In the DS1587, this bit is shipped from the factory cleared to 0.

In the DS1585, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended RAM functions. This occurs if the  $V_{BAT}$  pin is at a lower voltage than  $V_{BAUX}$ . If the DS1585 is to be backed-up using a single battery with the auxiliary features enabled, then  $V_{BAUX}$  should be used and connected to  $V_{BAT}$ . If  $V_{BAUX}$  is not to be used, it should be grounded and ABE should be cleared to 0

### WAKE UP/KICKSTART

The DS1585/DS1587 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the PWR output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the KS pin, without operating voltage applied to the V<sub>CC</sub> pin. As a result, system power may be applied upon such events as a key closure, or modern ring detect signal. In order to use either the wake up or the kickstart features, the DS1585/DS1587 must have an auxiliary battery connected to the VBAUX pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the PWR pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V<sub>CC</sub> voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and se-

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conds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the PWR pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V<sub>CC</sub> voltage to the DS1585/DS1587 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the  $\overline{\text{KS}}$  input pin will be monitored for a low going transition of minimum pulse width  $t_{\text{KSPW}}$ . When such a transition is detected, the  $\overline{\text{PWR}}$  line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the  $\overline{PWR}$  pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1585/DS1587  $V_{CC}$  pin rises above the  $V_{BAT}$  level before the power on timeout period (tpoTo) expires, then  $\overline{PWR}$  will remain at the active low level. If  $V_{CC}$  does not rise above  $V_{BAT}$  voltage in this time, then the  $\overline{PWR}$  output pin will be turned off and will return to its high impedance level. In this event, the  $\overline{IRQ}$  pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If  $V_{CC}$  is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2,  $\overline{PWR}$  will remain active and  $\overline{IRQ}$  will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram  $\overline{KS}$  is assumed to be pulled up to the  $V_{BAUX}$  supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The  $\overline{PWR}$  line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the

DS1585/DS1587 is pending, the IRQ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, and minutes match condition. KF will be set in response to a low going transition on KS. If the associated interrupt enable bit is set (WIE and/or KSE) then the IRQ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1585/DS1587 may cause IRQ to be driven low. While system power is applied, the on chip logic will always attempt to drive the PWR pin active in response to the enabled kickstart or wake up condition. This is true even if PWR was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain  $\overline{PWR}$  pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As  $V_{CC}$  voltage decays, the  $\overline{IRQ}$  output pin will be placed in a high impedance state when  $V_{CC}$  goes below  $V_{PE}$ . If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect,  $\overline{PWR}$  and  $\overline{IRQ}$  are tri-stated, and monitoring of wake up and kickstart takes place.

### RAM CLEAR

The DS1585/DS1587 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V<sub>CC</sub> pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the RCLR pin. This action will have no effect on either the clock/calendar settings or upon the contents of the 8K x 8 Extended RAM. The RAM clear Flag (RF, bank 1, register 04BH) will be set when the RAM clear operation has been completed. If V<sub>CC</sub> is present at the time of the RAM clear and RIE=1, the IRQ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The IRQ line will then return to its inactive high level provided there are no other pending interrupts. Once the RCLR pin is activated, all read/write accesses are locked out for a minimum recover time, specified as tREC in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the RCLR pin will have no effect on the contents of the user RAM, and transitions on the RCLR pin have no effect on RF.

### **EXTENDED REGISTERS**

Two extended control registers are provided supply controls and status information for the extended features offered by the DS1585/DS1587. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows:

### EXTENDED CONTROL REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V<sub>BAUX</sub>. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment is in progress to the time/date registers and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB - Power Active Bar control bit. When this bit is 0, the PWR pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE=1 OR KFAND KSE=1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the RCLR input (pin 4) if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

### **EXTENDED CONTROL REGISTER B**

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	18 <b>*</b> SH	RCE	*	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V<sub>BAUX</sub> pin (pin 26) for extended functions. On the DS1587 with an embedded lithium cell, this bit is shipped from the factory set to a logic 0.

E32K - Enable 32,768 output. This bit when written to a logic 1 will enable the 32,768 Hz oscillator frequency to be output on the SQW pin (pin 27) provided SQWE=1.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on pin 4 (RCLR) to clear all 114 bytes of user RAM. When RCE = 0, pin 4 and the RAM clear function are disabled.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the IRQ pin will be driven low when a RAM clear function is completed.

WIE- Wake Up Alarm Interrupt Enable. When  $V_{CC}$  voltage is absent and WIE is set to a 1, the  $\overline{PWR}$  pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When  $V_{CC}$  is then applied, the  $\overline{IRQ}$  pin will also be driven low. If WIE is set while system power is applied, both  $\overline{IRQ}$  and  $\overline{PWR}$  will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the  $\overline{PWR}$  or  $\overline{IRQ}$  pins.

KSE - Kickstart Interrupt Enable. When  $V_{CC}$  voltage is absent and KSE is set to a 1, the  $\overline{PWR}$  pin will be driven active low when a kickstart condition occurs ( $\overline{KS}$  pulsed low), causing the KF bit to be set to 1. When  $V_{CC}$  is then applied, the  $\overline{IRQ}$  pin will also be driven low. If KSE is set to 1 while system power is applied, both  $\overline{IRQ}$  and  $\overline{PWR}$  will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the  $\overline{PWR}$  or  $\overline{IRQ}$  pins.

\* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND
OPERATING TEMPERATURE

-0.3V TO +7.0V
0°C TO 70°C
-40°C TO +70°C

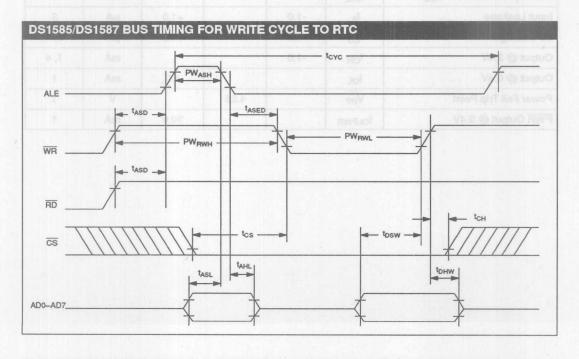
SOLDERING TEMPERATURE 260°C FOR 10 SECONDS

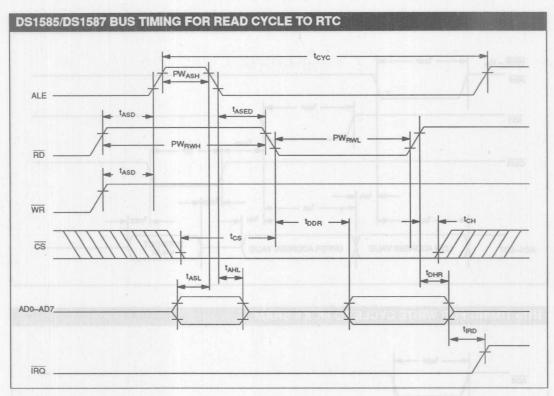
\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPE	RATING COND	ITIONS (	°C TO 70°C	C)		TO BOT
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	1000
Input Logic 1	V <sub>IH</sub>	2.2	TRUM	V <sub>CC</sub> +0.3	V	1
Input Logic 0	VIL	-0.3	JHA <sup>‡</sup>	+0.8	V	BBA Hex
Battery Voltage	V <sub>BAT</sub>	2.5		3.7	V	10
Auxiliary Battery Voltage	V <sub>BAUX</sub>	2.5	H-	3.7	V	10

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I <sub>CC1</sub>	201	35	50	mA	2
Standby Current CS = V <sub>CC</sub> -0.3V	I <sub>CC2</sub>		1	5.0	mA	6
Input Leakage	IIL	-1.0		+1.0	μА	3
I/O Leakage	ILO	-1.0		+1.0	μА	3, 4
Output @ 2.4V	Іон	-1.0			mA	1, 4
Output @ 0.4V	l <sub>OL</sub>		1/4	4.0	mA	1
Power Fail Trip Point	V <sub>PF</sub>		4.25		V	1
PWR Output @ 0.4V	lolpwr			10.0	mA	1

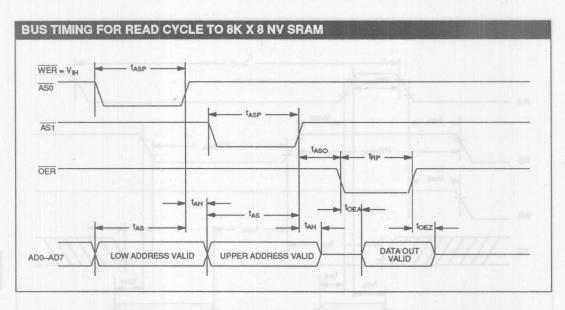
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	tcyc	305		DC	ns	T BEARC
Pulse Width, RD/WR Low	PWowL	125		BAU	ns	DMIEBOT
Pulse Width, RD/WR High	PWRWH	150			ns	
Input Rise and Fall Time	t <sub>R</sub> , t <sub>F</sub>	ton al neita	officiona sidt	30	ns	ni beteoi
Chip Select Setup Time Before WR, or RD	t <sub>CS</sub>	20	ne may mige	ili to aboltae	ns	phanothy
Chip Select Hold Time	t <sub>CH</sub>	0	rakeo et	TARETO	ns	MINISTER STATE
Read Data Hold Time	t <sub>DHR</sub>	10	JOEWY	80	ns	STEMARA
Write Data Hold Time	tDHW	0	ANV.		ns	wait2 vani
Muxed Address Valid Time to ALE Fall	t <sub>ASL</sub>	30	BIV		ns	logical tuo
Muxed Address Hold Time from ALE fall	t <sub>AHL</sub>	10	V <sub>L</sub>		ns	out Legio D
RD or WR High Setup to ALE Rise	tASD	25	NUASV		ns	officey Bay
Pulse Width ALE High	PWASH	60			ns	
ALE Low Setup to RD or WR Fall	tASED	40	10000000		ns	
Output Data Delay Time from RD	t <sub>DDR</sub>	20	KYSLEVS	120	ns	5
Data Setup Time	t <sub>DSW</sub>	100			ns	
IRQ Release from RD	t <sub>IRD</sub>		1205	. 2	μs	100000

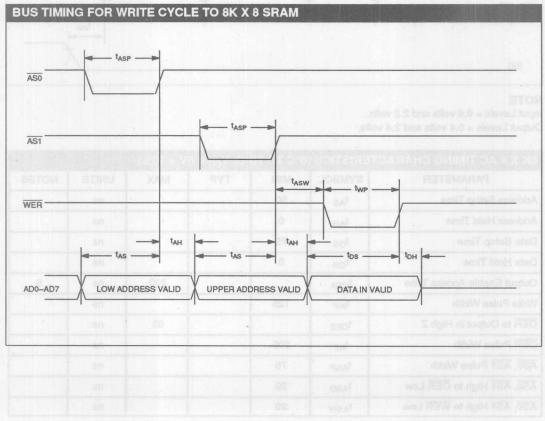


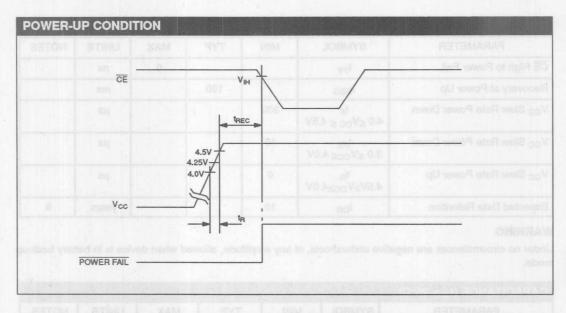


NOTE Input Levels = 0.8 volts and 2.2 volts. Output Levels = 0.4 volts and 2.4 volts.

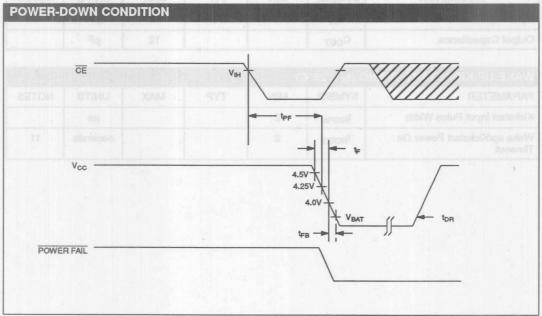
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t <sub>AS</sub>	50			ns	- Asia
Address Hold Time	t <sub>AH</sub>	0			ns	
Data Setup Time	t <sub>DS</sub>	75		HAT HE	ns	
Data Hold Time	t <sub>DH</sub>	0	- SAI		ns	
Output Enable Access Time	toea	SLAV SESS	MARIERADI V	200	ns	8
Write Pulse Width	t <sub>WP</sub>	125			ns	
OER to Output in High Z	t <sub>OEZ</sub>			50	ns	
OER Pulse Width	t <sub>RP</sub>	200			ns	
AS0, AS1 Pulse Width	t <sub>ASP</sub>	75			ns	
AS0, AS1 High to OER Low	t <sub>ASO</sub>	20			ns	
AS0, AS1 High to WER Low	t <sub>ASW</sub>	20			ns	











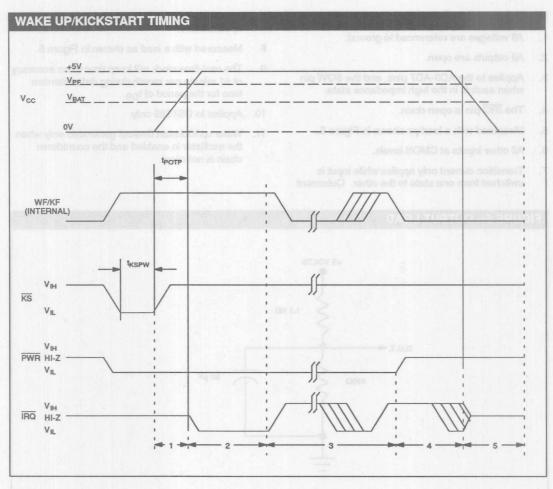
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE High to Power Fail	t <sub>PF</sub>	1		0	ns	
Recovery at Power Up	tREC	1.	150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤V <sub>CC</sub> ≤ 4.5V	300	of all		μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤V <sub>CC</sub> ≤ 4.0V	10	T VB.S		μѕ	
V <sub>CC</sub> Slew Rate Power Úp	t <sub>R</sub> 4.5V≥V <sub>CC≥</sub> 4.0V	0	- Tvo.x		μs	
Expected Data Retention	t <sub>DR</sub>	10	IM		years	9

#### WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE (t <sub>A</sub> = 25°C	;)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			12	pF	FACILIE
Output Capacitance	C <sub>OUT</sub>			12	pF	

WAKE UP/KICKSTART TIMING (t <sub>A</sub> = 25°C)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Kickstart Input Pulse Width	tkspw	2			μѕ	4.1	
Wake up/Kickstart Power On Timeout	t <sub>РОТО</sub>	2			seconds	11	



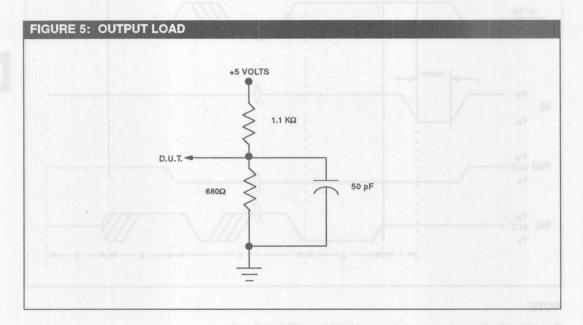
## NOTE

Time intervals shown above are referenced in Wake up/Kickstart section.

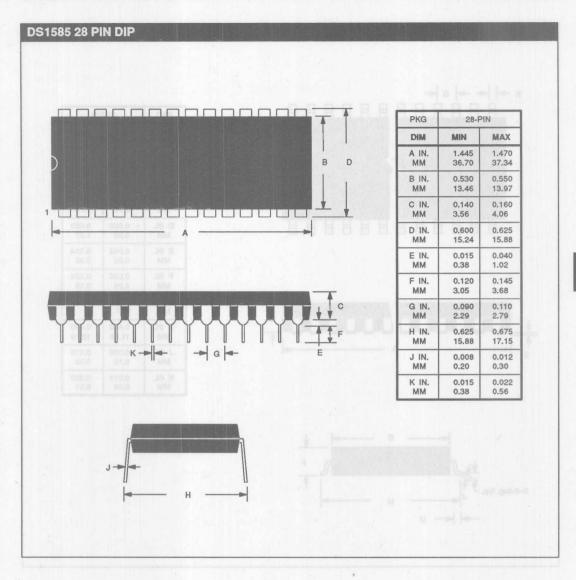
#### NOTES

- 1. All voltages are referenced to ground.
- 2. All outputs are open.
- Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
- 4. The IRQ pin is open drain.
- 5. Measured with a load as shown in Figure 5.
- 6. All other inputs at CMOS levels.
- Transition current only applies while input is switched from one state to the other. Quiescent

- input current given by input leakage current specification.
- 8. Measured with a load as shown in Figure 5.
- The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t<sub>DR</sub>.
- 10. Applies to DS1585 only.
- Wake up/Kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.

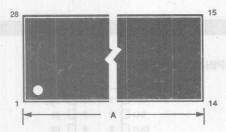


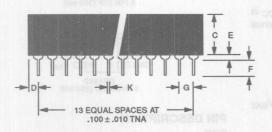




#### **DS1585S 28 PIN SOIC** 28-PIN PKG DIM MIN MAX A IN. 0.706 0.728 MM 17.93 18.49 B IN. 0.338 0.350 MM 8.58 8.89 C IN. 0.110 MM 2.18 2.79 0.050 D IN. 0.020 MM 0.58 1.27 0.002 0.014 0.36 F IN. 0.090 0.124 MM 2.29 3.15 BSC 0.050 G IN. 1.27 H IN. 0.460 0.480 MM 11.68 12.19 J IN. 0.006 0.013 MM 0.15 0.33 K IN. 0.014 0.020 0.36 0.51

#### **DS1585 28 PIN 740 MIL MODULE**





В

PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350 8.89	0.375 9.52
D IN.	0.100 2.54	0.130 3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.

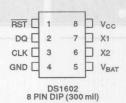


## DS1602 Elapsed Time Counter

#### **FEATURES**

- Two 32 bit counters keep track of real time and elapsed time
- · Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V<sub>BAT</sub> is less than 2.5 volts
- V<sub>CC</sub> powered counter counts seconds while V<sub>CC</sub> is above 4.25 volts and retains the count in the absence of V<sub>CC</sub> under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Maximum current drain of less than 1 μA from V<sub>BAT</sub> pin when serial port is disabled
- One byte protocol defines read/write, counter address and software clear function
- 8 pin dip or optional 8 pin SOIC
- Operating temperature range = -40°C to +85°C
- Reduced performance operation down to V<sub>CC</sub> = 2.5V

#### **PIN ASSIGNMENT**





#### **PIN DESCRIPTION**

RST - Reset CLK - Clock

DQ - Data input/output

GND - Ground

X1, X2 - Crystal inputs
VBAT - + Battery input

V<sub>CC</sub> - +5 volts

#### DESCRIPTION

The DS1602 is a real time clock/elapsed time counter designed to count seconds when  $V_{\rm CC}$  power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of  $V_{\rm CC}$ . The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The  $V_{\rm CC}$  powered counter will automatically record the amount of time that  $V_{\rm CC}$  power is applied. This function is particularly useful in determining the operational time of equipment in which the

DS1602 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1602 takes place via a 3 wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. A low cost 32.768 kHz crystal attaches directly to the XTAL1 and XTAL2 pins. If battery powered only operation is desired, the  $V_{\rm BAT}$  pin must be grounded and the  $V_{\rm CC}$  pin must be connected to the battery.

#### **OPERATION**

The main elements of the DS1602 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3 wire serial port. The port is activated by driving RST to a high state. With RST at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. Vcc must be present to access the DS1602. If V<sub>CC</sub> < V<sub>BAT</sub> the DS1602 will go into a battery backup mode which disables the serial port to conserve battery capacity. For battery only operations, the V<sub>BAT</sub> pin must be grounded and the V<sub>CC</sub> pin must be connected to the battery. This will keep the DS1602 out of battery backup mode. Battery powered operation down to 2.5V is possible with reduced speed performance on the serial port.

#### PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32 bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V<sub>CC</sub> active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at 2°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the IBAT current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous

counter will reset to zero when RST is taken low. Bit 1 of protocol (designated CVC) is used to clear the Vcc. active counter. When set to logical 1, the V<sub>CC</sub> active counter will reset to zero when RST is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8 bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

#### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RST input high. The RST input has two functions. First, RST turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the RST signal provides a method of terminating the protocol transfer or the 32 bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the RST input is transitioned low and the D/Q pin goes to a high impedance state. RST should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

#### **DATA INPUT**

Following the 8 bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until  $\overline{RST}$  is transitioned low to end data transfer and then high again to begin new data transfer.

#### **DATA OUTPUT**

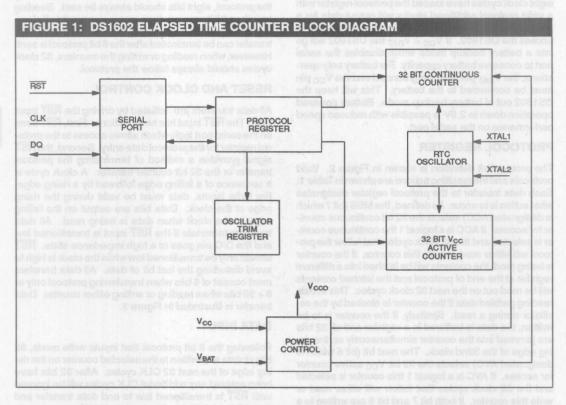
Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32 bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32 bit counter, RST must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

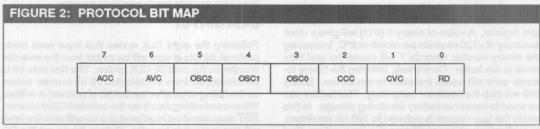
#### CRYSTAL SELECTION

A 32.768 kHz crystal, Daiwa Part No. DT26S or Seiko Part No. DS-VT-200 or equivalent can be directly connected to the DS1602 via pins 2 and 3. The crystal selected for use should have a specified load capacitance (C<sub>L</sub>) of 6 pF. Crystals with different load capacitance may cause the RTC oscillator to run faster or slower which effects the clock accuracy.

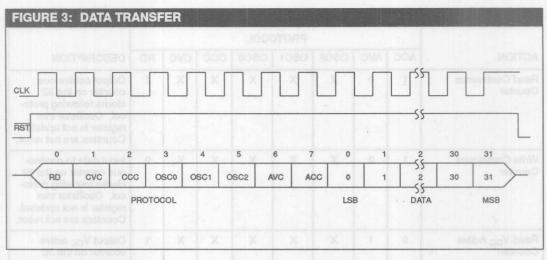
#### **BATTERY SELECTION**

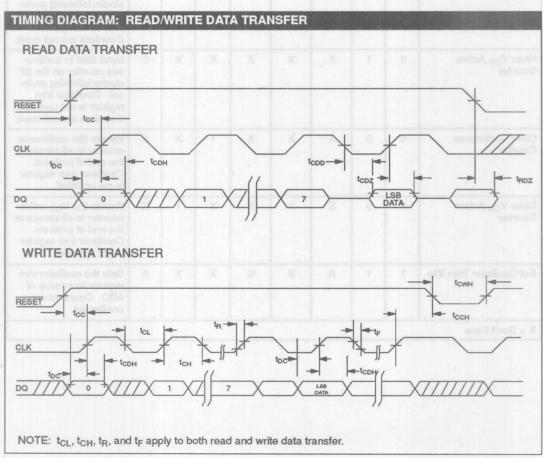
The battery selected for use with the DS1602 should have an output voltage between 2.5 and 3.5 volts. A lithium battery of 35 MAH or greater will run the elapsed time counter for over 10 years in the absence of power. Small lithium coin cell batteries produce both the proper output voltage and have the capacity to supply the DS1602 for the useable lifetime of the equipment where they are installed.





				PROTO	OCOL				
ACTION	ACC	AVC	OSC2	OSC1	OSC0	ccc	CVC	RD	DESCRIPTION
Read Continuous Counter	1	0	X	×	X	X	X	1	Output continuous counter on the 32 clocks following proto- col. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	21	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V <sub>CC</sub> Active Counter	0	1	×	X	X	X	X	1	Output V <sub>CC</sub> active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V <sub>CC</sub> Active Counter	0	1	X	X	×	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	×	×	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V <sub>CC</sub> Active Counter	0	0	Х	X	×	X	1	X	Resets the V <sub>CC</sub> active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	В	С	Х	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.





# 6

#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE -0.3V TO +7.0V -40°C TO +85°C -55°C TO +125°C

-260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C TO +85°C)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Supply Voltage	Vcc	4.5	5.0	5.5	V	up d to	
Battery Supply Voltage	V <sub>BAT</sub>	2.5	3.0	3.5	Velore	ran di xi	
Logic 1 Input	V <sub>IH</sub>	2.0	loses	V <sub>CC</sub> +0.3	V	A 17	
Logic 0 Input	V <sub>IL</sub>	-0.3	- cont	0.8	V	dwo1 To	

DC ELECTRICAL CHARA	ACTERISTICS (-4	40°C TO +	.85°C, V <sub>CC</sub> :	= 5V ±10%	)	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	Meanulted a Vist	-1-1	dor	+1	μА	pstovilA,
I/O Leakage	ILO	.B-1 -3	tha source of	+1	μΑ	logia on
Logic 1 Output	V <sub>OH</sub>	2.4			V	2
Logic 0 Output	V <sub>OL</sub>	.01		0.4	V	3
Active Supply Current	loc			o nig 100 or	mA	4
Timekeeping Current	I <sub>CC1</sub>	.11.	= TSA time	50	μА	5
Timekeeping Current	I <sub>BAT</sub>			400	nA	6
Leakage Current	IBATL		ancition	100	nA	11

CAPACITANCE (t <sub>A</sub> = 25	°C)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CI		5		pF	
I/O Capacitance	C <sub>VO</sub>		10		pF	
Crystal Capacitance	C <sub>X</sub>		6		pF	10

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	50		Ta a	ns	7.00
CLK to Data Hold	t <sub>CDH</sub>	70		BRU	ns	7
CLK to Data Delay	t <sub>CDD</sub>	vois diff to m	illerego lano	200	ns	7, 8, 9
CLK Low Time	t <sub>CL</sub>	250	silibeqa sini.	a enotiona adeute at the	ns	7
CLK High Time	t <sub>CH</sub>	250			ns	7
CLK Frequency	fclk	DC		2.0	MHz	7
CLK Rise & Fall	t <sub>F</sub> , t <sub>R</sub>	- Palvi		500	ns	ET ENAAA.
RST to CLK Setup	tcc	100	Veq		ns	7
CLK to RST Hold	t <sub>CCH</sub>	60	TABY.		ns	7
RST Inactive Time	t <sub>CWH</sub>	108	leV .		μs	7
RST Low to I/O High Z	t <sub>RDZ</sub>	-0.3	74	70	ns	7
CLK High to I/O High Z	tcDZ			20	ns	7

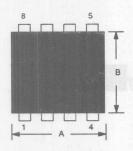
#### NOTES

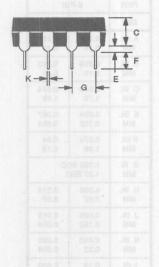
- 1. All voltages are reference to ground.
- Logic one voltages are specified at a source current of 1 mA.
- Logic zero voltages are specified at a sink current of 4 mA.
- 4. I<sub>CC</sub> is specified with the DQ pin open.
- I<sub>CC1</sub> is specified with V<sub>CC</sub> at 5.0V and RST = GND
- I<sub>BAT</sub> is specified with V<sub>CC</sub> < V<sub>BAT</sub> and V<sub>BAT</sub> within DC recommended operating conditions.

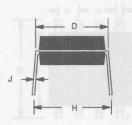
- Measured at V<sub>IH</sub> = 2.0V or V<sub>IL</sub> = 0.8V.
- 8. Measured at  $V_{OH} = 2.4V$  or  $V_{OL} = 0.4V$ .
- 9. Load capacitance = 50 pF.
- Specified as the load capacitance for which the crystal frequency is guaranteed (see crystal manufacturer's data sheet).
- Leakage current is the amount of current consumed from the battery when V<sub>CC</sub> is not present and the oscillator is turned off.





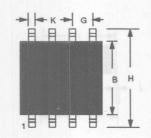


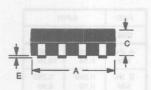


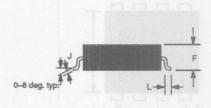


PKG	8-P	PIN
DIM	MIN	MAX
A IN. MM	0.360 9.14	0.400
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN. MM	0.015 0.38	0.040
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.4
J IN. MM	0.008 0.20	0.012
K IN.	0.015	0.021

## **DS1602 8 PIN SOIC 200 MIL**







PKG	8-P	IN
DIM	MIN	MAX
A IN.	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.007 0.254
FIN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BS 1.27 BS	
H IN.	0.302 7.67	0.318 8.07
J IN.	0.006 0.152	0.010 0.254
K IN.	0.013 0.33	0.020 0.508
LIN. MM	0.19 4.83	0.030 0.762

# DALLAS

# Elapsed Time Counter Module

#### **FEATURES**

- Two 32 bit counters keep track of real time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V<sub>BAT</sub> is less than 2.5 volts
- V<sub>CC</sub> powered counter counts seconds while V<sub>CC</sub> is above 4.25 volts and retains the count in the absence of V<sub>CC</sub> under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Powered internally by a lithium energy cell that provides over 10 years of operation
- One byte protocol defines read/write, counter address and software clear function
- Self contained crystal provides an accuracy of ±1 min per 300 hours of operation
- Operating temperature range = 0°C to +70°C
- Low profile SIP module

#### DESCRIPTION

The DS1603 is a real time clock/elapsed time counter designed to count seconds when  $V_{\rm CC}$  power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of  $V_{\rm CC}$ . The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The  $V_{\rm CC}$  powered counter will automatically record the amount of time that  $V_{\rm CC}$  power is applied. This function is particularly useful in determining the operational time of equipment in which the

#### **PIN ASSIGNMENT**

Vcc	•		1			
RST	ives		2			
DQ	BBFW		3			
NC	qqu		4			
CLK	0.8 1		5			
osc	0.84		6			
GND	CEAN A		7			
		0.00		100000	-1	

#### **PIN DESCRIPTION**

RST	rabita	Reset
CLK	B214	Clock
DQ	uniineo	Data Input/Output
GND	unilingo	Ground
Vcc	ner toll	+5 Volts
OSC	nan Jawa	1 Hz Oscillator Outpu
NC	national a	No Connection

DS1603 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1603 takes place via a 3 wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. The device contains a 32.768 kHz crystal which will keep track of time to within ±2 min/mo. An internal lithium energy source contains enough energy to power the continuous seconds counter for over 10 years.

6

#### **OPERATION**

The main elements of the DS1603 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3 wire serial port. The port is activated by driving RST to a high state. With RST at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. V<sub>CC</sub> must be present to access the DS1603. If V<sub>CC</sub> < the internal power supply (approximately 3.0 volts) the DS1603 will switch to internal power and disable the serial port to conserve energy. When running off of the internal power supply, only the continuous counter will continue to count and the counter powered by V<sub>CC</sub> will stop, but retain the count which had accumulated when V<sub>CC</sub> power was lost.

#### PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32 bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V<sub>CC</sub> active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at 25°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the internal power supply current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to zero when

RST is taken low. Bit 1 of protocol (designated CVC) is used to clear the V<sub>CC</sub> active counter. When set to logical 1, the V<sub>CC</sub> active counter will reset to zero when RST is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8 bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

#### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RST input high. The RST input has two functions. First, RST turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the RST signal provides a method of terminating the protocol transfer or the 32 bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the RST input is transitioned low and the D/Q pin goes to a high impedance state. RST should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

#### **DATA INPUT**

Following the 8 bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until RST is transitioned low to end data transfer and then high again to begin new data transfer.

#### DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32 bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32 bit counter, RST must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

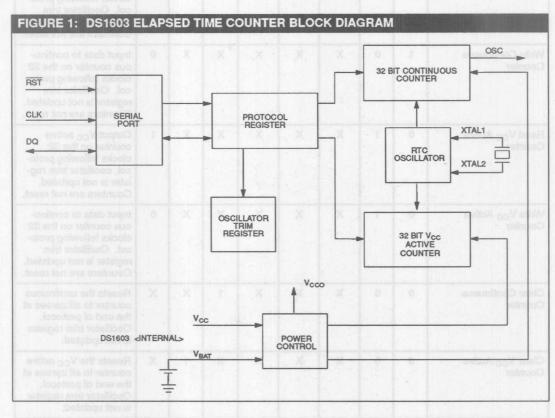
#### **OSCILLATOR OUTPUT**

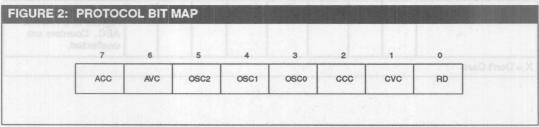
Pin 6 of the DS1603 module is a 1 Hz output signal. This signal is present only when  $V_{\rm CC}$  is applied and greater than the internal power supply. However, the output is guaranteed to meet TTL requirement only while  $V_{\rm CC}$  is within normal limits. This output can be used as a one

second interrupt or time tick needed in some applica-

#### **INTERNAL POWER**

The internal battery of the DS1603 module provides 35 MAH and will run the elapsed time counter for over 10 years in the absence of power.

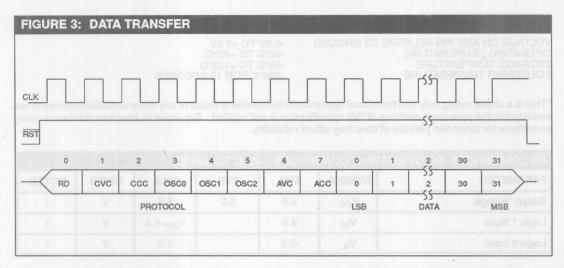


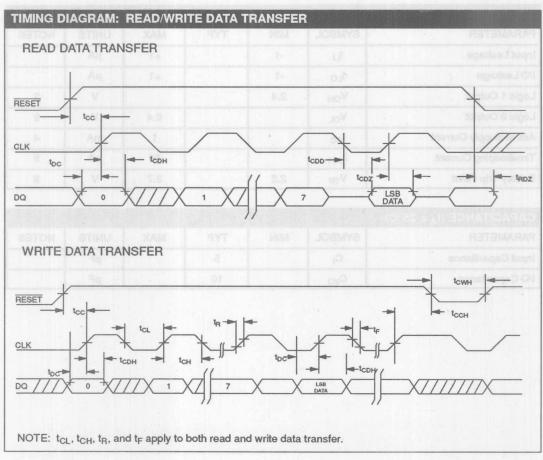


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	-			PROTO	OCOL				n 6 of the DS 1803 module
ACTION	ACC	AVC	OSC2	OSC1	OSC0	ccc	CVC	RD	DESCRIPTION
Read Continuous Counter	or <b>1</b> os woq to	0	X	X	X	X	X	tu <sup>1</sup> ju	Output continuous counter on the 32 clocks following proto- col. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X.	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V <sub>CC</sub> Active Counter	0	1	X	X	X	X	Х	1	Output V <sub>CC</sub> active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V <sub>CC</sub> Active Counter	0	1	Х	×	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	×	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V <sub>CC</sub> Active Counter	0	0	Х	Х	X	X	1	Х	Resets the V <sub>CC</sub> active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	В	С	Х	Х	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.







#### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.5V TO +7.0V -40°C TO +85°C -55°C TO +125°C

-260°C FOR 10 SECONDS

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C TO +85°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Supply Voltage	Vcc	4.5	5.0	5.5	V	1				
Logic 1 Input	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	1				
Logic 0 Input	V <sub>IL</sub>	-0.3		0.8	V	1				

DC ELECTRICAL CHAR	ACTERISTICS (-2	10°C 10 +	85°C, VCC	= 5V ±10%		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	ILI	-1		+1	μА	UACEN
I/O Leakage	I <sub>LO</sub>	-1		+1	μА	
Logic 1 Output	V <sub>OH</sub>	2.4			V	2
Logic 0 Output	V <sub>OL</sub>			0.4	V	3
Active Supply Current	Icc	V .	/ \	1/	mA	4
Timekeeping Current	I <sub>CC1</sub>			50	μА	5
Battery Trip Point	V <sub>TP</sub>	2.2		3.7	V	9

CAPACITANCE (t <sub>A</sub> = 25°C)										
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES				
Input Capacitance	CI		5	Halio	pF	THE PLAN				
I/O Capacitance	C <sub>VO</sub>		10		pF					

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	50			ns	6
CLK to Data Hold	t <sub>CDH</sub>	70			ns	6
CLK to Data Delay	tcDD			200	ns	6, 7, 8
CLK Low Time	t <sub>CL</sub>	250		Tenange was be	ns	6
CLK High Time	t <sub>CH</sub>	250			ns	6
CLK Frequency	fclk	DC		2.0	MHz	6
CLK Rise & Fall	t <sub>F</sub> , t <sub>R</sub>			500	ns	l d
RST to CLK Setup	tcc	100			ns	6
CLK to RST Hold	t <sub>CCH</sub>	60		LI TE	ns	6
RST Inactive Time	t <sub>CWH</sub>	1			μА	6
RST Low to I/O High Z	t <sub>RDZ</sub>			70	ns	6
CLK High to I/O High Z	tcpz			20	ns	6

#### NOTES

- 1. All voltages are reference to ground.
- Logic one voltages are specified at a source current of 1 mA.
- Logic zero voltages are specified at a sink current of 4 mA.
- 4. I<sub>CC</sub> is specified with the DQ pin open.
- 5.  $I_{CC1}$  is specified with  $V_{CC}$  at 5.0V and  $\overline{RST} = GND$ .

- 6. Measured at  $V_{IH} = 2.0V$  or  $V_{IL} = 0.8V$ .
- 7. Measured at  $V_{OH} = 2.4V$  or  $V_{OL} 0.4V$ .
- 8. Load capacitance = 50 pF.
- Battery trip point is the point at which the V<sub>CC</sub> powered counter and the serial port stop operation

## **DS1603 7 PIN MODULE** PKG 7-PIN DIM MIN MAX 0.830 21.08 0.850 21.59 0.650 16.51 0.670 C IN. 0.310 7.87 0.330 8.38 0.015 D IN. MM 0.030 В E IN. 0.110 0.140 3.56 0.015 0.38 0.021 G IN. 0.090 0.110 H IN. 0.105 2.67 0.135 3.43 J IN. 0.360 9.14 0.390 C C E D

# DALLAS

# Nonvolatile Timekeeping RAM

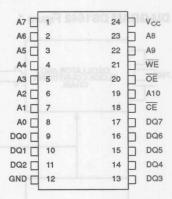
#### **FEATURES**

- Form, fit, and function compatible with the MK48T02 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 2K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- · Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V<sub>CC</sub> power supply tolerance

#### DESCRIPTION

The DS1642 is an 2K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 2K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/ write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the

#### PIN ASSIGNMENT



#### **PIN DESCRIPTION**

PIN DESC	MIP	ION
A0-A10		Address Input
CE	-	Chip Enable
OE		Output Enable
WE	-	Write Enable
Vcc	-	+5 Volts
GND	-	Ground
DQ0-DQ7	-	Data Input/Output

day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1642 also contains its own powerfail circuitry which deselects the device when the V<sub>CC</sub> supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V<sub>CC</sub> as errant access and update cycles are avoided.

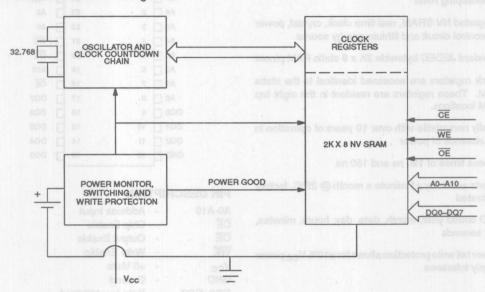
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#### **CLOCK OPERATIONS-READING THE CLOCK**

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1642 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt

is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

#### **BLOCK DIAGRAM DS1642 Figure 1**



#### TRUTH TABLE DS1642 Table 1

Vcc	CE	OE	WE	MODE	DQ	POWER
eour dwing eleck u	V <sub>IH</sub>	X	×	DESELECT	HIGH Z	STANDBY
EVOLTE LANG	VIL	X	V <sub>IL</sub>	WRITE	DATA IN	ACTIVE
5 VOLTS ± 10%	VIL	V <sub>IL</sub>	V <sub>IH</sub>	READ	DATA OUT	ACTIVE
	VIL	VIH	V <sub>IH</sub>	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V <sub>BAT</sub>	X	X	×	DESELECT	HIGH Z	CMOS STANDBY
<v<sub>BAT</v<sub>	X	Х	×	DESELECT	HIGH Z	DATA RETENTION MODE

### 1-

#### SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1642 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

# STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The OSC bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

#### FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is

running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e.,  $\overline{CE}$  low, and  $\overline{OE}$  low) and address for seconds register remain valid and stable.

#### **CLOCK ACCURACY**

The DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1642 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T02 family) will not have any effect even though the DS1642 appears to accept calibration data.

# 6

#### DS1642 REGISTER MAP - BANK1 Table 2

ADDRESS	vietted n			FILMOT	FUNCTION					
ADDRESS	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	FUNCTI	ON
7FF	rbotoega	e) old Ser	(e ork of )	upe-ylate	ny - yd	bareleb)	atab baar	ritive-avit	YEAR	00-99
7FE	X	X	X	austo raus y which n	59E - 6	IN CHARGE SERV	res in nem ses Active	op 2W 1e	MONTH	01-12
7FD	X	X		-	-		-	-	DATE	01-31
7FC	X	FT	X	X	X	-	-	-	DAY	01-07
7FB	X	X	-	77-1		-	-	-	HOUR	00-23
7FA	X	-	-	-			-		MINUTES	00-59
7F9	OSC					-	-	-	SECONDS	00-59
7F8	W	R	-	16-11	-	-	-	4	CONTROL	Α

OSC = STOP BIT W = WRITE BIT R = READ BIT X = UNUSED FT = FREQUENCY TEST

#### NOTES

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

#### RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever WE (write enable) is high, and CE (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within tAA after the last address input is stable, providing that the CE and OE access times are satisfied. If CE or OE access times are not met, valid data will be available at the latter of chip enable access (t<sub>CEA</sub>) or at output enable access time (t<sub>OEA</sub>). The state of the data input/output pins (DQ) is controlled by CE and OE. If the outputs are activated before tAA, the data lines are driven to an intermediate state until tAA. If the address inputs are changed while CE and OE remain valid, output data will remain valid for output data hold time (tOH) but will then go indeterminate until the next address access.

#### WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever  $\overline{WE}$  and  $\overline{CE}$  are in their active state. The start of a write is referenced to the latter occurring transition of  $\overline{WE}$  or  $\overline{CE}$ . The addresses must be held valid throughout the cycle.  $\overline{CE}$  or  $\overline{WE}$  must return inactive for a minimum of  $t_{WR}$  prior to the initiation of another read or write cycle. Data in must be valid  $t_{DS}$  prior to the end of write and remain valid for  $t_{DH}$  afterward. In a typical application, the  $\overline{OE}$  signal will be high during a write cycle. However,  $\overline{OE}$  can be active provided that care is taken with the data bus to avoid bus contention. If  $\overline{OE}$  is low prior to  $\overline{WE}$  transitioning low the data bus can become active with read data defined by the address inputs. A low transition on  $\overline{WE}$  will then disable the outputs  $t_{WEZ}$  after  $\overline{WE}$  goes active.

#### DATA RETENTION MODE

When  $V_{CC}$  is within nominal limits ( $V_{CC} > 4.5$  volts) the DS1642 can be accessed as described above by read or write cycles. However, when  $V_{CC}$  is below the power fail point  $V_{PF}$  (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the  $\overline{CE}$  signal. When  $V_{CC}$  falls below the level of the internal battery supply, power input is switched from the  $V_{CC}$  pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until  $V_{CC}$  is returned to nominal level.

#### INTERNAL BATTERY LONGEVITY

The DS1642 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V<sub>CCI</sub> supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V<sub>CC</sub> power. The DS1642 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1642 will be much longer than 10 years since no internal lithium battery energy is consumed when V<sub>CC</sub> is present. In fact, in most applications, the life expectancy of the DS1642 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

### **ABSOLUTE MAXIMUM RATINGS\***

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO +70°C -20°C TO +70°C 260°C FOR 10 SECONDS

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	VIH	2.2		V <sub>CC</sub> +0.3	٧	LOOM
Logic 0 Voltage All Inputs	V <sub>IL</sub>	-0.3		0.8	V	

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le t_A \le +70^{\circ}C; V_{CC} (MAX) \le V_{CC} \le V_{CC} (MIN))$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V <sub>CC</sub> Power Supply Current	I <sub>CC1</sub>	1	30	50	mA	2, 3
TTL Standby Current (CE = VIH)	I <sub>CC2</sub>	05	3 14	6	mA	2, 3
CMOS Standby Current (CE=V <sub>CC</sub> -0.2V)	I <sub>CC3</sub>	DA .	2	4.0	mA	2, 3
Input Leakage Current (any input)	IIL I	-1	not not	+1	μА	ala Saha
Output Leakage Current	loL	-1	unt	+1	μА	Think! etc.
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0 mA)	V <sub>OH</sub>	2.4		8	V	) TEST (
Output Logic 0 Voltage (I <sub>OUT</sub> = +2.1 mA)	V <sub>OL</sub>			0.4	VO V	alevel, hu ill notion
Write Protection Voltage	V <sub>TP</sub>	4.0	4.25	4.5	V	screens as each

#### AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } +70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} + 10\%)$ 

PARAMETER	SYMBOL	DS1642-12		DS1642-15		HAMPE	MITARIES
		MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120		150		ns	
Address Access Time	t <sub>AA</sub>	eb ent to edication	120	anolionui enoliona r	150	ns	nis is a s
CE Access Time	t <sub>CEA</sub>	may atte	120	wing belon	150	ns	ritin mun
CE Data Off Time	t <sub>CEZ</sub>		40	SO CHIEF	50	ns	usunn
Output Enable Access Time	tOEA		100	manan i	120	ns	
Output Enable Data Off Time	toez		40	ment of the	50	ns	The State of the S
Output Enable to DQ Low-Z	toEL	5		5		ns	A. Auth
CE to DQ Low-Z	t <sub>CEL</sub>	5		5		ns	
Output Hold from Address	ŧон	5	× 1	5		ns	1777
Write Cycle Time	twc	120		150	TO A CLAS	ns	PAGE 157 V
Address Setup Time	t <sub>AS</sub>	0		0		ns	
CE Pulse Width	tcew	100		120		ns	
Address Hold from End of Write	t <sub>AH</sub>	15		20	1000	ns	inonu
Write Pulse Width	twew	120		150	htV = BO	ns	IL Stand
WE Data Off Time	twez		40	nool ]	50	ns	MOS SUM
WE or CE Inactive Time	t <sub>WR</sub>	10		15		ns	100 V = 3
Data Setup Time	t <sub>DS</sub>	85		110	hdus Aus)	ns	100.1700
Data Hold Time High	t <sub>DH</sub>	15		20	- 1	ns	ent worken

### **AC TEST CONDITIONS**

Input Levels: 0V TO 3V

Transition Times: 5 ns

## CAPACITANCE

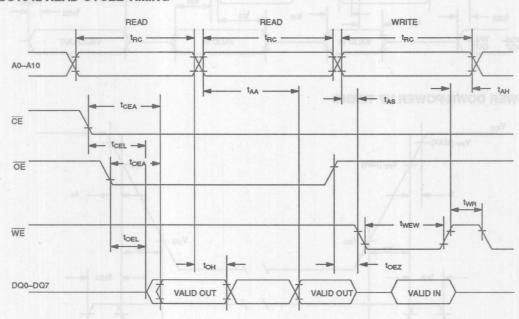
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	CI			7	pF	
Capacitance on DQ pins	C <sub>DQ</sub>			10	pF	

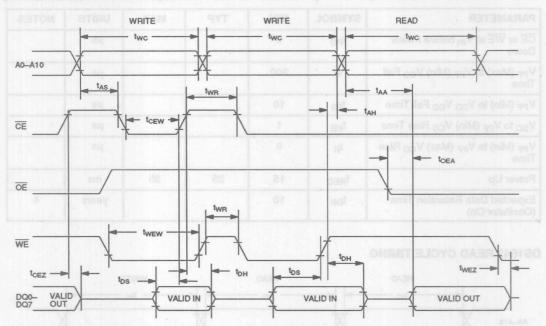
## AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE or WE at V <sub>IH</sub> before Power Down	t <sub>PD</sub>	0			μѕ	
V <sub>PF</sub> (Max) to V <sub>PF</sub> (Min) V <sub>CC</sub> Fall Time	t <sub>F</sub>	300			μs	GIRLO.
V <sub>PF</sub> (Min) to V <sub>SO</sub> V <sub>CC</sub> Fall Time	t <sub>FB</sub>	10			μѕ	
V <sub>SO</sub> to V <sub>PF</sub> (Min) V <sub>CC</sub> Rise Time	t <sub>RB</sub>	1	1	Wao! T	μѕ	3
V <sub>PF</sub> (Min) to V <sub>PF</sub> (Max) V <sub>CC</sub> Rise Time	t <sub>R</sub>	0			μs	
Power Up	t <sub>REC</sub>	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t <sub>DR</sub>	10	land at		years	4

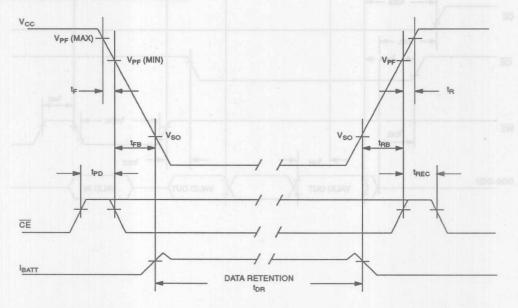
#### **DS1642 READ CYCLE TIMING**



#### DS1642 WRITE CYCLE TIMING



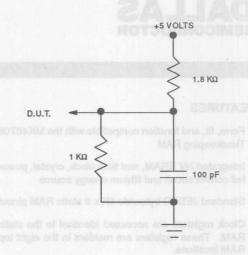
#### **POWER DOWN/POWER UP TIMING**



#### **NOTES**

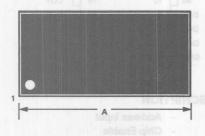
- 1. All voltages are referenced to ground.
- 2. Typical values are at 25°C and nominal supplies.
- 3. Outputs are open.
- 4. Data retention time is at 25°C and is calculated from the date code on the device package plus one year. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

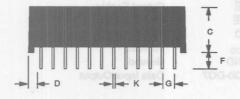
#### **OUTPUT LOAD**

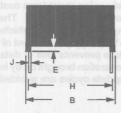


# 6

#### **DS1642 24 PIN PACKAGE**







PKG	24-PIN			
DIM	MIN	MAX		
A IN.	1.270 37.34	1.290 37.85		
B IN.	0.675 17.15	0.700 17.78		
C IN.	0.315 8.00	0.335 8.51		
D IN.	0.075 1.91	0.105 2.67		
E IN.	0.015 0.38	0.030 0.76		
F IN.	0.120 3.05	0.160 4.06		
G IN. MM	0.090 2.29	0.110 2.79		
H IN.	0.590 14.99	0.630 16.00		
J IN.	0.008 0.20	0.012 0.30		
K IN.	0.015 0.43	0.025 0.58		



# Nonvolatile Timekeeping RAM

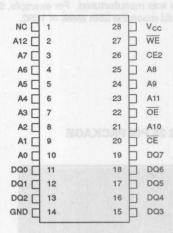
#### **FEATURES**

- Form, fit, and function compatible with the MK48T08 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 8K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V<sub>CC</sub> power supply tolerance

#### DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/ write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

A0-A12	-	Address Input
CE	-	Chip Enable
CE2	-	Chip Enable
OE	-	Output Enable
WE	-	Write Enable
NC	-	No Connection
Vcc		+5 Volts
GND	-	Ground
DQ0-DQ7		Data Input/Outpu

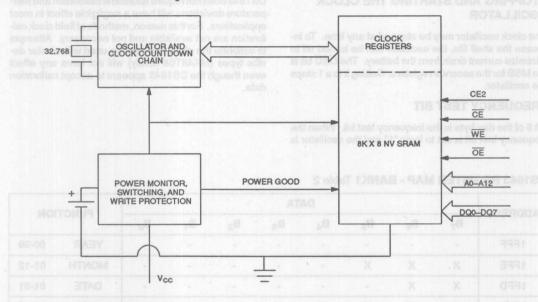
day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own powerfail circuitry which deselects the device when the  $\rm V_{CC}$  supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low  $\rm V_{CC}$  as errant access and update cycles are avoided.

#### CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt

is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

## **BLOCK DIAGRAM DS1643 Figure 1**



#### TRUTH TABLE DS1643 Table 1

Vcc	CE	CE2	OE	WE	MODE	DQ	POWER
earth carron	VIH	Х	X	X	DESELECT	HIGH Z	STANDBY
69-00 SQN00	X	V <sub>IL</sub>	X	X	DESELECT	HIGH Z	STANDBY
5 VOLTS ± 10%	VIL	V <sub>IH</sub>	X	VIL	WRITE	DATA IN	ACTIVE
	VIL	VIH	VIL	VIH	READ	DATA OUT	ACTIVE
	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	VIH	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V <sub>BAT</sub>	X	Х	Х	X	DESELECT	HIGH Z	CMOS STANDBY
<v<sub>BAT</v<sub>	X	X.	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

#### SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

# STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The OSC bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

#### **FREQUENCY TEST BIT**

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is

running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e.,  $\overline{\text{CE}}$  low,  $\overline{\text{OE}}$  low, CE2 high, and address for seconds register remain valid and stable).

#### **CLOCK ACCURACY**

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643 appears to accept calibration data

#### DS1643 REGISTER MAP - BANK1 Table 2

ADDRESS		DATA						FUNCTIO		
	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	FUNCTI	ON
1FFF	11-11	- 1	-	-	-	-	-	4	YEAR	00-99
1FFE	X	X	X	- "	- 1			- 1	MONTH	01-12
1FFD	X	X		-	100	-	-	lov I	DATE	01-31
1FFC	X	FT	X	X	X			eldal Es	DAY	01-07
1FFB	X	X			100	500	38	ean	HOUR	00-23
1FFA	X	E IJ:	Della .	TOO D		v	v		MINUTES	00-59
1FF9	OSC	7.11	STLE	trous to	iond.	V- :	y -	.v -	SECONDS	00-59
1FF8	W	R		-		-	-		CONTROL	Α

OSC = STOP BIT W = WRITE BIT R = READ BIT X = UNUSED FT = FREQUENCY TEST

#### NOTES

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

#### RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever WE (write enable) is high, CE (chip enable) is low and CE2 (chip enable 2) is high. The device architecture allows ripplethrough access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within tAA after the last address input is stable, providing that the CE, CE2 and OE access times are satisfied. If CE, CE2, or OE access times are not met, valid data will be available at the latter of chip enable access (t<sub>CFA</sub>) or at output enable access time (toeA). The state of the data input/output pins (DQ) is controlled by CE, CE2, and OE. If the outputs are activated before tAA, the data lines are driven to an intermediate state until tAA. If the address inputs are changed while CE, CE2, and OE remain valid, output data will remain valid for output data hold time (toH) but will then go indeterminate until the next address access.

#### WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever  $\overline{WE}$ ,  $\overline{CE}$ , and CE2 are in their active state. The start of a write is referenced to the latter occurring transition of  $\overline{WE}$ ,  $\overline{CE}$ , or CE2. The addresses must be held valid throughout the cycle.  $\overline{CE}$ , CE2, or  $\overline{WE}$  must return inactive for a minimum of  $t_{WR}$  prior to the initiation of another read or write cycle. Data in must be valid  $t_{DS}$  prior to the end of write and remain valid for  $t_{DH}$  afterward. In a typical application, the  $\overline{OE}$  signal will be high during a write cycle. However,  $\overline{OE}$  can be active provided that care is taken with the data bus to avoid bus contention. If  $\overline{OE}$  is low prior to  $\overline{WE}$  transitioning low the data bus can become active with read data defined by the address inputs. A low transition on  $\overline{WE}$  will then disable the outputs  $t_{WEZ}$  after  $\overline{WE}$  goes active.

### **DATA RETENTION MODE**

When  $V_{CCI}$  is within nominal limits ( $V_{CC} > 4.5$  volts) the DS1643 can be accessed as described above by read or write cycles. However, when  $V_{CCI}$  is below the power fail point  $V_{PF}$  (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the  $\overline{CE}$  and CE2 signals. When  $V_{CCI}$  falls below the level of the internal battery supply, power input is switched from the  $V_{CCI}$  pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until  $V_{CCI}$  is returned to nominal level.

#### **INTERNAL BATTERY LONGEVITY**

The DS1643 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V<sub>CCI</sub> supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V<sub>CCI</sub> power. The DS1643 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1643 will be much longer than 10 years since no internal lithium battery energy is consumed when V<sub>CCI</sub> is present. In fact, in most applications, the life expectancy of the DS1643 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS\*

VOLTAGE ON ANY PIN RELATIVE TO GROUND OPERATING TEMPERATURE STORAGE TEMPERATURE SOLDERING TEMPERATURE

-0.3V TO +7.0V 0°C TO +70°C -20°C TO +70°C 260°C FOR 10 SECONDS

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Supply Voltage	Vcc	4.5	5.0	5.5	ana Vena a	ugni dand	
Logic 1 Voltage All Inputs	V <sub>IH</sub>	2.2	o sugue so litru eteric	V <sub>CC</sub> +0.3	V	ot) emit b	
Logic 0 Voltage All Inputs	VIL	-0.3		0.8	٧	searbha b	

# DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le t_A \le +70^{\circ}C; V_{CC} (MAX) \le V_{CC} \le V_{CC} (MIN))$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Average V <sub>CC</sub> Power Supply Current	l <sub>CC1</sub>	a the out	30	55	mA	2,3	
TTL Standby Current (CE = V <sub>IH</sub> , CE2 = V <sub>IL</sub> )	l <sub>CC2</sub>	of pect	3	6	mA	2, 3	
CMOS Standby Current (CE=V <sub>CC</sub> -0.2V, CE2=GND+0.2V)	Іссз	noil na nain wa	2	4.0	mA	2,3	
Input Leakage Current (any input)	I <sub>IL</sub>	-1	us can pacal drans induta.	+1	μА	in nine on	
Output Leakage Current	loL	-1	M slugiuo e	+1	μА	holismeni Turk and	
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0 mA)	V <sub>OH</sub>	2.4			V		
Output Logic 0 Voltage (I <sub>OUT</sub> = +2.1 mA)	V <sub>OL</sub>			0.4	V		
Write Protection Voltage	V <sub>TP</sub>	4.0	4.25	4.5	V		

# $(0^{\circ}\text{C to } +70^{\circ}\text{C}, \text{V}_{\text{CC}} = 5.0\text{V} + 10\%)$

## AC ELECTRICAL CHARACTERISTICS

RAX UNITS LIGOTES	OVMDOL	DS16	643-12	DS16	43-15	LINITO	NOTEC
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120		150		ns	A SERVICE
Address Access Time	t <sub>AA</sub>		120		150	ns	900
CE and CE2 Access Time	tCEA		120	esi l	150	ns	(nlM) 99
CE and CE2 Data Off Time	t <sub>CEZ</sub>		40	ent 1	50	ns	aV of og
Output Enable Access Time	toea		100	pit	120	ns	(niM) aq
Output Enable Data Off Time	toez		40		50	ns	- 6011
Output Enable to DQ Low-Z	toEL	5		5		ns	UN 10110
CE and CE2 to DQ Low-Z	t <sub>CEL</sub>	5		5	Bigal no	ns	Apressed Deciliator
Output Hold from Address	tон	5		5		ns	
Write Cycle Time	twc	120		150	MINAT 3.	ns	11843 F
Address Setup Time	tas	0		0	en eller	ns	
CE and CE2 Pulse Width	tcew	100		120	- ori -	ns	
Address Hold from End of Write	t <sub>AH</sub>	15		20		ns	
Write Pulse Width	t <sub>WEW</sub>	120		150		ns	
WE Data Off Time	twez		40	PI I I	50	ns	
WE or CE Inactive Time	t <sub>WR</sub>	10		15	1	ns	gap 35
Data Setup Time	t <sub>DS</sub>	85		110	lana mot	ns	
Data Hold Time High	t <sub>DH</sub>	15		20		ns	

# **AC TEST CONDITIONS**

Input Levels: Transition Times: 0V TO 3V 5 ns

# CAPACITANCE

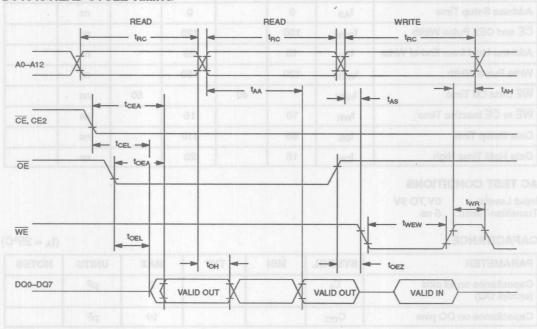
 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	CI		Tue au	7	pF	500-000
Capacitance on DQ pins	C <sub>DQ</sub>	THE.		10	pF	

# AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE2, CE or WE at V <sub>IH</sub> before Power Down	t <sub>PD</sub>	0			μs	aless O best
V <sub>PF</sub> (Max) to V <sub>PF</sub> (Min) V <sub>CC</sub> Fall Time	t <sub>F</sub>	300	. And		μs	klress Ad
V <sub>PF</sub> (Min) to V <sub>SO</sub> V <sub>CC</sub> Fall Time	t <sub>FB</sub>	10	OEA		μs	SIQ bos S
V <sub>SO</sub> to V <sub>PF</sub> (Min) V <sub>CC</sub> Rise Time	t <sub>RB</sub>	<sup>64</sup> 1	CEZ	91	μs	E and OB
V <sub>PF</sub> (Min) to V <sub>PF</sub> (Max) V <sub>CC</sub> Rise Time	t <sub>R</sub>	0	OEA	ne ime	μs	ulput Bina
Power Up	tREC	15	25	35	ms	non-il tuette
Expected Data Retention Time (Oscillator On)	t <sub>DR</sub>	10	.se		years	4

# **DS1643 READ CYCLE TIMING**

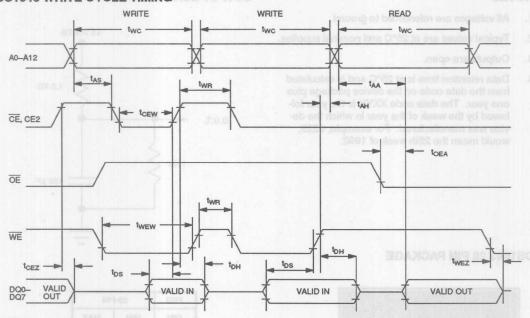


## NOTE

The CE2 control signal functions exactly the same as the  $\overline{\text{CE}}$  signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to  $\overline{\text{CE}}$  apply to CE2 with the opposite active state.

# 6

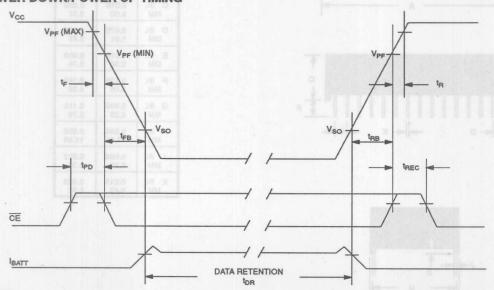
### DS1643 WRITE CYCLE TIMING



#### NOTE

The CE2 control signal functions exactly the same as the  $\overline{\text{CE}}$  signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to  $\overline{\text{CE}}$  apply to CE2 with the opposite active state.

#### POWER DOWN/POWER UP TIMING

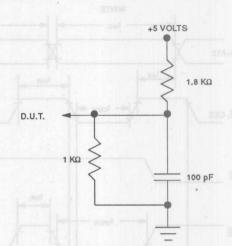


## NOTE

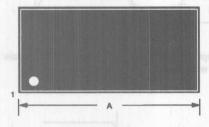
The CE2 control signal functions exactly the same as the  $\overline{\text{CE}}$  signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to  $\overline{\text{CE}}$  apply to CE2 with the opposite active state.

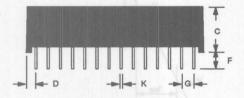
## NOTES

- OUTPUT LOAD
- 1. All voltages are referenced to ground.
- 2. Typical values are at 25°C and nominal supplies.
- 3. Outputs are open.
- Data retention time is at 25°C and is calculated from the date code on the device package plus one year. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

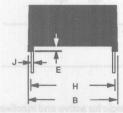


## **DS1643 28 PIN PACKAGE**





PKG	28-F	PIN
DIM	MIN	MAX
A IN.	1.470 37.34	1.490 37.85
B IN. MM	0.675 17.15	0.700 17.78
C IN.	0.315 8.00	0.335 8.51
D IN.	0.075 1.91	0.105 2.67
E IN.	0.015 0.38	0.030 0.76
F IN.	0.120 3.05	0.160 4.06
G IN.	0.090 2.29	0.110 2.79
H IN.	0.590 14.99	0.630 16.00
J IN.	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58







# DS2404 EconoRAM Time Chip

### **FEATURES**

- Unique 1-wire interface requires only one port pin for communication
- Contains real-time clock/calendar in binary format
- 4096 bits of SRAM organized in 16 pages, 256 bits per page
- Interval timer can automatically accumulate time when power is applied
- Programmable cycle counter can accumulate the number of system power-on/off cycles
- Programmable alarms can be set to generate interrupts for interval timer, real-time clock, and/or cycle counter
- Write protect feature provides tamper-proof time data
- Programmable expiration date that will limit access to SRAM and timekeeping
- Data integrity assured with strict read/write protocols
- 3-wire I/O available for high speed data communications
- Unique 64-bit factory lasered ROM available
- Space-saving 16-pin SOIC package
- Operating temperature range from -20° C to +85° C
- Operating voltage range from 2.8 to 5.5 Volts

### DESCRIPTION

The DS2404 EconoRAM Time Chip offers a simple solution for storing and retrieving vital data and time information with minimal hardware. The DS2404 contains a unique lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts and 4096 bits of SRAM. Two separate ports are provided for communication, 1-wire and 3-wire. Using the 1-wire port, only one pin is required for communication, and the lasered ROM can be read even when the DS2404 is without power. The 3-wire port provides high

#### **PIN ASSIGNMENT**

	1			-	1100
VCC	1	0	16	ш	VCC
IRQ	2		15		X1
RST	3		14		X2
DQ	4		13		GND
1/0	5		12		NC
CLK	6		11		1HZ
NC I	7		10		VBATO
GND	8		9		VBATB

16 PIN SOIC (300 Mil)

#### **PIN DESCRIPTION**

Pin#	Pin Name	Description
Pin 1&16	-Vcc	2.8 to 5.5 Volts
Pin 2	- IRQ	Interrupt Output
Pin 3	- RST	3-Wire Reset Input
Pin 4	- DQ	3-Wire Input/Output
Pin 5	- VO	1-wire Input/Output
Pin 6	- CLK	3-Wire Clock Input
Pin 7 & 12	- NC	No Connection
Pin 8 & 13	- GND	Ground
Pin 9	- V <sub>BATB</sub>	Battery Backup Input
Pin 10	- V <sub>BATO</sub>	Battery Operate Input
Pin 11	- 1 Hz	1 Hz Output
Pin 14 & 15	- X <sub>1</sub> ,X <sub>2</sub>	Crystal Connections

speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS2404 insures data integrity. Utilizing backup energy sources, the data is nonvolatile and allows for stand-alone operation.

The DS2404 features can be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, expiration timer, and event scheduler.

#### **DETAILED PIN DESCRIPTION**

Pin	Symbol	Description					
Pin 1 & 16	V <sub>CC</sub>	Power input pins for $V_{CC}$ operate mode. 2.8 to 5.5 volts operation. Either pin can be used for $V_{CC}$ . Only one is required for normal operation. (See $V_{BATO}$ pin description and "Power Control" section).					
Pin 2	ĪRQ	Interrupt output pin: Open drain.					
Pin 3	RST	Reset input pin for 3-wire operation. (See "Parasite Power" section.)					
Pin 4	DQ	Data input/output pin for 3-wire operation.					
Pin 5	1/0	Data input/output for 1-wire operation: Open drain. (See "Parasite Power" section.)					
Pin 6	CLK	Clock input pin for 3-wire operation.					
Pin 7 & 12	NC	No connection pins.					
Pin 8, 13	GND	Ground pin: Either pin can be used for ground.					
Pin 9	V <sub>BATB</sub>	Battery backup input pin: Battery voltage can be 2.8 to 5.5 volts. (See VBATO pin description and "Power Control" section.)					
Pin 10 V <sub>BATO</sub>		<b>Battery operate input pin</b> for 2.8 to 5.5 volt operation. The V <sub>CC</sub> & V <sub>BATB</sub> pins must be grounded when this pin is used to power the chip. (See "Power Control" section.)					
Pin 11	1Hz	1 Hz square wave output: Open drain.					
Pin 14, 15	X <sub>1</sub> , X <sub>2</sub>	Crystal pins. Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S (be sure to request 6 pF load capacitance). Crystals may be ordered directly from Dallas Semiconductor. Part number is DS9032 NOTE: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.					

#### **OVERVIEW**

The DS2404 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

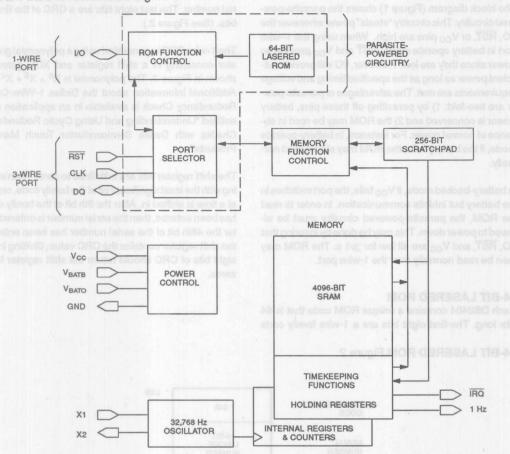
Two communication ports are provided, a 1-wire port and a 3-wire port. A port selector determines which of the two ports is being used. The communication ports and the ROM are parasite-powered via I/O,  $\overline{RST}$ , or  $V_{CC}$ . This allows the ROM to be read in the absence of power. The ROM data is accessible only through the 1-wire port. The scratchpad and memory are accessible via either port.

If the 3-wire port is used, the master provides one of four memory function commands: 1) read memory, 2) read scratchpad, 3) write scratchpad, or 4) copy scratchpad. The only way to write memory is to first write the scratchpad and then copy the scratchpad data to memory. (See Figure 6.)

If the 1-wire port is used, the memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands.

The "Power Control" section provides for two basic power configurations, battery operate mode and  $V_{CC}$  operate mode. The battery operate mode utilizes one supply connected to  $V_{BATO}$ . The  $V_{CC}$  operate mode may utilize two supplies; the primary supply connects to  $V_{CC}$  and a backup supply connects to  $V_{BATD}$ .

#### **DS2404 BLOCK DIAGRAM Figure 1**



#### **COMMUNICATION PORTS**

Two communication ports are provided, a 1–wire and a 3–wire port. The advantages of using the 1–wire port are as follows: 1) provides access to the 64–bit lasered ROM, 2) consists of a single communication signal (I/O), and 3) multiple devices may be connected to the 1–wire bus. The 1–wire bus has a maximum data rate of 16.6K bits/second and requires one  $5 \text{K}\Omega$  external pullup.

The 3-wire port consists of three signals, RST, CLK, and DQ. RST is an enable input, DQ is bidirectional serial

data, and the CLK input is used to clock in or out the serial data. The advantages of using the 3-wire port are 1) high data transfer rate (2 MHz), 2) simple timing, and 3) no external pull-up required.

Port selection is accomplished on a first-come, first-serve basis. Whichever port comes out of reset first will obtain control. For the 3-wire port, this is done by bringing RST high. For the 1-wire port, this is done on the first falling edge of I/O after the reset and presence pulses. (See "1-Wire Signalling" section.)

#### PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O,  $\overline{RST}$ , or  $V_{CC}$  pins are high. When using the 1-wire port in battery operate mode,  $\overline{RST}$  and  $V_{CC}$  provide no power since they are low. However, I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off these pins, battery power is conserved and 2) the ROM may be read in absence of normal power. For instance, in battery-operate mode, if the battery fails, the ROM may still be read normally.

In battery-backed mode, if  $V_{CC}$  fails, the port switches in the battery but inhibits communication. In order to read the ROM, the parasite-powered circuitry must be allowed to power down. This may be done by insuring that I/O,  $\overline{RST}$ , and  $V_{CC}$  are all low for  $\gg 1$  s. The ROM may then be read normally over the 1-wire port.

#### 64-BIT LASERED ROM

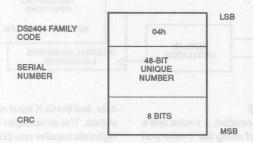
Each DS2404 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code

(DS2404 code is 04h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

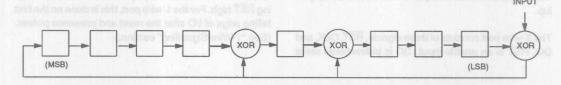
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is  $X^8 + X^5 + X^4 + 1$ . Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

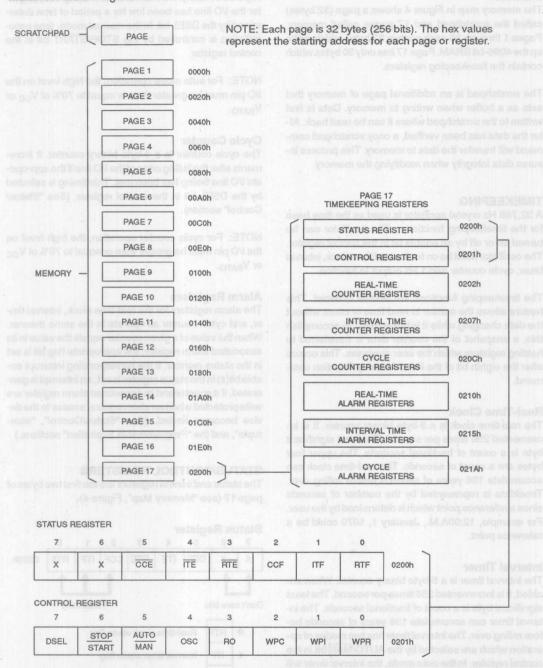
## **64-BIT LASERED ROM Figure 2**



## 1-WIRE CRC CODE Figure 3



# **MEMORY MAP** Figure 4



#### **MEMORY**

The memory map in Figure 4 shows a page (32 bytes) called the scratchpad and 17 pages called memory. Pages 1 through 16 each contain 32 bytes which make up the 4096-bit SRAM. Page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page of memory that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

#### **TIMEKEEPING**

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

#### **Real-Time Clock**

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

#### **Interval Timer**

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/MAN bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control

register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/START bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 70% of  $V_{\rm CC}$  or  $V_{\rm BATO}$ .

#### **Cycle Counter**

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 70% of  $V_{CC}$  or  $V_{BATO}$ .

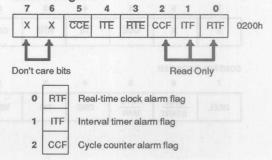
#### **Alarm Registers**

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

#### STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

# Status Register



When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3 RTE Real-time interrupt enable
4 ITE Interval timer interrupt enable
5 CCE Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

1

# **Control Register**

2 WPC

5

D	SEL	ST	OP ART	AUTO MAN.	osc	RO	WPC	WPI	WPR	0201h
0	WF	PR		te protec						S
1	WF	P	Writ	te protec	ct inter	valt	imer/al	arm re	gisters	

4 3 2

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

Write protect cycle counter/alarm registers

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS2404 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/START bit.



If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is  $123\pm2$  ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is  $3.5\pm0.5$  ms.

#### MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. Two examples follow the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

# **ADDRESS REGISTERS** Figure 5

e (Lescus, te se mune varione) • Unio Uni is set to a logic	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	Т7	Т6	T5	T4	ТЗ	T2	T1	ТО
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	Т9	Т8
ENDING ADDRESS WITH DATA STATUS (E/S)	AA	OF	PF	E4	E3	E2	E1	EO

# Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

## Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

#### Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained

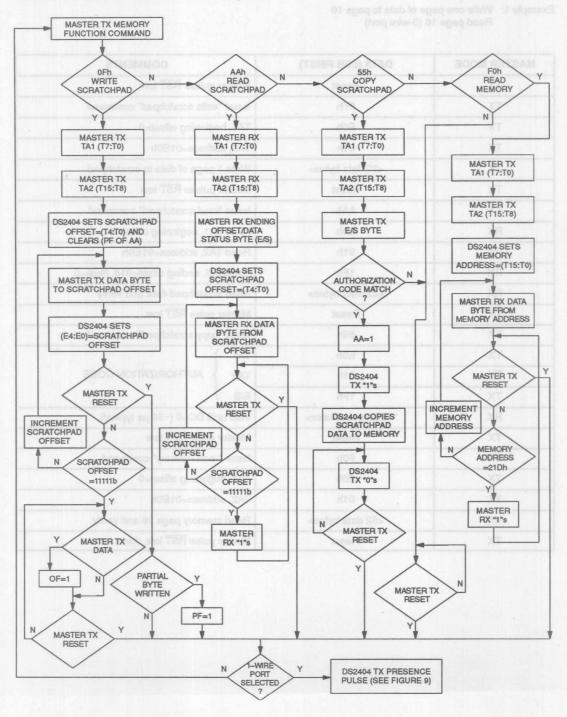
in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. At this point, the part will go into a  $T_X$  mode, transmitting a logic 1 to indicate the copy is in progress. A logic 0 will be transmitted after the data has been copied. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30  $\mu$ s.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

#### Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of page 17. After the end of page 17, logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

# **MEMORY FUNCTION FLOW CHART** Figure 6



# **MEMORY FUNCTION EXAMPLES**

Example 1: Write one page of data to page 16 Read page 16 (3-wire port)

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
TX	Reset	Master pulses RST low	
TX	0Fh	Issue "write scratchpad" command	
TX	E0h	TA1, beginning offset=0	
TX	01h	TA2, address=01E0h	
TX	<32 data bytes>	Write 1 page of data to scratchpad	
TX	Reset	Master pulses RST low	
TX	AAh	Issue "read scratchpad" command	
RX	E0h	Read TA1, beginning offset=0	
RX	01h	Read TA2, address=01E0h	
RX	1Fh	Read E/S, ending offset=31d, flags=0	
RX	<32 data bytes>	Read scratchpad data and verify	
TX	Reset	Master pulse RST low	
TX	55h	Issue "copy scratchpad" command	
TX	E0h	TA1	
TX	01h	TA2 AUTHORIZATION CODE	
TX	1Fh	E/S XTETTAM	
RX	<busy indicator=""></busy>	Wait until DQ=0 (~30 µs typical)	
TX	Reset	Master pulse RST low	
TX	F0h	Issue "read memory" command	
TX	E0h	TA1, beginning offset=0	
TX	01h	TA2, address=01E0h	
RX	<32 data bytes>	Read memory page 16 and verify	
TX	Reset	Master pulse RST low, done	

6

Example 2: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory (1-wire port).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 μs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	OR add to a OOh	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
BX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX osc	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 ) ."O" oigot a of bearo
TX	00h	TA2 AUTHORIZATION CODE
TX	07h	E/S el y le a seri dell'il metays a el aud adw-f
RX	<busy indicator=""></busy>	Wait until 0
TX made and a	Reset Reset	Reset pulse and hymnolisi no addressing 1001
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX of wolder	aud en la company de la compan	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

# WRITE PROTECT/PROGRAMMABLE EXPIRATION

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS2404 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protects their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

## WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR	Interval Timer Interval Time Alarm WPR	Cycle Counter Cyclé Counter Alarm WPR
ythey bas stob t	WPI WPC RO	WPI WPC RO	WPI WPC RO
	OSC*	OSC* STOP/START** AUTO/MAN	OSC* DSEL

<sup>\*</sup> Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".

#### 1-WIRE BUS SYSTEM

The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS2404 behaves as a slave. The exception is when the DS2404 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

#### HARDWARE CONFIGURATION

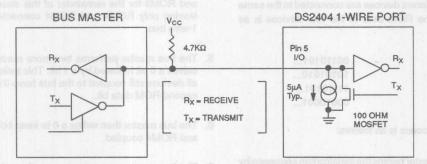
The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it

at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS2404 (I/O pin 5) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus requires a pull-up resistor of approximately  $5K\Omega$ 

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480  $\mu$ S, all components on the bus will be reset.

<sup>\*\*</sup> Forced to a logic "0".

# **HARDWARE CONFIGURATION Figure 8**



#### TRANSACTION SEQUENCE

The protocol for accessing the DS2404 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

#### INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2404 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

#### **ROM FUNCTION COMMANDS**

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

#### Read ROM [33h]

This command allows the bus master to read the DS2404's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2404 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

## Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2404 on a multidrop bus. Only the DS2404 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

## Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

#### Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

#### **Example of a ROM Search**

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

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The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101
ROM2	10101010
ROM3	11110101
ROM4	00010001

The search process is as follows:

- The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
- The bus master will then issue the search ROM command on the 1-wire bus.
- 3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

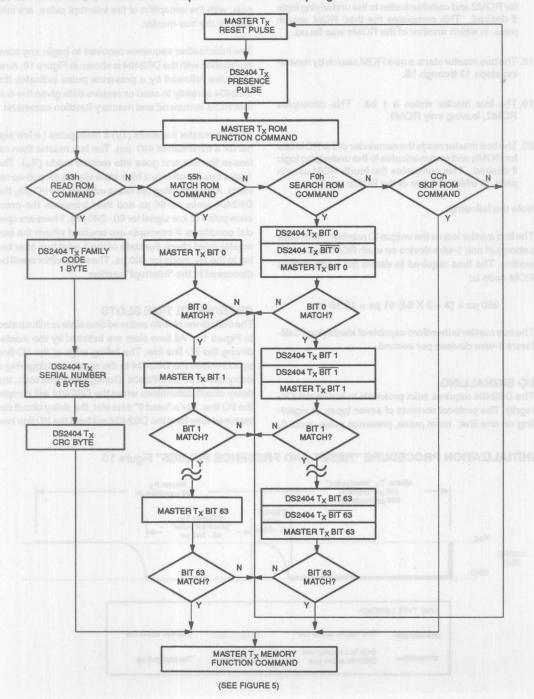
The data obtained from the two reads of the 3-step routine have the following interpretations:

- There are still devices attached which have conflicting bits in this position.
- All devices still coupled have a 0 bit in this bit position.
- All devices still coupled have a 1 bit in this bit position.
- 11 There are no devices attached to the 1-wire bus

- The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
- The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
- The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
- The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
- The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
- The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.
- 10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
- 11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
- 12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
- 13. The bus master starts a new ROM search by repeating steps 1 through 3.
- 14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
- 15. The bus master executes two read time slots and receives two zeros.
- 16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

# 6

# ROM FUNCTIONS FLOW CHART (1-WIRE PORT ONLY) Figure 9



- 17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.
- The bus master starts a new ROM search by repeating steps 13 through 15.
- 19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
- 20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

960 
$$\mu$$
s + (8 + 3 X 64) 61  $\mu$ s = 13.16 ms

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

#### I/O SIGNALLING

The DS2404 requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0,

write 1, read 0, read 1, and interrupt pulse. All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

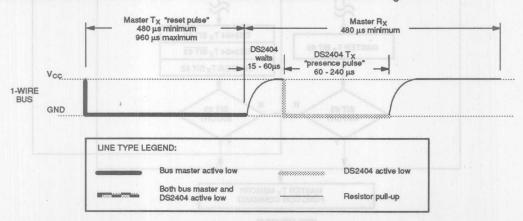
The initialization sequence required to begin any communication with the DS2404 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS2404 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits  $(T_X)$  a reset pulse (a low signal for a minimum of 480  $\mu$ s). The bus master then releases the line and goes into receive mode  $(R_X)$ . The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS2404 waits 15-60  $\mu$ s and then transmits the presence pulse (a low signal for 60 - 240  $\mu$ s). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the  $R_X$  mode for 480  $\mu$ s. These conditions will be discussed in the "Interrupt" section.

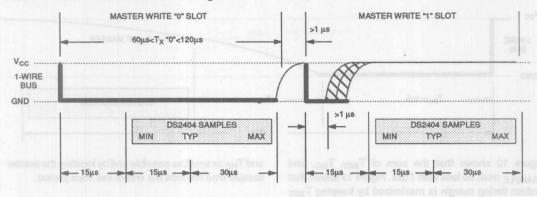
#### **READ/WRITE TIME SLOTS**

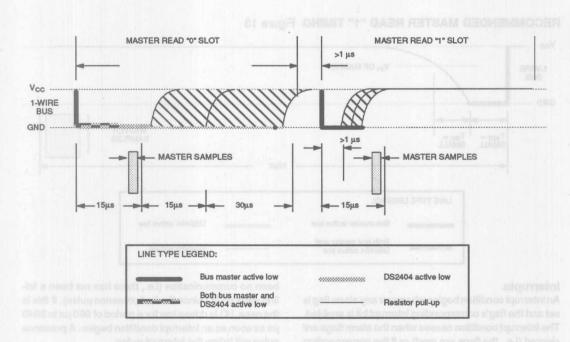
The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS2404 to the master by triggering a delay circuit in the DS2404. During write time slots, the delay circuit determines when the DS2404 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS2404 will hold the I/O line low.

#### INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



# **READ/WRITE TIMING DIAGRAM** Figure 11





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## **DETAILED MASTER READ "1" TIMING Figure 12**

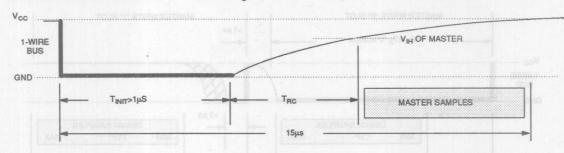
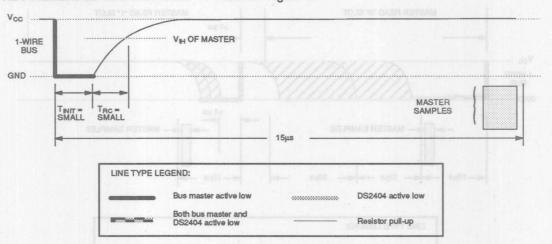


Figure 12 shows that the sum of  $T_{INIT}$ ,  $T_{RC}$ , and  $T_{SAMPLE}$  must be less than 15 $\mu$ s. Figure 13 shows that system timing margin is maximized by keeping  $T_{INIT}$ 

and  $T_{RC}$  as small as possible and by locating the master sample time towards the end of the 15 $\mu$ s period.

# **RECOMMENDED MASTER READ "1" TIMING Figure 13**



#### Interrupts

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled. An interrupt condition may be detected on either the  $\overline{\rm IRQ}$  pin or the I/O pin. During the interrupt condition, the open-drain  $\overline{\rm IRQ}$  pin is driven low and held low until the interrupt condition ceases.

On the 1-wire port, the part responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 14) occurs only when I/O is high and there has

been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960  $\mu s$  to 3840  $\mu s$  as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

A type 2 interrupt (Figure 17) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960  $\mu s$  to 4800  $\mu s$ . A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

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NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

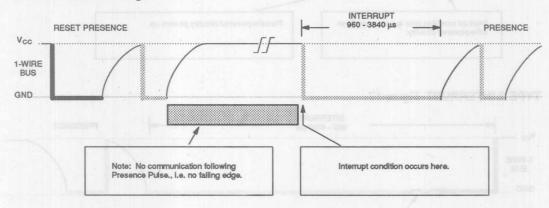
Special cases exist as follows:

Special Case A (Figure 15): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be

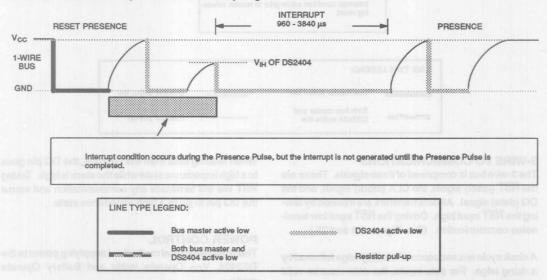
postponed until the presence pulse is over and I/O is a logic 1.

Special Case B (Figure 16): If an interrupt condition exists while the parasite-powered circuitry is powered down (i.e., I/O, RST, and V<sub>CC</sub> have been low for ≫1s), a type 1 interrupt will occur after the first presence pulse following I/O going high, just as in Special Case A.

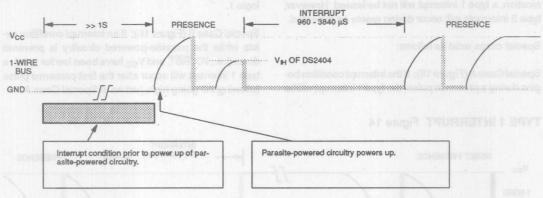
**TYPE 1 INTERRUPT** Figure 14



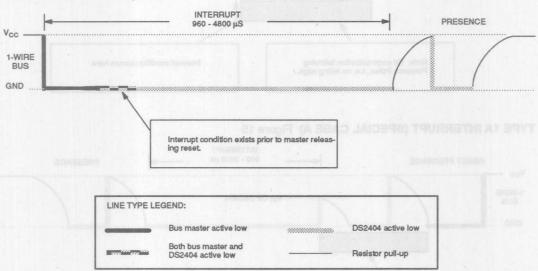
# TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15



# TYPE 1B INTERRUPT (SPECIAL CASE B) Figure 16



# **TYPE 2 INTERRUPT** Figure 17



#### 3-WIRE I/O COMMUNICATIONS

The 3-wire bus is comprised of three signals. These are the  $\overline{RST}$  (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the  $\overline{RST}$  input high. Driving the  $\overline{RST}$  input low terminates communication. (See Figures 24 and 25.)

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. When reading data from the DS2404, the DQ pin goes to a high impedance state while the clock is high. Taking RST low will terminate any communication and cause the DQ pin to go to a high impedance state.

#### POWER CONTROL

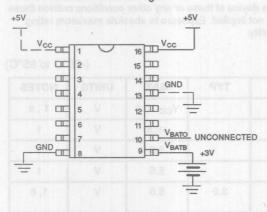
There are two typical methods of supplying power to the DS2404,  $V_{CC}$  Operate mode and Battery Operate mode.

6

V<sub>CC</sub> Operate Mode (Battery Backed)

Figure 18 shows the necessary connections for operating the DS2404 in V<sub>CC</sub> Operate mode.

## VCC OPERATE MODE Figure 18



 V<sub>CC</sub>
 Pin 1 & 16
 2.8 to 5.5 volts

 V<sub>BATB</sub>
 Pin 9
 2.8 to 5.5 volts\*

 V<sub>BATO</sub>
 Pin 10
 must be unconnected

\*While  $V_{BATB}$  may range from 2.8 to 5.5V, if the voltage on  $V_{BATB}$  ever exceeds the voltage on  $V_{CC}$ , the DS2404 will retain data, but will not allow access through the 1- or 3-wire port.

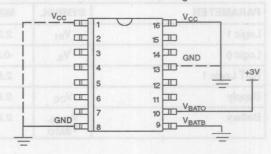
The  $V_{BATB}$  pin is normally connected to any standard 3-volt lithium cell or other energy source. As  $V_{CC}$  falls below  $V_{BATB}$ , the power switching circuit allows  $V_{BATB}$  to provide energy for maintaining clock functionality and data retention. No communication can take place while  $V_{BATB}$  is greater than  $V_{CC}$ . During power-up, when  $V_{CC}$ 

rises above V<sub>BATB</sub> (~200 mV), the power switching circuit connects V<sub>CC</sub> and disconnects V<sub>BATB</sub>. If the oscillator is on, no communication can take place until V<sub>CC</sub> has stayed (~200 mV) above V<sub>BATB</sub> for 123  $\pm$  2 ms.

**Battery Operate Mode** 

Figure 19 shows the necessary connections for operating the DS2404 in Battery Operate mode.

# **BATTERY OPERATE MODE** Figure 19



 V<sub>CC</sub>
 Pin 1 & 16
 Ground

 V<sub>BATB</sub>
 Pin 9
 Ground

 V<sub>BATO</sub>
 Pin 10
 2.8 to 5.5 volts

The V<sub>BATO</sub> pin is normally connected to any standard 3-volt lithium cell or other energy source. Battery Operate mode provides low power consumption when used in conjunction with 1-wire interface.

Note: If the the 3-wire interface is used in Battery Operate mode, the voltage on DQ must never exceed the voltage on V<sub>BATO</sub>.

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to +7.0V -20°C to 85°C -55°C to +125°C 260°C for 10 seconds

#### RECOMMENDED DC OPERATING CONDITIONS

(-20°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.2	1	V <sub>CC</sub> +0.3	V	1,9
Logic 0	V <sub>IL</sub>	-0.3	eroritaturorian	+0.8	V	1
RST Logic 1		2.8	VE+	5.5	V	01
Supply	V <sub>CC</sub>	2.8		5.5	٧	1
Battery	V <sub>BATB</sub> , V <sub>BATO</sub>	2.8	3.0	5.5	٧	1,6

### DC ELECTRICAL CHARACTERISTICS

 $(-20^{\circ}\text{C to }85^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	ILO	ASV AS	AESU entros	/ rao e 1 = 100V	μА	ENS STABLE
Output Current @ 2.4V	Іон	py-8-1			mA	Jug and
Output Current @ 0.4V	loL	( 0.2) ye ni h	Laborator alice a	1	mA	
RST Resistance to Ground	Z <sub>RST</sub>	40	65	90	ΚΩ	muldil to
D/Q Resistance to Ground	Z <sub>DQ</sub>	40	65	90	ΚΩ	STABY WO
CLK Resistance to Ground	Z <sub>CLK</sub>	40	65	90	ΚΩ	a retention
Active Current	I <sub>CC1</sub>	Q	V nadw ,qu-1	2	mA	5
Standby Current	I <sub>CC2</sub>			500	μА	
I/O Operate Charge	Q <sub>BATO</sub>			200	nC	10
Batt Current (OSC On)	I <sub>BAT1</sub>			350	nA	7
Batt Current (OSC Off)	I <sub>BAT2</sub>			200	nA	7

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			10	pF	
Output Capacitance	C <sub>OUT</sub>			15	pF	
I/O (1-Wire)	C <sub>IN/OUT</sub>			800	pF	8

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# AC ELECTRICAL CHARACTERISTICS: 3-WIRE INTERFACE (-20°C to 85°C, V<sub>GC</sub> = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	gas traditional	EN UT BEW	ns	2
CLK to Data Hold	<sup>t</sup> CDH	40			ns	2
CLK to Data Delay	tcod			100	ns	2,3,4
CLK Low Time	t <sub>CL</sub>	250			ns	2
CLK High Time	tсн	250	abuta milita	of antonion flor	ns	2
CLK Frequency	tclk	DC	udu De des	2.0	MHz	2
CLK Rise & Fall	t <sub>R</sub> ,t <sub>F</sub>	d, the parest	allqqs nsed	500	ns	2
RST to CLK Setup	tcc	1			μѕ	2
CLK to RST Hold	t <sub>CCH</sub>	40	ATT ASSESSED THE	REGISTER SOFT OF STATE	ns	2
RST Inactive Time	t <sub>CWH</sub>	250	1/0,8.fa (an	yd 28 lin) bi	ns	2
RST to I/O High Z	t <sub>CDZ</sub>			50	ns	2

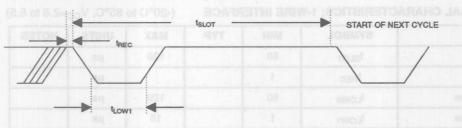
# AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (-20°C to 85°C, V<sub>CC</sub>=2.8 to 5.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	tslot	60		120	μѕ	1111
Recovery Time	tREC	1		1	μѕ	1777
Write 0 Low Time	t <sub>LOW0</sub>	60		120	μs	
Write 1 Low Time	t <sub>LOW1</sub>	1		15	μѕ	1 3 11
Read Data Valid	t <sub>RDV</sub>			15	μs	
Interrupt	t <sub>INT</sub>	960	T Figure 2	4800	μѕ	HW BRIN
Reset Time High	t <sub>RSTH</sub>	480	and the same		μѕ	
Reset Time Low	t <sub>RSTL</sub>	480		960	μѕ	-
Presence Detect High	t <sub>PDHIGH</sub>	15		60	μѕ	100
Presence Detect Low	tppLow	60		240	μs	1777

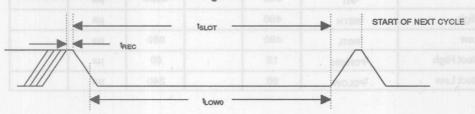
## NOTES - - V 0 28 of 0 005

- 1. All voltages are referenced to ground.
- 2.  $V_{IH} = 2.0 \text{V}$  or  $V_{IL} = 0.8 \text{V}$  with 10 ns maximum rise and fall time.
- 3.  $V_{OH} = 2.4V$  and  $V_{OL} = 0.4V$ .
- 4. Load capacitance = 50 pF.
- 5. Measured with outputs open.
- 6. When battery is applied to VBATO input, VCC and VBATB must be 0V.
- 7. VBATB, or VBATO = 3.0V; all inputs inactive state.
- Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V<sub>CC</sub>, 5 μs after power has been applied, the parasite capacitance will not affect normal communications
- For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V<sub>CC</sub> or V<sub>BATO</sub>.
- 10. Read or write scratchpad (all 32 bytes) at 3.0V.

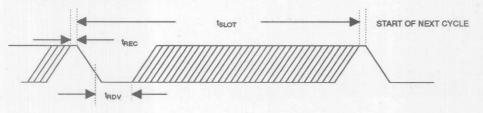
# 1-WIRE WRITE ONE TIME SLOT Figure 20



# 1-WIRE WRITE ZERO TIME SLOT Figure 21

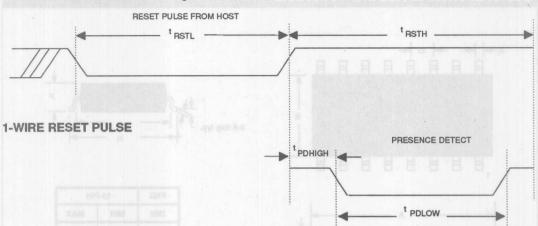


# 1-WIRE READ ZERO TIME SLOTS Figure 22

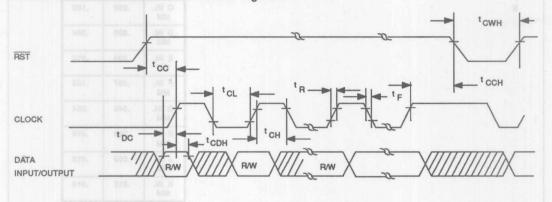


# 6

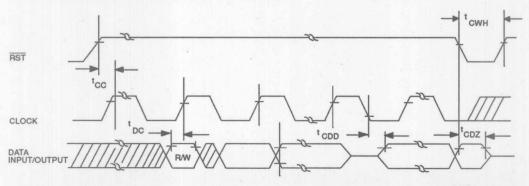
# 1-WIRE PRESENCE DETECT Figure 23

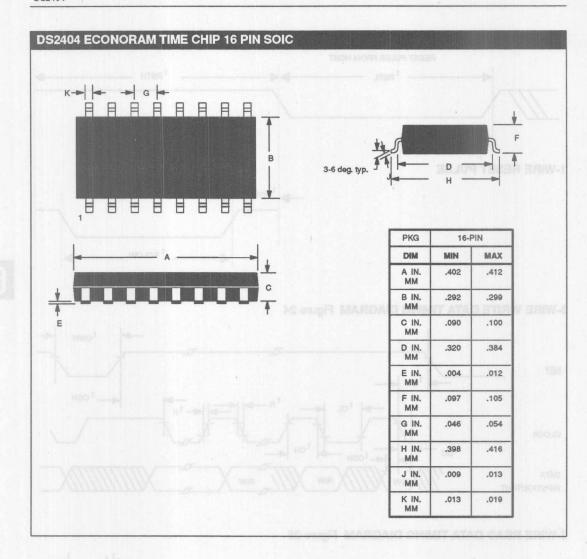


# 3-WIRE WRITE DATA TIMING DIAGRAM Figure 24



# 3-WIRE READ DATA TIMING DIAGRAM Figure 25





7

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

# **User-Insertable Memory**

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

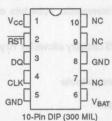
# **DALLAS**SEMICONDUCTOR

## DS1200 Serial RAM Chip

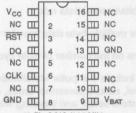
### **FEATURES**

- 1024 bits of read/write memory
- Low data retention current for battery backup applications
- · 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- · No restrictions on the number of write cycles
- Low-power CMOS circuitry
- Applications include:
  - software authorization
  - computer identification
  - system access control
  - secure personnel areas
  - calibration
  - automatic system setup
  - traveling work record

### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 1



16-Pin SOIC (300 MIL) See Mech. Drawing - Sect. 16, Pg. 6

### PIN DESCRIPTION

V<sub>CC</sub> -+5 Volts RST - RESET

DQ - Data Input/Output

CLK - Clock
GND - Ground

V<sub>BAT</sub> - Battery (+)
NC - No Connection

### DESCRIPTION

The DS1200 Serial RAM Chip is a miniature read/write memory which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, RST, and DATA INPUT/OUTPUT.

Nonvolatility can be achieved by connecting a battery of 2 to 4 volts at the battery input  $V_{BAT}$ . A load of 0.5  $\mu$ A

should be used to size the external battery for the required data retention time. If nonvolatility is not required the  $V_{BAT}$  pin should be grounded.

For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than  $V_{BAT}$ , see the DS1201 Electronic Tag 1024-Bit data sheet.

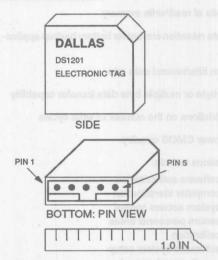


### DS1201 Electronic Tag

### **FEATURES**

- User-insertable, nonvolatile 1024 bits of read/write memory
- Low-power CMOS circuitry allows for 10 years of data retention
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- · Four million bits/second data rate
- Single-byte or multiple-byte data transfer capability
- No restrictions on the number of write cycles
- Applications include computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record.

### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 12

### PIN DESCRIPTION

Pin 1 Vcc +5 Volts
Pin 2 RST RESET

Pin 3 DQ Data Input/Output

Pin 4 CLK Clock Pin 5 GND Ground

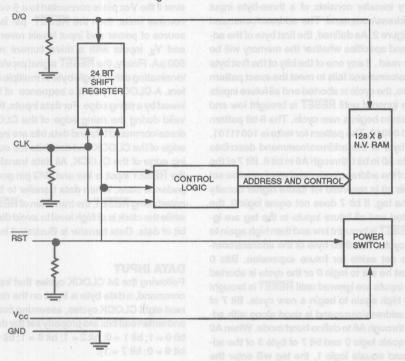
### DESCRIPTION

The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK,

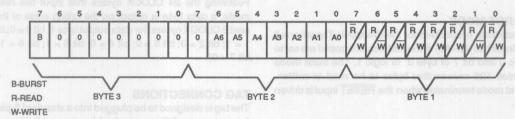
RESET, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

# 7

### **ELECTRONIC TAG BLOCK DIAGRAM Figure 1**



### **ADDRESS/COMMAND** Figure 2



### **OPERATION**

The block diagram (Figure 1) of the Electronic Tag illustrates the main elements of the device: shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle RESET is taken high and 24 bits are loaded into the shift register, providing both address and command information. Each bit is input serially on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read or input

data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hardwired applications, active power is supplied by the Vcc pin. Alternatively, for user-insertable applications, power can be supplied by the RESET pin.

### ADDRESS/COMMAND

Each memory transfer consists of a three-byte input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until RESET is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logic 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logic 0, the cycle is aborted and all future inputs to the tag are ignored until RESET is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logic 0 or the cycle is aborted and all future inputs are ignored until RESET is brought low and then high again to begin a new cycle. Bit 7 of byte 3 of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logic 0 and bit 7 of byte 3 of the address command equals logic 1, the tag will enter the burst mode after the address/command sequence is complete.

### **BURST MODE**

Burst mode is specified for the Electronic Tag when all address bits (A0-A6) of the address/command are set to logic 0 and bit 7 of byte 3 to logic 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the RESET input is driven low.

### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RESET input high. The RESET input serves three functions. First, RESET turns on the control logic which allows access to the shift register for the address/command sequence. Second, the RESET signal provides a power source for the cycle to follow. To meet this requirement, a drive

source for RESET of 2 mA @ 3.8 volts is required. However if the Vcc pin is connected to a 5-volt source within nominal limits, then the RESET pin is not used as a source of power and input levels revert to normal VIH and VII inputs with a drive current requirement of 500 μA. Finally, the RESET signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the RESET input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using RESET, the transition of RESET must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

### **DATA INPUT**

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next eight CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

### DATA OUTPUT

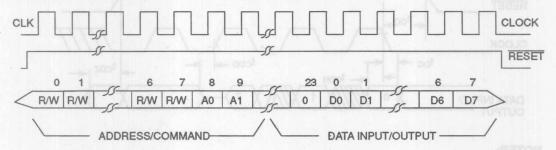
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

### TAG CONNECTIONS

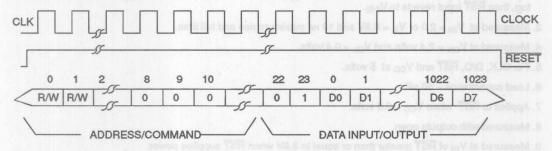
The tag is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to ensure connection integrity before data transfer begins. CLOCK, RESET, and DATA INPUT/OUTPUT all have internal 40K ohm pulldown resistors to ground which can be sensed by a reading device.

### **DATA TRANSFER** Figure 3

### SINGLE BYTE TRANSFER



### **BURST MODE TRANSFER**

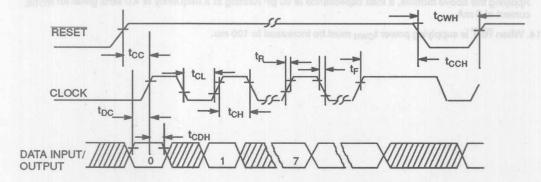


### NOTES

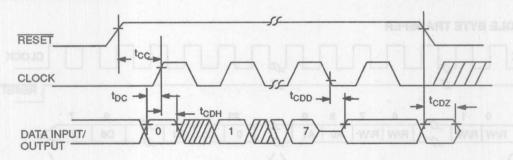
- 1. Data input sampled on rising edge of clock cycle.
- 2. Data output changes on falling edge of clock.

### **READ/WRITE DATA TRANSFER Figure 4**

### **WRITE DATA TRANSFER**



### READ DATA TRANSFER



### NOTES:

- 1. All voltages and resistances are referenced to ground.
- Input levels apply to CLK, D/Q, and RST while V<sub>CC</sub> is within nominal limits. When V<sub>CC</sub> is not connected to the tag, then RST input reverts to V<sub>IHF</sub>.
- 3. Measured at  $V_{IH} = 2.0$  or  $V_{IL} = 0.8V$  and 10 ns maximum rise and fall time.
- 4. Measured at VOH = 2.4 volts and VOI = 0.4 volts.
- 5. For CLK, D/Q, RST and Vcc at 5 volts.
- 6. Load capacitance = 50 pF.
- 7. Applies to RST when V<sub>CC</sub> < 3.8 volts.
- 8. Measured with outputs open.
- 9. Measured at VIH of RST greater than or equal to 3.8V when RST supplies power.
- 10. Logic 1 maximum is  $V_{CC}$  + 0.3V if the  $V_{CC}$  pin supplies power and  $\overline{RST}$  +0.3V if the  $\overline{RST}$  pin supplies power.
- 11. RST logic 1 maximum is V<sub>CC</sub> + 0.3V if the V<sub>cc</sub> pin supplies power and 5.5V maximum if RST supplies power.
- 12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected to the date of manufacture.
- 13. Average AC RST current can be determined using the following formula:

I<sub>TOTAL</sub> = 2 + I<sub>LOAD DC</sub> +(4 X 10-3)(CL + 140)f

ITOTAL and ILOAD are in mA; CL is in pF; f is in MHz.

Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I<sub>TOTAL</sub> current of 5 mA.

14. When RST is supplying power town must be increased to 100 ms.

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### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground
-1.0 to +7.0V
Operating Temperature
O°C to 70°C
Storage Temperature
-40°C to +70°C

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0			V	1,2,10
Logic 0	VIL	-0.3		0.8	V	1
RESET Logic 1	VIHE	3.8			V	1,7,11
Supply	Vcc	4.5	5.0	5.5	V	1

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IL.			+500	μА	5
Output Leakage	ILO			+500	μА	5
Output Current @ 2.4V	Іон	-1			mA	
Output Current @ 0.4V	l <sub>OL</sub>			+2	mA	
RST Input Resistance	Z <sub>RST</sub>	10		40	K ohms	1
D/Q Input Resistance	Z <sub>DQ</sub>	10		40	K ohms	1
CLK Input Resistance	Z <sub>CLK</sub>	10		40	K ohms	1
Active Current	l <sub>CC1</sub>			. 6	mA	8
Standby Current	I <sub>CC2</sub>	1		2.5	mA	8
RST Current	I <sub>RST</sub>				mA	7,8,13

CAPACITANCE

 $(t_{\Delta} = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	-
Output Capacitance	C <sub>OUT</sub>			7	pF	

### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35			ns	3,9
Data to CLK Hold	t <sub>CDH</sub>	40	dictego largo	beut bes vir	ns	3,9
Data to CLK Delay	tcdd	Son et notte villateiles i	Signature and	125	ns	3,4,6,9
CLK Low Time	tcL	125			ns	3,9
CLK High Time	t <sub>CH</sub>	125		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns	3,9
CLK Frequency	fclk	DC	1	4.0	MHz	3,9
CLK Rise & Fall	t <sub>R</sub> ,t <sub>F</sub>		2017	500	ns	9
RST to CLK Setup	tcc	1			μs	3,9
CLK to RST Hold	t <sub>CCH</sub>	40	19917		ns	3,9
RST Inactive Time	t <sub>CWH</sub>	125	0.0		ns	3,9,14
RST to I/O High Z	t <sub>CDZ</sub>		some	50	ns	3,9
Expected Data Retention Time	t <sub>DR</sub>	10	TOBMA		Years	12



## DS1217A Nonvolatile Read/Write Cartridge

### **FEATURES**

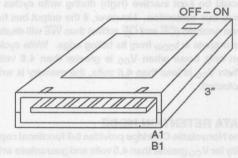
- User-insertable
- Capacity up to 32K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP socket via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

### DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in densities ranging from  $2K \times 8$  to  $32K \times 8$  in 8K byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The

### **PIN ASSIGNMENT**

Name	Posl	tion	Name
Ground	A1 [	B1	No Connect
+5 Volts	A2	B2	Address 14
Write Enable	A3 _	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
Output Enable	A8	B8	Address 3
Address 10	A9	B9	Address 2
Cartridge Enable	A10 _	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground



See Mech. Drawing - Sect. 16, Pg. 14

remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory contents. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory contents.

### READ MODE

The DS1217A executes a read cycle whenever  $\overline{WE}$  (write enable) is inactive (high) and  $\overline{CE}$  (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within  $t_{ACC}$  (access time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (output enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{OE}$  times are not satisfied, then data access must be measured from the latter occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ); the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access. Read cycles can only occur when  $v_{CC}$  is greater than 4.5 volts. When  $v_{CC}$  is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

### WRITE MODE

The DS1217A is in the write mode whenever both the WE and CE signals are in the active (low) state after address inputs are stable. The last falling edge to occur of either CE or WE will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (twn) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in today from its falling edge. Write cycles can only occur when V<sub>CC</sub> is greater than 4.5 volts. When V<sub>CC</sub> is less than 4.5 volts, the memory is write protected.

### **DATA RETENTION MODE**

The Nonvolatile Cartridge provides full functional capability for  $V_{CC}$  greater than 4.5 volts and guarantees write protection for  $V_{CC}$  less than 4.5 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1217A constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data

during power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects the external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that  $V_{CC}$  power is restored to the cartridge, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. For this reason, the cartridge provides battery redundancy. The DS1217A features an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

# REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems that contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and driving circuitry is increased.

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### **CARTRIDGE NUMBERING** Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS		
DS1217A/16K-25	2K x 8	*Address 11, 12, 13, 14	lead Cycle Time	
DS1217A/64K-25	8K x 8	*Address 13, 14	emil seeco	
DS1217A/128K-25	16K x 8	*Address 14	blaV JuguO of 3	
DS1217A/192K-25	24K x 8	00)	blaV luquO of 3	
DS1217A/256K-25	32K x 8	goot evitor	E or CE to Output A	

<sup>\*</sup>Unused address inputs must be held low (VIL).

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Connection Relative to Ground Operating Temperature Storage Temperature

-0.3V to +7.0V 0°C to 70°C -40°C to +70°C

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	Legal stat
Input High Voltage	V <sub>IH</sub>	2.2		Vcc	V	
Input Low Voltage	V <sub>IL</sub>	0.0		+0.8	V	

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CC</sub>=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Leakage Current	IIL	-60		+60	μА	
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	lio	-10		+10	μА	
Output Current @ 2.4V	I <sub>ОН</sub>	-1.0	-2.0		mA	
Output Current @ 0.4V	loL	2.0	3.0		mA	
Standby Current CE=2.2V	I <sub>CCS1</sub>		5.0	10	mA	
Operating Current	I <sub>CCO1</sub>	and the	35	75	mA	

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Capacitance	CIN			75	pF	
Input/Output Capacitance	C <sub>VO</sub>			75	pF	

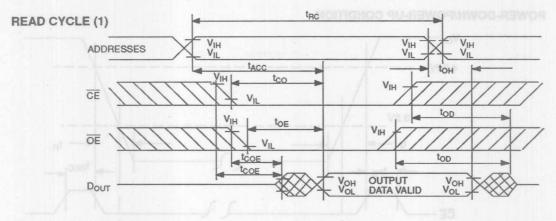
<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

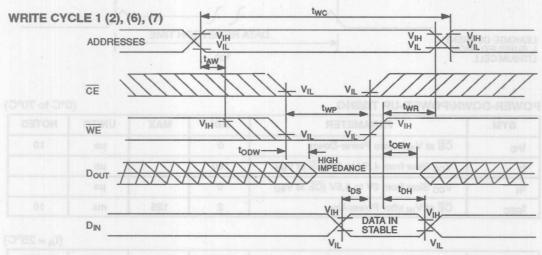
### AC ELECTRICAL CHARACTERISTICS

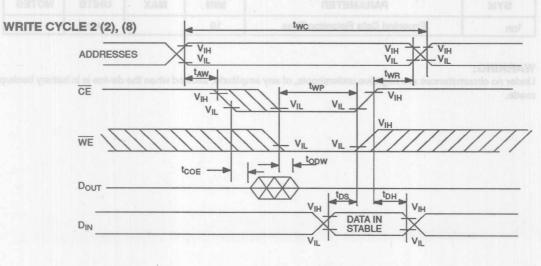
(0°C to 70°C; V<sub>CC</sub>=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Read Cycle Time	t <sub>RC</sub>	250	219		ns	D81217A	
Access Time	tACC	8 x	718	250	ns	DSTRIVA	
OE to Output Valid	t <sub>OE</sub>	8 x	let .	125	ns	D81217A	
CE to Output Valid	tco	8 x	use .	250	ns	DS1217A	
OE or CE to Output Active	t <sub>COE</sub>	5	158		ns	5	
Output High Z from Deselection	t <sub>OD</sub>		( <sub>a</sub> V) wol	125	ns	5	
Output Hold from Address Change	tон	5	*88	MITARI MI	ns	Ln Toss	
Write Cycle Time	two areas	250			ns	T gebere	
Write Pulse Width	t <sub>WP</sub>	170			ns	3	
Address Setup Time	t <sub>AW</sub>	0	enego lenok	and bris vite	ns	is a ci cid	
Write Recovery Time	t <sub>WR</sub>	20	Bouge Bill N	nacinons of	ns	I CONSUME	
Output High Z from WE	topw			100	ns	5	
Output Active from WE	t <sub>OEW</sub>	5	CHOO DE	HAMBEO	ns	5	
Data Setup Time	t <sub>DS</sub>	100	250810		ns	4	
Data Hold Time from WE	t <sub>DH</sub>	20	. 33 <sub>A</sub>		ns	4	

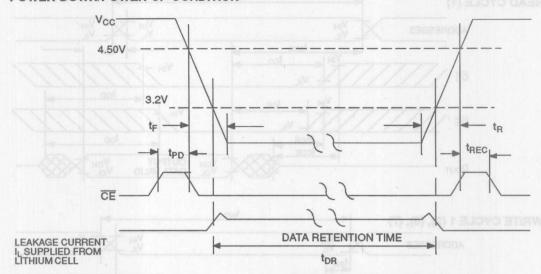
			-







### POWER-DOWN/POWER-UP CONDITION



### POWER-DOWN/POWER-UP TIMING

(0°C to 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES	
t <sub>PD</sub>	CE at V <sub>IH</sub> before Power-Down	0		μs	10	
tF	V <sub>CC</sub> Slew from 4.5V to 0V (CE at V <sub>IH</sub> )	100	77770	μѕ		
t <sub>R</sub>	V <sub>CC</sub> Slew from 0V to 4.5V ( $\overline{\text{CE}}$ at V <sub>IH</sub> )	0	XXXXX	μs		
tREC	REC CE at VIH after Power-Up		125	ms	10	

 $(t_A = 25^{\circ}C)$ 

SYM PARAMETER		MIN	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	10	- (1	years	9

### WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in battery backup mode.

### NOTES:

- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{II}$ . If  $\overline{OE} = V_{IH}$  during the write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- 5. These parameters are sampled with a 5pF load and are not 100% tested.
- 6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remains in a high impedance state during this period.
- Each DS1217A is marked with a 4-digit date code AABB. AA designates the year of manufacture; BB designates the week of manufacture. The expected t<sub>DB</sub> is defined as starting at the date of manufacture.
- 10. Removing and installing the cartridge with power applied may disturb data.

### DC TEST CONDITIONS

Outputs Open t Cycle = 250ns All Voltages Are Referenced to Ground

### **AC TEST CONDITIONS**

Output Load: 100pF + 1TTL Gate Input Pulse Levels: 0 - 3.0V Timing Measurement Reference Levels Input: 1.5 V



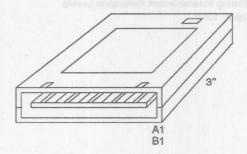
# DS1217M Nonvolatile Read/Write Cartridge

### **FEATURES**

- User-insertable
- Data retention greater than 5 years
- Capacity up to 512K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP via ribbon cable
- Software-controlled banks maintain 32 x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- · Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0 − 70°C

### **PIN ASSIGNMENT**

Name	Posit	lon	Name
Ground	A1 [	☐ B1	No Connect
+5 Volts	A2	B2	Address 14
Write Enable	A3 _	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
Output Enable	A8	B8	Address 3
Address 10	A9	B9	Address 2
Cartridge Enable	A10 _	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground
	-	1	



See Mech. Drawing - Sect. 16, Pg. 14

### DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The Nonvolatile Cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required

for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin bytewide memory sites.

# 7

### READ MODE

The DS1217M executes a read cycle whenever  $\overline{WE}$  (write enable) is inactive (high) and  $\overline{CE}$  (cartridge enable) is active (low). The unique address specified by the address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within  $t_{ACC}$  (access time) after the last address input signal is stable, providing that  $\overline{CE}$  (cartridge enable) and  $\overline{OE}$  (output enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  times are not satisfied, then data access must be measured from the late occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access. Read cycles can only occur when  $v_{CC}$  is greater than 4.5 volts. When  $v_{CC}$  is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

### WRITE MODE

The DS1217M is in the write mode whenever both the WE and CE signals are in the active (low) state after address inputs are stable. The last occurring falling edge of either CE or WE will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (twn) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE and OE active) then WE will disable the outputs in topy from its falling edge. Write cycles can only occur when V<sub>CC</sub> is greater than 4.5 volts. When V<sub>CC</sub> is less than 4.5 volts, the memory is write-protected.

### DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for  $V_{CC}$  greater than 4.5 volts and guarantees write protection for  $V_{CC}$  less than 4.5 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1217M constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects the external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that  $V_{\rm CC}$  power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

### **BANK SWITCHING**

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern which will set the band switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch Chip data sheet for more detail.)

# REMOTE CONNECTION VIA A RIBBON

Existing systems which contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part

Number 499188-4. The 28-pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

### **CARTRIDGE NUMBERING** Table 1

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	offs. When Voo 14 easthan 4.5 volts th
DS1217M 2-25	156K x 8	8
DS1217M 3-25	384K x 8	12
DS1217M 4-25	512K x 8	or weborn extra ert 16 i MVISTOG ert

### **ADDRESS INPUT PATTERN** Table 2

ADDRESS							BI	T SEC	QUEN	CE						
INPUTS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	e wety n	0	inf.it	0	0	0	1,00	to B (	0	nid <sub>O</sub>	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1	1
A10	san (d	0	m1aj	0	0	0	1	110	0	1	0	matai-	:10	offe	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

### **BANK SELECT TABLE** Table 3

BANK		А8 ВП	SEQ	JENCE	
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	n 1es	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1100	0	0	111/2	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0

BANK		А8 ВП	SEQU	JENCE	
BANK 7	1	0	1	1	1
BANK 8	5v10.4	nadi	0	0	0
BANK 9	1	1	0	0	1
BANK 10	00130	pe1 e	0	9148	0
BANK 11	1	1	0	1	1
BANK 12	14.81pt	101108	Vijan	0	0
BANK 13	1	1	1	0	1
BANK 14	1 2 100	110	ong M	F1 and	0
BANK 15	1	1	1	1	1

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Connection Relative to Ground
Operation Temperature
Storage Temperature

-0.3V to + 7.0V 0°C to 70°C -40°C to +70°C

### RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	٧	Julgot Hotel
Input High Voltage	VIH	2.2		Vcc	V	W-0 54-4
Input Low Voltage	VIL	0.0	Harris Harris	+0.8	V	

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	IIL	-60		+60	μА	all such
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-10	waoi	+10	μА	doA Jugtus
Output Current @ 2.4V	loн	-1.0	-2.0		mA	ata Satur
Output Current @ 0.4V	loL	2.0	3.0	IL.	mA	bloH sta
Standby Current CE = 2.2V	I <sub>CCS1</sub>		15	25	mA	
Operating Current	I <sub>CCO1</sub>		50	100	mA	riput Load

### DC TEST CONDITIONS

Outputs Open t Cycle = 250 ns

All Voltages Are Referenced to Ground

### CAPACITANCE

(ta =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			100	pF	
Input/Output Capacitance	C <sub>OUT</sub>			100	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	250		100	ns	stage Ten
Access Time	tACC	reb edt la n	strasco Isaci	250	ns	e o ai airti
OE to Output Valid	toE	I fon ai noifi	oriongs sidt (	125	ns	l betsolbn
CE to Output Valid	tco			210	ns	
OE or CE to Output Active	t <sub>COE</sub>	5	памоэ и	DITARBO	ns	5
Output High Z From Deselection	top	MIM	TORMAS	125	ns	5
Output Hold From Address Change	tон	5	J ooV		ns	Power Su
Read Recovery Time	t <sub>RR</sub>	40	1 107		ns	after a sensite
Write Cycle Time	twc	250	1	1	ns	10-11-10-91
Write Pulse Width	t <sub>WP</sub>	170			ns	3
Address Setup Time	t <sub>AW</sub>	0	COLUMN	PER PROPERTY	ns	Dava.
Write Recovery Time	t <sub>WR</sub>	20	arogna (s)		ns	
Output High Z From WE	topw	40	11	100	ns	5
Output Active From WE	toew	5	OF		ns	5
Data Setup Time	t <sub>DS</sub>	100	loud		ns	10 114 110
Data Hold Time From WE	t <sub>DH</sub>	20			ns	4 0

### **AC TEST CONDITIONS**

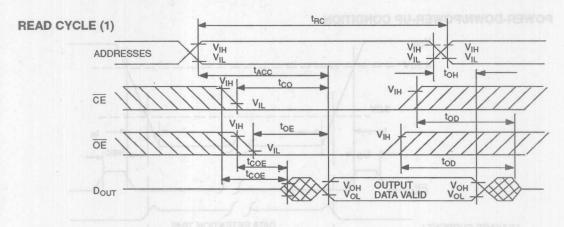
Output Load: 100pF + 1TTL Gate Input Pulse Levels: 0-3.0V

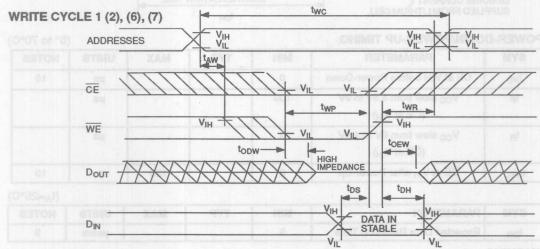
Timing Measurement Reference Levels

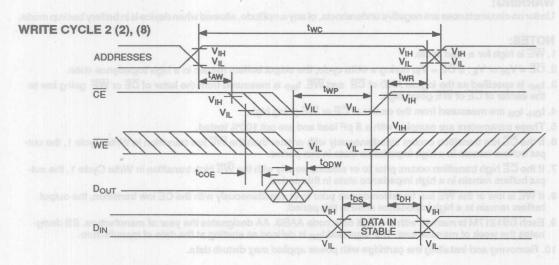
Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

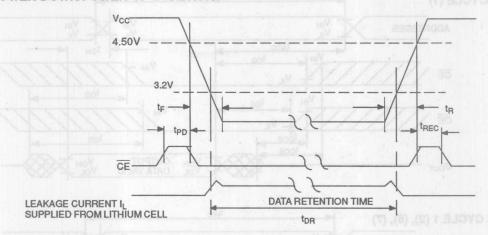
Ag i			







### POWER-DOWN/POWER-UP CONDITION



### POWER-DOWN/POWER-UP TIMING

(0° to 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
tpD	CE at VIH before Power-Down	0	7777	////	μѕ	10
t <sub>F</sub>	V <sub>CC</sub> slew from 4.5V to 0V (CE at V <sub>IH</sub> )	100			μѕ	
t <sub>R</sub>	V <sub>CC</sub> slew from 0V to 4.5V (CE at V <sub>IH</sub> )	0	200		μѕ	
t <sub>REC</sub>	CE at V <sub>IH</sub> after Power-Up	2	XXXX	125	ms	10

(tA=25°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t <sub>DR</sub>	Expected Data Retention Time	5			years	9

### **WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

### NOTES:

- 1. WE is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during a write cycle, the output buffers remain in a high impedance state.
- 3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CE}}$  of  $\overline{\text{WE}}$  going high.
- 4. t<sub>DH</sub>, t<sub>DS</sub> are measured from the earlier of CE or WE going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
- If the CE high transition occurs prior to or simultaneously with the WE high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
- If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state in this period.
- Each DS1217M is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t<sub>DB</sub> is defined as starting at the date of manufacture.
- 10. Removing and installing the cartridge with power applied may disturb data.

### **FEATURES**

- Low-cost, add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 Kbps communication rate
- Up to five Keys and/or Tags resident at one time

# PIN CONNECTIONS AND DEFINITIONS Intermediary Bytewide Socket

Pin 7 - 10 Address Inputs

Pin 11 D0

Pin 20 Conditioned Chip Enable (CE)

Pin 22 Output Enable (OE)

Pin 14 Ground

Pin 28 Vcc

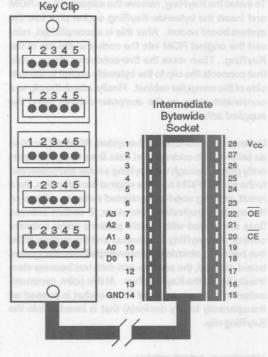
\* All pins pass through except 20

### **Key Clip**

### DESCRIPTION

The DS1250 KeyRing adapts low pin-count Electronic Keys (DS1204U), TimeKeys (DS1207) or Electronic Tags (DS1201) to JEDEC bytewide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28-pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating five-conductor ribbon cable can be routed out of the system enclosure if desired and the clip

### **PIN ASSIGNMENT**



5-Conductor Ribbon Cable

can be attached where convenient with the adhesive provided. Up to five Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit that redirects information flow from the bytewide memory to the inserted keys/tags. A special software-generated address sequence causes the redirection to take place. Typical data transfer rates of 50 Kbps are possible with an assembly language software driver.

# HARDWARE IMPLEMENTATION: 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board that contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM that is used for boot sequences, basic I/O system implementation, EPROM storage, or some form of dedicated software monitor application.

To install the KeyRing, remove the existing 28-pin ROM and insert the bytewide KeyRing socket pins into the system board socket. After this is accomplished, reinsert the original ROM into the socket at the top of the KeyRing. Then route the five-conductor ribbon cable that connects the clip to the bytewide socket to the outside of the computer cabinet. Finally, attach the clip to a convenient place on the computer cabinet using the supplied adhesive.

Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM bus becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) that is inserted into the KeyRing clip.

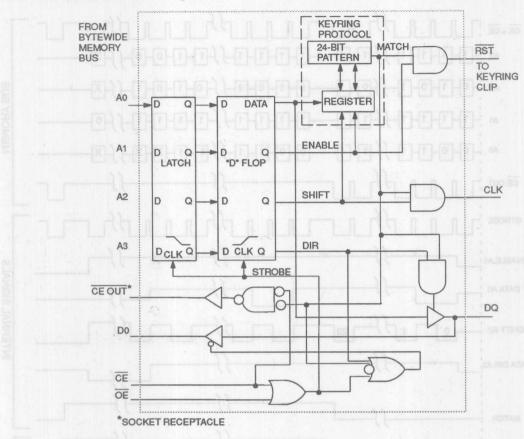
### **KEYRING OPERATION**

The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of  $\overline{CE}$  In and  $\overline{OE}$  In. The  $\overline{CE}$  input is connected to the memory bus  $\overline{CE}$  and the  $\overline{OE}$  input is connected to the memory bus  $\overline{OE}$  input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic that will generate signals for Keys and

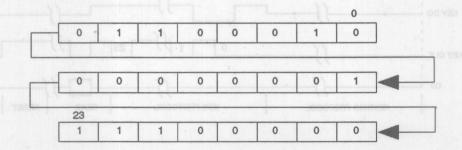
Tags. The KeyRing protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal that activates the communications sequence. A0 defines the data that is compared for recognition. A2 is used to clock in information defined by A0. Initially, the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

Data transfer through the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each rising edge of the strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal that causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the RST signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate that allows Key DQ to drive the D0 line to the memory bus. When RST is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized at the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

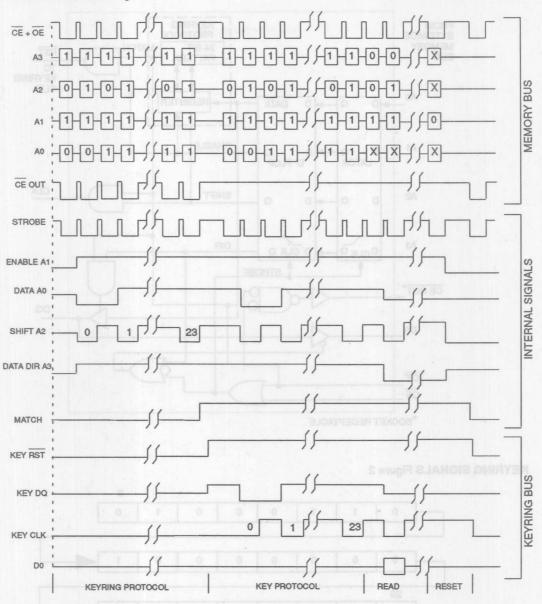
### **KEYRING BLOCK DIAGRAM** Figure 1



# KEYRING SIGNALS Figure 2



### **KEYRING SIGNALS** Figure 3



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature -1.0V to +7.0V 0°C to 70°C -40°C to +70°C

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	٧	1
Logic 0 Input	V <sub>IL</sub>	-0.3	# 1	+0.8	٧	1008)1
Supply	Vcc	4.5	5.0	5.5	V	1

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{CC} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>IL</sub>	-1	140	ты ресовы	μА	DAOG
Output Leakage	lLO			1	μА	
Output Current @ 2.4V	Іон	-1			mA	
Output Current @ 0.4V	loL	+4		. 8.	mA	KEY
RST Output Current @ 3.8V	I <sub>OHR</sub>	16			mA	DIG. F
Supply Current	Icc	No.		6	mA	2

### CAPACITANCE

(ta=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	
Input/Output	C <sub>VO</sub>		5	10	pF	

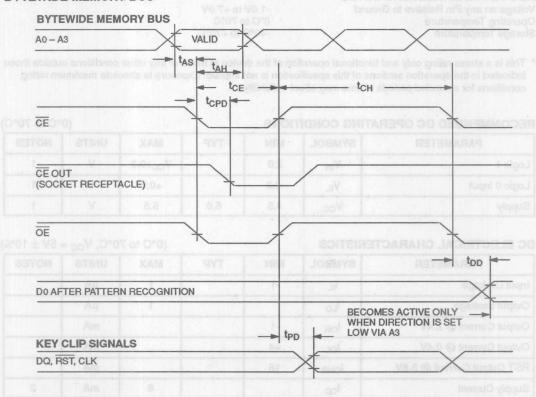
### **AC ELECTRICAL CHARACTERISTICS**

(0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

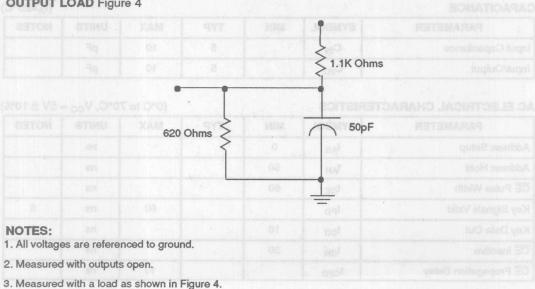
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0	8		ns	
Address Hold	t <sub>AH</sub>	50			ns	
CE Pulse Width	t <sub>CE</sub>	60			ns	
Key Signals Valid	t <sub>PD</sub>			60	ns	3
Key Data Out	t <sub>DD</sub>	10			ns	3
CE Inactive	t <sub>CH</sub>	30	,D	ucilg of best	ns	gisliov IIA
CE Propagation Delay	t <sub>CPD</sub>			10	ns	Mensured

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### **BYTEWIDE MEMORY BUS**



### **OUTPUT LOAD Figure 4**



121891 6/6

# 7

# **DALLAS** SEMICONDUCTOR

# DS1258K-001 CyberCard Portable Data Carrier Evaluation Kit

### **FEATURES**

- Read or write any Cyber Portable Data Carriers with a PC host
- No slot required; connects to parallel printer port
- Normal computer to printer operation unaffected
- Compatible with all desktop PC's having a DIN-5 keyboard connector
- Comes with user-linkable drivers for systems integrators
- Example Intel 8051 (DS5000) Assembly Language program
- Includes:

DS1258Cl Computer Interface
DS1258HI Single Slot User Interface
DS1258J Cyber Power Cable
Floppy Disk Labeled "Cyber EV Kit Disk 1"
Data Book
DS6417 – 256 Cyber Portable Data Carrier

DS6417 - CyberCard User's Guide

# Computer DS1258CI Printer 0.6 m Keyboard Receptacle 5 4 3 2 1

### DESCRIPTION

The DS1258K–001 Cyber Products EV Kit serves as a software reference guide for users who are designing with Dallas Semiconductor Cyber products. This cookbook package allows a user to easily interface Portable Data Carrier Cyber products with an IBM-compatible computer. A software diskette is included which contains a demonstration program written in Pascal. With this cookbook, applications software can be easily developed using higher level languages such as 'C', FORTRAN, etc. Additionally, included on the diskette is a source level listing of a program written in DS5000 As-

sembly Language for reading and writing the various Cyber products.

### INSTRUCTIONS

Install the "Cyber Cookbook Diskette" in the default disk drive and type "CYBERCRD". This command will execute the CyberCard demonstration program. For installation instructions, refer to the CyberCard User's Guide.



# DS1258K-002 CyberKey Carrier Evaluation Kit

### **FEATURES**

- Read or write any CyberKey with a PC host
- No slot required; connects to parallel printer port
- Normal computer to printer operation unaffected
- Compatible with all desktop PC's having a DIN-5 keyboard connector
- Comes with user linkable drivers for systems integraters
- Example Intel 8051 (DS5000) Assembly Language program
- Includes:

DS1258CI Computer Interface
DS1258HI Single Slot User Interface
DS1258J Cyber Power Cable
Floppy Disk Labeled "CyberKey Kit Disk 1"
Data Book
DS6201 – 1K RAM CyberKey
DS6204 – Secure CyberKey

DS6205 – Multi CyberKey DS6207 – Time CyberKey

# Computer DS1258CI Printer 0.6 m Keyboard Receptacle 5 4 3 2 1

### DESCRIPTION

The DS1258K–002 CyberKey EV Kit serves as a software reference guide for users who are designing with the Dallas Semiconductor Cyber products. This cookbook package allows a user to easily interface Cyber-Key products with an IBM compatible computer. A software diskette is included which contains a demonstration program written in Pascal. With this cookbook, applications software can be easily developed using higher level languages such as 'C', FOR-TRAN, etc. Additionally, included on the diskette is a source level listing of a program written in DS5000 Assembly Language for reading and writing the various Cyber products.

### INSTRUCTIONS

Install the "Cyber Cookbook Diskette" in the default disk drive and type "RUN ME". This command will give instructions for printing document files which should be read carefully before proceeding.

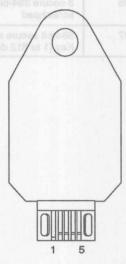
# **DALLAS**SEMICONDUCTOR

DS620x CyberKey

### **FEATURES**

- Greater than 50,000 cycle connector life
- Durable and rugged
- · Ground pin makes first and breaks last
- 3-wire serial interface (DQ, CLK, and RST) simplifies microprocessor interconnect
- Guided entry on mating connector overcomes orientation problems
- Greater than 10 years of data retention with no limitations or restrictions on write cycles
- Low-power CMOS circuitry
- Applications include software authorization, computer identification, system access control, calibration, data storage, automatic system setup, and travelling work record

### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 13

### PIN DESCRIPTION

- 1 Ground
- 2 Clock
- 3 Data
- 4 RST
- 5 V<sub>CC</sub>

### DESCRIPTION

CyberKeys are miniature electronic memories with self-contained lithium energy sources. Depending upon the memory device internal to the CyberKey, secure, non-secure, time-related, and combinations of these functions are available. Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLK (clock), RST (reset), and DQ (data). Low pin count and a guided entry for a mating receptacle overcome mechanical

problems normally encountered when a conventional integrated circuit package is inserted by the end user. CyberKeys are designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years. Small, lightweight construction makes the devices suitable for carrying in a pocket or direct attachment to an object. Figure 1 lists the memory devices utilized in the different CyberKeys. For further information please see the referenced data sheets.

### **CYBERKEY DEVICES** Figure 1

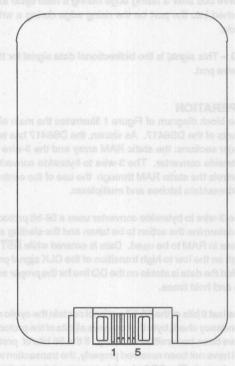
CYBERKEY	DESCRIPTION	RELATED DATA SHEET
DS6200	64-bit unique serial number with CRC Checking	DS2400
DS6201	1024 bits non-secure static RAM	DS1200
DS6204	128-bit secure static RAM: 64-bit password and 64-bit ID	DS1204
DS6205	3 secure 384-bit subkeys, 512-bit scratchpad	DS1205
DS6207	384-bit secure static RAM: Internal Time Key (1 to 512 days)	DS1207

# CyberCard EV 4M-Bit NV SRAM

### **FEATURES**

- Greater than 50,000 insertion connector life
- Durable and rugged
- · Ground pin makes first and breaks last
- User-insertable memory
- Capacities from 256K bits to 4M bits of nonvolatile memory
- Up to 1 million bits per second transfer rate
- Automatic write protection circuitry safeguards against data loss
- Cyclic redundancy check monitors serial data transmission for errors
- Compact size and shape
- Wide operating temperature range of -20°C to +70°C

### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 13

### PIN DESCRIPTION

Pin 1 Ground

Pin 2 Clock

Pin 3 Data

Pin 4 RST

Pin 5 Vcc

### DESCRIPTION

The DS6417 CyberCard EV is a nonvolatile serial access RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 256K bits to 4M bits. Data is transferred to and from the RAM through a standard 3-wire serial interface which is comprised of DQ, RST,

and CLK signals. The serial port requires a 7-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmissions for errors.

### PIN DESCRIPTION OVERVIEW

RST – This pin controls all communication to the DS6417. When this signal is LOW, all communication to the serial port is inhibited. When high, data can be clocked into or out of the serial port.

CLK – This input signal is used to input or extract data from the serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven onto the 3-wire bus after a falling edge during a read cycle and latched into the port on the rising edge during a write cycle.

DQ – This signal is the bidirectional data signal for the 3-wire port.

### **OPERATION**

The block diagram of Figure 1 illustrates the main elements of the DS6417. As shown, the DS6417 has two major sections: the static RAM array and the 3-wire to bytewide converter. The 3-wire to bytewide converter controls the static RAM through the use of the control/address/data latches and multiplexer.

The 3-wire to bytewide converter uses a 56-bit protocol to determine the action to be taken and the starting address in RAM to be used. Data is entered while  $\overline{RST}$  is high on the low to high transition of the CLK signal provided the data is stable on the DQ line for the proper setup and hold times.

The last 8 bits of the 56-bit protocol contain the cyclic redundancy check byte that ensures all bits of the protocol have been transmitted correctly. If the 56 bits of protocol have not been received properly, the transaction will be aborted. The CRC check byte can catch up to three bit errors within the 56-bit protocol and can also be used on incoming and outgoing data streams to check the integrity of the data being read or written.

# PROTOCOL COMMANDS Table 1

### **PROTOCOL**

The 3-wire bus protocol can cause six different actions to be taken by the DS6417 (see Table 1).

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action to be taken involves a read or a write. A read function is defined by the binary pattern [11101000]. This pattern is applicable to commands 1,3,5, and 6 of Table 1. A write function is defined by the binary pattern [00010111]. This pattern is applicable to commands 2 and 4 of Table 1. Any other pattern which is entered into this read/write field will cause the transaction to be terminated. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of protocol referred to as the command field. The command field bits are shown as the binary values in Table 1.

### **BURST READ**

A burst read uses a 19-bit address field which consists of the second byte, third byte, and the first three bits of the fourth byte of the protocol to determine the starting address of the information to be read from the RAM. The byte of data that has been accessed is transferred to the 3-wire bus a bit at a time, LSB first, by driving the DQ line on the falling edge of the next eight clocks.

### **BURST WRITE**

A burst write uses the same 19 bit address field to determine the starting address of information to be written in RAM. Data is shifted from the DQ line into an eight bit shift register on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte by byte basis automatically incrementing the selected address by one location for each successive byte.

- 1) [00110 binary] burst read
- 2) [10001 binary] burst write
- 3) [00101 binary] read protocol select bits
- 4) [01110 binary] write protocol select bits
- 5) [11 XXX binary] burst read masking portions of the protocol select bits
- 6) [00011 binary] read the CRC register

7

Termination of a current transaction will occur at any time the RST signal is taken low. If a byte of data has been loaded into the shift register a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when the RST signal goes low, no writing occurs. Reads can be terminated at any point since there is no potential for the corruption of RAM data.

### READ CRC.

The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the 56-bit protocol. The 8-bit CRC value is valid for both the 56-bit protocol and also all data that is read or written from the RAM. After a burst read or write has finished and RST has gone low, the final value of the CRC is stored in an internal register of the DS6417. If a read CRC register command is issued, the stored CRC value is driven onto the DQ signal line by the first eight clock cycles after the 56-bit protocol is received. The CRC value generated by the DS6417 should match the value generated by the host system which is transmitting or receiving data on the other end of the 3-wire bus.

It should be noted that the CRC for a previous transaction can only be obtained if a read CRC command is issued immediately after the  $\overline{RST}$  signal goes low to reset the DS6417, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever the  $\overline{RST}$  signal goes low again.

Three commands are used to set the select bits in the protocol. Once the select bits are set to a binary value, they must be matched when protocol is sent or further activity is prevented. The bits allow for up to 65,536 different binary combinations. Therefore, multiple DS6417s can be connected on the same 3-wire bus and only the selected device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field. To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have a large number of DS6417s in use and uniquely identify each one. A read can occur successfully without knowing the select bits, but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS6417 in the presence of many DS6417s. A read in the read/ write field and a [11000 binary] in the command field will execute a mask read that ignores all select bits to determine the presence of any DS6417s. With the detection of at least one device, a search can begin by masking all but a single pair of DS6417 select bits. A read in the read/write field and a [11001 binary] in the command field will unmask the first two LSB's of byte 4 of the select bits (Figure 3). With these two select bits unmasked, only an exact match of four possible combinations (00, 01, 10, or 11) of these two select bits will now allow access through the 3-wire port to RAM. Therefore, repeating the unmasking of the two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of the four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will yield an exact match of the one DS6417 out of the possible 65,536 in no more than 32 attempts.

### **CRC GENERATION**

The logic involved in the CRC generation is shown in Figure 4. Basically, the scheme is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQ IN to the CRC generator while each byte is being assembled and at the same time, output data to the output (DQOUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire bus.

The reset signal (RSB) must be high while the CRC generator is being used as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS6417 CRC requirements.

However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Microcontroller. The assembly language procedure DO\_CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to cal-

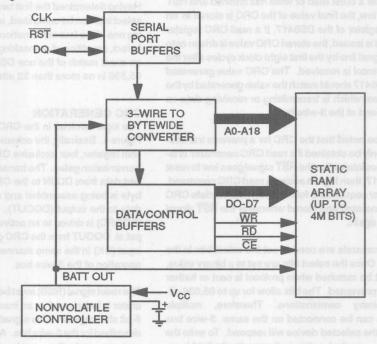
culate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO\_CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

### 3-WIRE BUS

The 3-Wire bus is comprised of three signals. These are the RST (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the RST input high. The RST signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the RST is low and the DQ pin goes to a high impedance state. When data transfers to the DS6417 are terminated by the RST signal going low, the transition of the RST going low must occur during a high level of the CLK signal. Failure to insure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figures 5 and 6 for normal modes of operation.

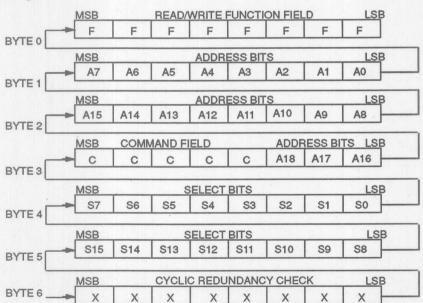
### **BLOCK DIAGRAM** Figure 1



## CRC CODE Table 2

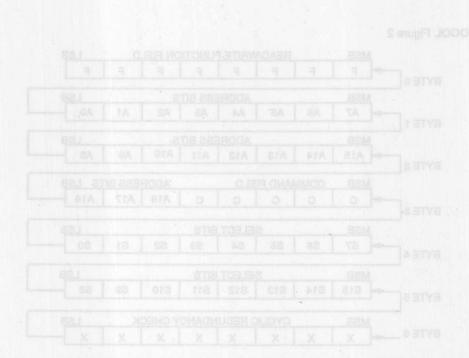
DO_CR	PUSH	ACC		:Save the Accumulator
	PUSH	В		;Save the B register
	PUSH	ACC		;Save bits to be shifted
CRC L	MOV OOP:	В,	#8	;Set to shift eight bits
0 0	XRL	Α,	CRC	;Calculate DQIN xor CRCTO
	RRC	A		:Move it to the last
	MOV	Α,	CRC	:Get the last CRC value
	JNC	ZERO		;Skip if DQIN xor CRCTO=0
110	XBL	A,	0CCH	:Update the CRC value
ZERO:		- even in	Vice and Alexander	
	RRC	Α .		;Position the new CRC
	MOV	CRC,	A A	;Store the new CRC
	POP	ACC		;Get the remaining bits
	RR	A SEED		;Position next bit in LSB
	PUSH	ACC		Save the remaining bits
	DJNZ	B. BEBUS	CRC LOOP	;Repeat for eight bits
	POP	ACC		;Clean up the stack
	POP	B 2 3 8 1 A	UNIMASK	Restore the B register
	POP	ACC		:Restore the Accumulator
	RET	700		Return

## **PROTOCOL** Figure 2

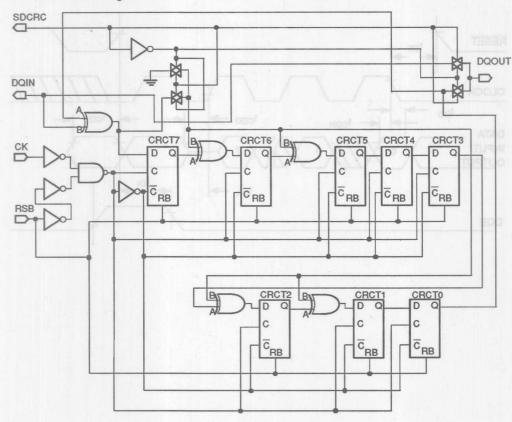


## **SELECT BITS MASK** Figure 3

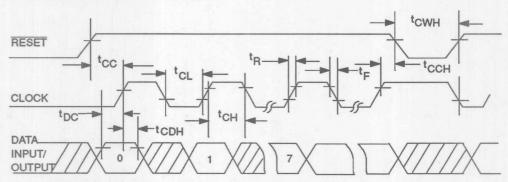
S15 S14 S13 S12 S11 S10 S9 S8	S7	S6	S5	S4	S3	S2	S1	S0	0: PUS			
Dave Its Brigare battiris ed of stid evast							DOA	1	COI	MMA	ND F	IELD
Set to shift eight bile.					A O.V.	A1.1	,8	1	1	X	X	X
Calculate DOIN year DROTO			190		ASK		1		IRX	0	0	0
That off of it evolutions of the second of t			UNN	IASK	2 LS	B'S	- 8		MO	0	0	1
			UNN	IASK	4 LS	B'S	BES		JNC	0	1	0
			UNN	IASK	6 LS	B'S	A		DEF	0	1	1
			UNN	IASK	8 LS	B'S	ORO SSA		YOM	1	0	0
		l	JNM	ASK 1	10 LS	SB'S	A		9B	1	0	1
		ou t	JNM	ASK 1	12 LS	B'S	- <del>, G</del>		►La	1	1	0
		l	JNM	ASK 1	14 LS	B'S	ACC		POP	1	1	1



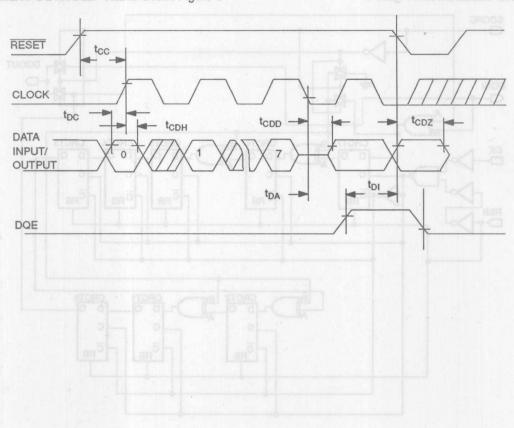
## **CRC GENERATION** Figure 4



## **TIMING DIAGRAM - WRITE DATA Figure 5**



## TIMING DIAGRAM - READ DATA Figure 6



**ABSOLUTE MAXIMUM RATINGS\*** Voltage on any Pin Relative to Ground **Operating Temperature** Storage Temperature

-0.3V to +7.0V 0°C to 70°C -40°C to +70°C

This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	Vcc	-4.5	5.0	5.5	Volts	east Dur
Input High Voltage	V <sub>IH</sub>	2.2	toc	V <sub>CC</sub>	Volts	LID of Tar
Input Low Voltage	V <sub>IL</sub>	0.0	Hoo!	+0.8	Volts	EH alnux

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub>=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>IL</sub>	-60		+60	μА	ERSOLE C
I/O Leakage	ILO	-10		+10	μА	tov AS 6
Output Current	I <sub>ОН</sub>	-1.0	-2.0		mA	2
Output Current	l <sub>OL</sub>	2.0	3.0		mA	3
Operating Current	l <sub>OP</sub>	Çune 7	10	20	mA	G-REWY
Input Capacitance	C <sub>IN</sub>		5		pF	700
I/O Capacitance	C <sub>IB</sub>		5	1	pF	

#### **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CCI</sub> Slew Rate	t <sub>F</sub>	300			μs	4
V <sub>CCI</sub> Slew Rate	t <sub>R</sub>	1			μѕ	4
Power Down to PF	tpF	0			μs	4
PF Recovery	tREC	METENTE	ATTACO	100	μs	4

#### AC ELECTRICAL CHARACTERISTICS

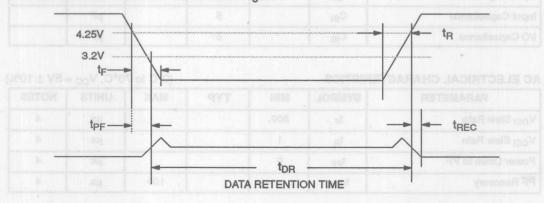
(V<sub>CC</sub>=5V ± 10%, 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	35, 14,		ns	2
Data to CLK Hold	t <sub>CDH</sub>	40	idanego lanci	sty and tune	ns	2
Data to CLK Delay	tcDD	villidailes :	me may affect	125	ns	2,3,5
CLK Low Time	t <sub>CL</sub>	500			ns	2
CLK High Time	t <sub>CH</sub>	500	IN COMDA	UTANE90	ns	2
CLK Frequency	fclk	DC	TORRES	1	MHz	2
CLK Rise & Fall Time	t <sub>R</sub> t <sub>F</sub>	6.4	DOV.	500	ns	CALS JEWIO
RST to CLK Setup	tcc	188	HoV		μѕ	2
CLK to RST Hold	t <sub>CCH</sub>	40	дV		ns	2
RST Inactive Time	tcwH	125			ns	2
RST to D/Q High Z	t <sub>CDZ</sub>		BOTTE	50	ns	2

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. @ 2.4 volts.
- 3. @ 0.4 volts.
- 4. See Figure 7.

### **POWER-DOWN/POWER-UP CONDITION Figure 7**

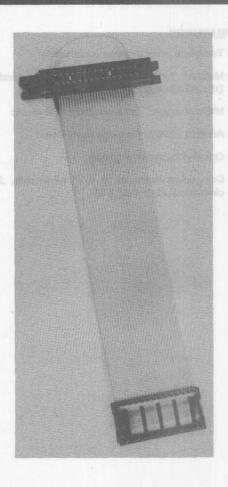


# DALLAS

## DS9000 Bytewide Cable Harness

#### **FEATURES**

- Converts 30-position card edge to popular bytewide 28-pin DIP socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- 28-position DIP plug inserts into any standard 28-position IC DIP socket
- Color stripe indicates pin one on 28-pin DIP plug
- Standard six-inch cable length



#### DESCRIPTION

The DS9000 Bytewide Cable Harness is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges or any other 30-position card edge to the popular bytewide 28-pin DIP socket. An additional ground lead and dual

key positions allow for proper insertion and withdrawal of Nonvolatile Read/Write Cartridges. A six-inch cable length allows for flexibility in end applications but does not substantially affect the performance characteristics of the DS1217.

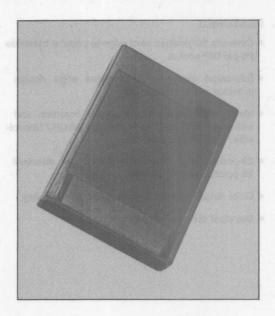
7



# DS9002 Cartridge Housing

#### **FEATURES**

- Two-piece, snap together construction
- Matches form factor of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- Made of rugged, flame-retardant ABS plastic
- Accepts DS9003 Cartridge Proto Board
- Opening for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" PCB



#### DESCRIPTION

The DS9002 Cartridge Housing is a rugged, two-piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either through-hole mounted or surface mounted on both sides depending upon density requirement and board

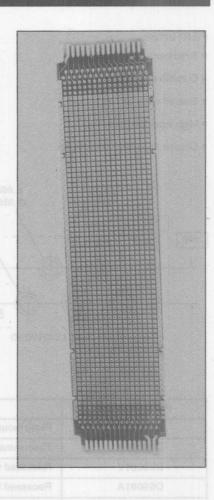
design. The outside profile of the PCB should match the DS9003 Cartridge Proto Board. Applications include nonvolatile static RAM, ROM, or EPROM memory cartridges.



## DS9003 Cartridge Proto Board

#### **FEATURES**

- Matches profile of DS1217 Nonvolatile Read/Write Cartridges
- Plated through-hole pattern for wire wrap or solder mount development
- Allows for a single double-size cartridge or two standard-size cartridges
- · Gold-plated card edge fingers
- Connects to standard 28-pin DIP socket via DS9000 Bytewide Cable Harness
- · Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



#### **FEATURES**

The DS9003 Cartridge Proto Board is a developmental printed circuit board for prototyping portable hand-held cartridges. The gold-plated card edge connections conform to the popular 28-pin bytewide DIP socket pinout

when used with the DS9000 Bytewide Cable Harness. The card profile matches that of the DS1217 Nonvolatile Read/Write Cartridges and can be used with the DS9002 Cartridge Housing.

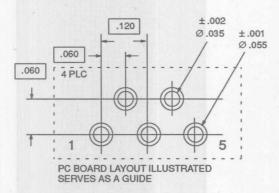
7

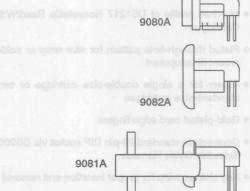


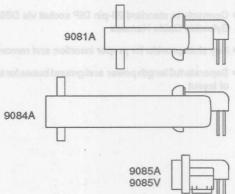
## DS908xx CyberKey/Card Receptacles

#### **FEATURES**

- Solid base metal contacts
- Durable and rugged
- Guided entry on receptacle
- High insertion force
- Greater than 50,000 cycle life







PART NUMBER	DESCRIPTION
DS9080V	Flush mount CyberKey receptacle, vertical PCB mount
DS9080A	Flush mount CyberKey receptacle, right angle PCB mount
DS9081V	Recessed CyberKey receptacle, vertical PCB mount
DS9081A	Recessed CyberKey receptacle, right angle PCB mount
DS9082V	Flush mount CyberCard receptacle, vertical PCB mount
DS9082A	Flush mount CyberCard receptacle, right angle PCB mount
DS9084V	Recessed CyberCard EV receptacle, vertical PCB mount
DS9084A	Recessed CyberCard EV receptacle, right angle PCB mount
DS9085A	Flush mount CyberCard receptacle, right angle PCB mount
DS9085V	Flush mount CyberCard receptacle, vertical angle PCB mount

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 

Silicon Timed Circuits

Multiport Memory

MASI elitslovnok

ntelligent Sockets

Timekeeping

Jser-Insertable Memory

User-Insertable Memory (Secured)

Battery Backup and Battery Chargers

System Extension

Sip Stik Prefabs

Automatic Identification

Microcontrollers

Telecommunications

Teleservicing

Packages

# **DALLAS**SEMICONDUCTOR

## DS1204U Electronic Key

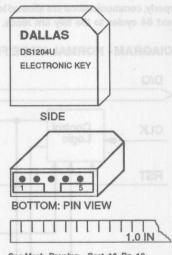
#### **FEATURES**

- · Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit security match code virtually prevents deciphering by exhaustive search with over 10<sup>19</sup> possibilities
- 128 bits of secure read/write memory create additional al barriers by permitting data changes as often as needed
- Rapid erasure of identification security match code and secure read/write memory can occur if tampering is detected
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low-power CMOS circuitry
- · Four million bps data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

#### DESCRIPTION

The DS1204U Electronic Key is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a procedure with a serial format to retrieve or update data. Interface cost to a microprocessor is minimized by on-chip circuit-

#### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 12

#### DIN DESCRIPTION

LIM PERCUIT LIGH	
Pin 1 - V <sub>CC</sub>	+5 Volts
Pin 2 - RST	Reset
Pin 3 - DQ	Data Input/Output
Pin 4 - CLK	Clock
Pin 5 - GND	Ground

ry that permits data transfer with only three signals: Clock (CLK), Reset (RST), and Data Input/Output (DQ).

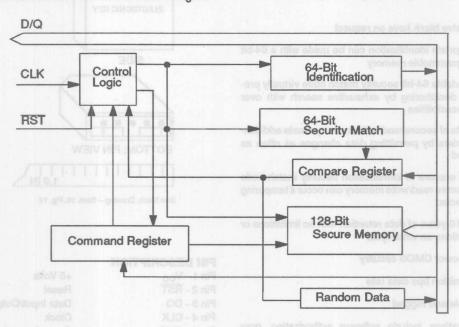
Low pin count and a guided entry for mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

#### **OPERATION - NORMAL MODE**

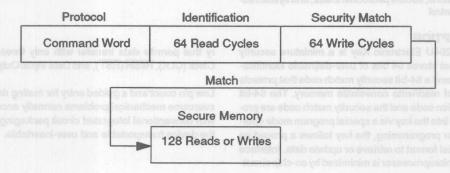
The Electronic Key has two modes of operation: normal and program. The block diagram (see Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, RST is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines normal operation for read or write, or communications are ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are reads. Data is

clocked out of the key on the high-to-low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/ write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

#### **BLOCK DIAGRAM - NORMAL MODE** Figure 1



### **SEQUENCE - NORMAL MODE Figure 2**



Reset High

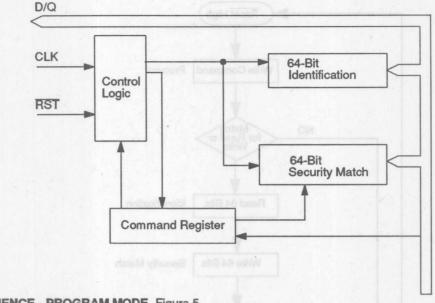
## 8

#### **PROGRAM MODE**

The block diagram in Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode,  $\overline{RST}$  is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact pattern that defines pro-

gram operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the 128 bits that follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

#### **BLOCK DIAGRAM - PROGRAM MODE** Figure 4



#### **SEQUENCE - PROGRAM MODE** Figure 5

Protocol	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

#### **COMMAND WORD**

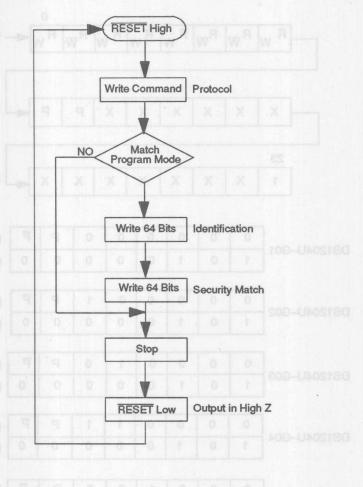
Each data transfer for the normal and program mode begins with a three-byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128-bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern that selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining six bits of byte 2 and the first seven bits of byte 3 form unique patterns that allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has five patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor, the user can specify any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

#### NOTE:

Contact the Dallas Semiconductor sales office for a special command word code assignment that makes possible an exclusive blank key.

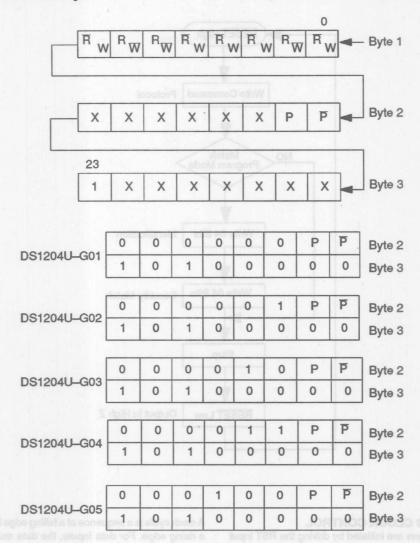


#### RESET AND CLOCK CONTROL

All data transfers are initiated by driving the  $\overline{RST}$  input high. The  $\overline{RST}$  input serves three functions. First, it turns on control logic, which allows access to the command register for the command sequence. Second, the  $\overline{RST}$  signal provides a power source for the cycle to follow. To meet this requirement, a drive source for  $\overline{RST}$  of 2 mA @ 3.0 volts is required. However, if the  $V_{CC}$  pin is connected to a 5-volt source within nominal limits, the  $\overline{RST}$  is not used as a source of power and input levels revert to normal  $V_{IH}$  and  $V_{IL}$  inputs with a drive current requirement of 500  $\mu A$ . Third, the  $\overline{RST}$  signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the RST pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated using RST, the transition of RST must occur while the clock is at a high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

### **COMMAND WORD** Figure 7

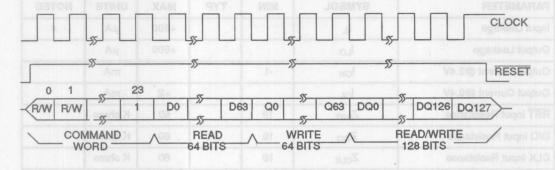


#### **KEY CONNECTIONS**

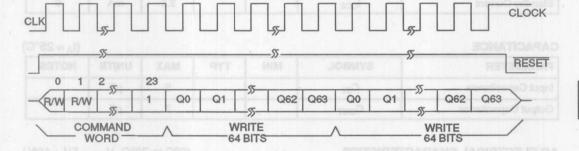
The key is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applica-

tions, contact to the key pins can be determined to ensure connection integrity before data transfer begins. CLK, RST, and DQ all have internal 20K ohm pulldown resistors to ground that can be sensed by a reading device.

### **DATA TRANSFER - NORMAL MODE** Figure 8



## **DATA TRANSFER - PROGRAM MODE** Figure 9



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature -1.0V to +7.0V 0°C to 70°C -40°C to +70°C

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.0	and.		V	1, 8, 10
Logic 0	VIL	-0.3	and the same of	+0.8	V	ulland 13
RESET Logic 1	V <sub>IHE</sub>	3.0			V	1, 9, 11
Supply	Vcc	4.5	5.0	5.5	V	1

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C;  $V_{CC} = 5V \pm 10$ %)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>IL</sub>			+500	μА	4
Output Leakage	l <sub>LO</sub>			+500	μА	
Output Current @2.4V	Іон	-1			mA	
Output Current @0.4V	loL		-	+2	mA	1 0.
RST Input Resistance	Z <sub>RST</sub>	10	201	60	K ohms	MAGE   MAG
D/Q Input Resistance	Z <sub>DQ</sub>	10	GABR	60	K ohms	100
CLK Input Resistance	Z <sub>CLK</sub>	10		60	K ohms	
RST Current @3.0V	I <sub>RST</sub>			2	mA	6, 9, 13
Active Current	I <sub>CC1</sub>	a eurifi.	EUCIN	6	mA	6
Standby Current	I <sub>CC2</sub>	h		2.5	mA	6

## CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

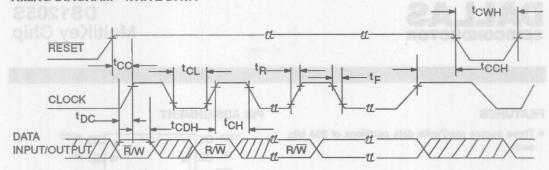
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	Thomas Total	Land	5	pF	7 .0
Output Capacitance	C <sub>OUT</sub>			7	pF	THE PLAN

#### AC ELECTRICAL CHARACTERISTICS

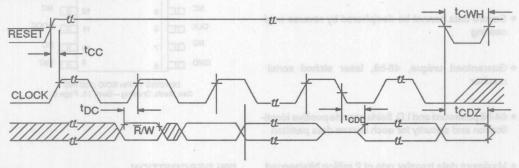
(0°C to 70°C, V<sub>CC</sub> = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	br br	IN ALT IN	ns	2,7
CLK to Data Hold	t <sub>CDH</sub>	40			ns	2,7
CLK to Data Delay	tcdd			100	ns	2, 3, 5, 7
CLK Low Time	t <sub>CL</sub>	125	ego Banolfo	nly and fu	ns	2,7
CLK High Time	t <sub>CH</sub>	125	vem emit	periods of	ns	2,7
CLK Frequency	fclk	DC		4.0	MHz	2,7
CLK Rise & Fall	t <sub>R</sub> , t <sub>F</sub>	500	RUN DAY	IAHERO	ns	2,7
RST to CLK Setup	tcc	1	700070		μѕ	2,7
CLK to RST Hold	t <sub>CCH</sub>	40	HIV		ns	2,7
RST Inactive Time	tcwH	125	-BV		ns	2, 7, 14
RST to I/O High Z	t <sub>CDZ</sub>		SHIY	50	ns	2,7

#### **TIMING DIAGRAM - WRITE DATA**



#### **TIMING DIAGRAM - READ DATA**



#### NOTES:

- 1. All voltages are referenced to GND.
- 2. Measured at  $V_{IH} = 2.0$  or  $V_{IL} = .8V$  and 10ns maximum rise and fall time.
- 3. Measured at  $V_{OH} = 2.4$  volts and  $V_{OL} = 0.4$  volts.
- 4. For CLK, D/Q, and RST.
- 5. Load capacitance = 50 pF.
- 6. Measured with outputs open.
- 7. Measured at  $V_{IH}$  of  $\overline{RST} \ge 3.0V$  when  $\overline{RST}$  supplies power.
- Logic 1 maximum is V<sub>CC</sub> + 0.3 volts if the V<sub>CC</sub> pin supplies power and RST + 0.3 volts if the RST pin supplies power.
- 9. Applies to  $\overline{RST}$  when  $V_{CC} < 3.0V$ .
- Input levels apply to CLK, DQ, and RST while V<sub>CC</sub> is within nominal limits. When V<sub>CC</sub> is not connected to the key, then RST input reverts to V<sub>IHE</sub>.
- RST logic 1 maximum is V<sub>CC</sub> + 0.3 volts if the V<sub>CC</sub> pin supplies power and 5.5 volts maximum if RST supplies power.
- 12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected to the designate of manufacture.
- 13. Average AC  $\overline{RST}$  current can be determined using the following formula:  $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3}) (CL + 140)^f$

I<sub>TOTAL</sub> and I<sub>LOAD</sub> are in mA; C<sub>L</sub> is in pF; f is in MHz.

Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I<sub>TOTAL</sub> of 5 mA.

14. When RST is supplying power t<sub>CWH</sub> must be increased to 100 ms average.

#### **FEATURES**

- Three secure read/write data partitions of 384 bits each
- One non-secure read/write data partition of 512 bits
- Secure data cannot be deciphered by reverse engineering
- Guaranteed unique, 48-bit, laser etched serial number
- 64-bit password and I.D. fields provide positive identification and security for each secure data partition
- Maximum data transfer rate of 2 million bits/second
- Low-power CMOS circuitry
- Access via 3-wire or 1-wire interface
- Applications include proprietary data, financial transactions, secure personnel areas, and systems access control

#### DESCRIPTION

The DS1205S MultiKey Chip is an enhanced version of the DS1204U Electronic Key which has both a standard 3-wire interface (data, clock, and reset) and a 1-wire interface. The DS1205S MultiKey has three secure read/write subkeys which are each 384 bits in length. In addition, there is a 512-bit read/write scratchpad which can be used as a non-secure data area or as a holding register for data transfer to one of the three subkeys. Each subkey within the part is uniquely addressable on byte boundaries.

#### PIN ASSIGNMENT

VCCI	四	1	V	16	vcco
NC		2		15	NC
RST		3		14	1/0
DQ		4		13	GND
NC		5		12	NC
CLK		6		11	DQOE
NC		7		10	NC
GND		8		9	BAT

DS1205S 16-Pin SOIC (300 mil) See Mech. Drawing - Sect. 16, Page 6

#### **PIN DESCRIPTION**

VCCI	+5V Supply (Battery Backup Mode)
RST	Reset (3-Wire)
DQ	Data (3-Wire)
CLK	Clock (3-Wire)
GND	Ground TEA has DIE MID I
BAT	Battery (+) (Battery Backup Mode)
DQOE	Data Available (3-Wire)
VO	Data I/O (1-Wire)
Vcco	Battery (+) (Battery Powered Mode)

#### **OPERATING MODES**

There are two modes of operation for powering the DS1205S MultiKey Chip. In the Normal Mode (Battery Backup),  $V_{\rm CC}$  power is supplied to the part on the  $V_{\rm CCI}$  pin, while the battery backup source is applied to the BAT pin. In this mode of operation, the chip supply is switched internally between  $V_{\rm CCI}$  and BAT (depending on which is higher) and this level is presented internally to the  $V_{\rm CCO}$  pin. In the Battery Operate Mode, the battery supply is connected directly to the  $V_{\rm CCO}$  pin while the  $V_{\rm CCI}$  and BAT pins are grounded.

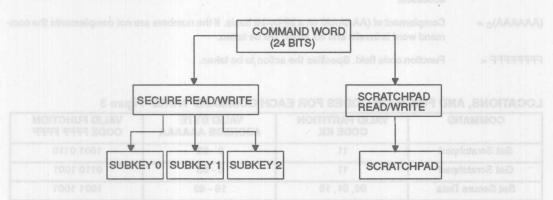
#### INTERFACES

Two interfaces to the DS1205S are provided. The 1-wire interface requires a 1-wire I/O command for addressing the device. An additional function command word is then passed through the 1-wire interface to access the various DS1205S functions. The 3-wire interface (data (DQ), reset (RST), and clock (CLK)) requires only the function command word. The four 1-wire I/O commands that deal with the unique lasered ROM are available only through the 1-wire interface. All other functions are available through either interface.

#### **FUNCTIONS**

A command word written written to the DS1205S Multi-Key specifies the operation to be performed and the partition to be operated on. There are two classes of functions available. One class includes operations on the read/write secure partitions. The other class includes operations on the read/write scratchpad (Figure 1).

#### **COMMAND OPERATIONS Figure 1**



The 24 bit function command word is organized into three fields of eight bits each. These one byte fields include the function to be performed, the memory partition to be accessed and the starting byte address for the data transfer operation. The starting byte address and the partition codes are required to be given in both real and complement form. If these values do not match, access to the part will be denied (Figure 2).

The function command word is presented to the DS1205S LSB first. The first byte contains the 8-bit

function code that defines which of the six valid function codes is to be executed. Each function code is valid for only certain partition and starting address combinations. Figure 3 illustrates the valid partition code, starting address and function code combinations. The second byte consists of the 2-bit partition code, identifying which partition is being accessed, and the 6-bit starting byte address, which specifies where to start the access of the given partition. The third byte consists of the complement of the 2-bit partition code and the complement of the 6-bit starting byte address.

### COMMAND WORD STRUCTURE Figure 2

MSB			LSB	
(KK)c(AAAA	AA)c (	KK) (AAAAAA)	FFFFFF	FF

Two-bit number specifying which partition is to be accessed, 00 specifies subkey 0, 01 specifies (KK) = subkey 1. 10 specifies subkey 2. 11 specifies the scratchpad.

Complement of (KK) on a bit-by-bit basis. If the numbers are not complements the command (KK)c = word is invalid and no action will be taken.

Address field containing address bits that define the starting byte address of the partition to be

(AAAAAA) =accessed.

 $(AAAAAA)_C =$ Complement of (AAAAAA) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

FFFFFFF = Function code field. Specifies the action to be taken.

## LOCATIONS, AND FUNCTION CODES FOR EACH COMMAND WORD Figure 3

COMMAND	VALID PARTITION CODE KK	VALID BYTE ADDRESS AAAAAA	VALID FUNCTION CODE FFFF FFFF	
Set Scratchpad	11	0 - 63	1001 0110	
Get Scratchpad	21A/10/6 11	0 - 63	0110 1001	
Set Secure Data	00, 01, 10	. 16 - 63	1001 1001	
Get Secure Data	00, 01, 10	16 - 63	0110 0110	
Set Security Match	00, 01, 10	000000	0101 1010	
Move Block	00, 01, 10	000000	0011 1100	

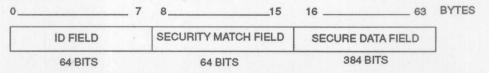
#### SECURE PARTITION COMMANDS

Each of the three secure partitions within the DS1205S MultiKey is comprised of a 64-bit I.D. field, a 64-bit security match code and a 384-bit secure data field (Figure 4). The three commands that operate on the secure partitions are:

- 1) Set Security Match
- 2) Set Secure Data
- 3) Get Secure Data

As a guard against attackers, the security match code can never be read. Similarly, tampering through reprogramming will immediately clear the entire secure partition.

## **SECURE PARTITION ORGANIZATION** Figure 4



#### SET SECURITY MATCH

The Set Security Match command is used to enter data into the I.D. and security match fields of the selected secure partition. The DS1205S will respond to the command by outputting the 64-bit I.D. field of the selected secure partition. The next 64 clock cycles are used to echo the I.D. field back to the DS1205S. Upon receipt of the correct I.D., the DS1205S MultiKey will erase the contents of the selected secure partition. The part is then ready to receive the the new 64-bit I.D. and the 64-bit security match code. The flow sequence is shown in Figure 5.

#### SET SECURE DATA

The Set Secure Data command is used to write data into the selected secure partition. After the command is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is output. The next 64 bits of input comprise a password that must match the security match code of the selected secure partition. If the password and the security match are identical, data is written to the secure data field starting at the address specified in the command word. If the password and the security match code are not identical, the DS1205S will terminate the transaction immediately. The flow sequence is shown in Figure 6.

#### **GET SECURE DATA**

The Get Secure Data command is used to retrieve data from the selected secure partition. After the command word is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is returned. The next 64 bits are the password being written to the DS1205S. If the presented password and the security match code of the selected secure partition are identical, the DS1205S will output the contents of the secure data field starting from the byte specified in the command word. If the presented password is not identical to the security match code, the DS1205S MultiKey will use the password as a "seed" for its internal random number generator. This results in a repeatable, seemingly valid yet false response to the invalid password. The flow sequence is shown in Figure 7.

#### SCRATCHPAD READ/WRITE COMMANDS

The 512-bit read/write scratchpad of the DS1205S MultiKey is not protected by a security match code. This

partition is byte addressable. The scratchpad can be used to store unsecured data or it can act as a staging area to build and verify data structures to be transferred to a secure partition. The three commands that operate on the read/write scratchpad are:

- 1) Set Scratchpad Data
- 2) Get Scratchpad Data
- B) Move Block

#### SET SCRATCHPAD DATA

The Set Scratchpad Data command is used to enter data into the DS1205S MultiKey scratchpad. The command word must specify the starting byte address for the data transfer. Valid byte addresses are 0 through 63. The DS1205S MultiKey will write data to the scratchpad until byte 63 has been written or until the RST line goes to a logic low level. The flow sequence is shown in Figure 8.

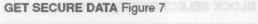
#### **GET SCRATCHPAD DATA**

The Get Scratchpad data command is used to retrieve data from the 512-bit scratchpad. The command word must specify the starting byte address for the data retrieval. Valid byte addresses are 0 through 63. The DS1205S MultiKey will retrieve data from the scratchpad until byte 63 has been read or the RST line goes to a logic low level. The flow sequence is shown in Figure 9.

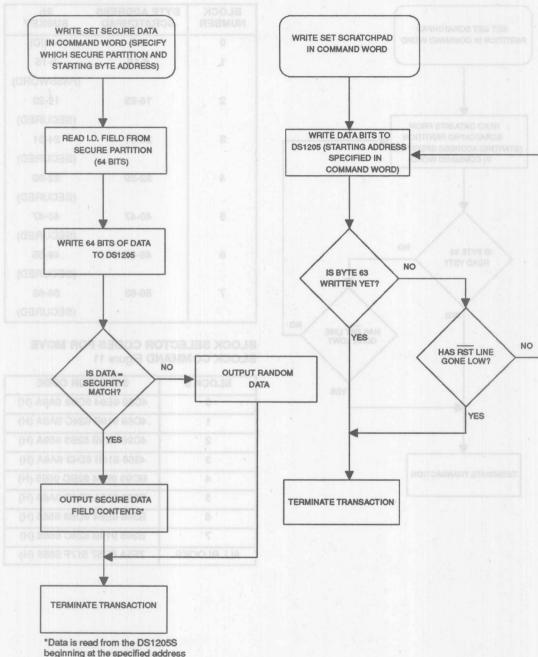
#### **MOVE BLOCK**

The Move Block command is used to transfer data, which has been previously entered into the scratchpad and verified, to one of the three secure subkeys. Data can be transferred as one large block of 512 bits or it can be transferred in blocks of 64 bits each (Figure 10). There are nine valid block selectors which are used to specify which block or blocks are to be transferred (Figure 11). As a further precaution against accidental erasure of a secure subkey, the 64-bit password of the destination subkey must be entered and match the destination subkey. If the passwords fail to match, the operation is terminated. The flow sequence is shown in Figure 12.

#### **SET SECURITY MATCH** Figure 5 **SET SECURE DATA Figure 6** WRITE SET PASSWORD WRITE SET SECURE DATA IN COMMAND WORD (SPECIFY WHICH IN COMMAND WORD (SPECIFY WHICH SECURE PARTITION AND SECURE PARTITION) STARTING BYTE ADDRESS) READ I.D. FIELD FROM SECURE PARTITION (64 BITS) READ I.D. FIELD FROM SECURE PARTITION (64 BITS) WRITE 64 BITS OF DATA TO DS1205 (OLD I.D.) WRITE 64 BITS OF DATA TO DS1205 NO IS DATA = I.D? **TERMINATE** TRANSACTION NO TERMINATE IS DATA = YES TRANSACTION PASSWORD? ERASE I.D. AND PASSWORD FIELD, SECURE DATA FIELD FOR SELECTED YES SECURE PARTITION. WRITE DATA TO SECURE \*Data is written to the DS1205S beginning at the specified address and continuing until either Bit 511 is written or the RST DATA FIELD (STARTING ADDRESS SPECIFIED IN WRITE 64 BITS OF DATA line is brought low. COMMAND WORD)\* FOR NEW I.D. FIELD DATA WRITE 64 BITS OF DATA FOR NEW PASSWORD **TERMINATE TRANSACTION** FIELD DATA TERMINATE **TRANSACTION**

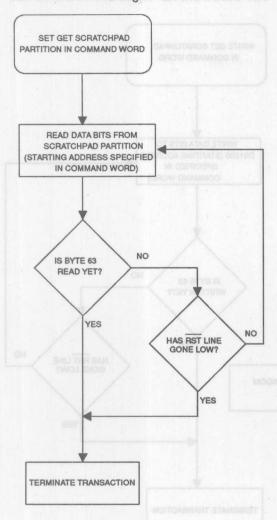


## SET SCRATCHPAD Figure 8



\*Data is read from the DS1205S beginning at the specified address and continuing until either Bit 511 is read or the RST line is brought low.

## SET SCRATCHPAD Figure 9



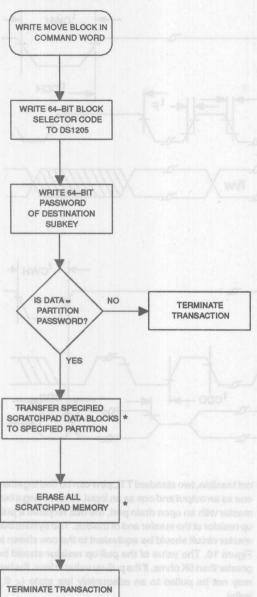
### BLOCK SELECTIONS Figure 10

BLOCK NUMBER	BYTE ADDRESS SCRATCHPAD	IN: SUBKEY
0	Y910 0-7, 080W 08	0-7(ID)
1.	8-15	8-15
		(PASSWORD)
2	16-23	16-23
		(SECURED)
3	24-31	24-31
	(NA BITS)	(SECURED)
4	32-39	32-39
		(SECURED)
5	40-47	40-47
	ATACISC ATISA	(SECURED)
6	48-55	48-55
	-	(SECURED)
7	56-63	56-63
		(SECURED)

## BLOCK SELECTOR CODES FOR MOVE BLOCK COMMAND Figure 11

BLOCK #	SELECTOR CODE
0	4C69 6E64 9DB3 9A9A (H)
1	4C69 919B 624C 9A9A (H)
2	4C96 6E9B 62B3 659A (H)
3	4366 616B 6D43 6A6A (H)
4	BC99 9E94 92BC 9595 (H)
5	B369 9164 9D4C 9A65 (H)
6	B396 6E64 9DB3 6565 (H)
7	B396 919B 624C 6565 (H)
ALL BLOCKS	7F5A 5D57 517F 5656 (H)

## **MOVE BLOCK** Figure 12



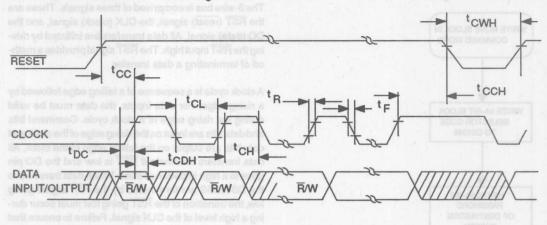
\*TRANSPARENT TO USER

#### 3-WIRE BUS

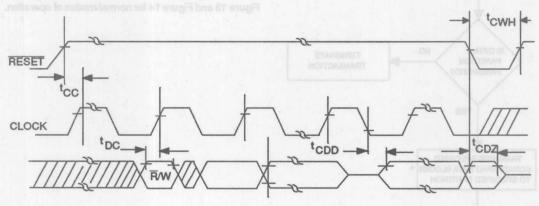
The 3-wire bus is comprised of three signals. These are the RST (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the RST input high. The RST signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if RST is low and the DQ pin goes to a high impedance state. When data transfers to the DS1205S are terminated by the RST signal going low, the transition of the RST going low must occur during a high level of the CLK signal. Failure to ensure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figure 13 and Figure 14 for normal modes of operation.

### WRITE DATA TIMING DIAGRAM Figure 13



## READ DATA TIMING DIAGRAM Figure 14



#### 1-WIRE PROTOCOL

The 1-wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1205S is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence.

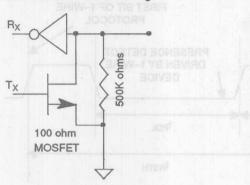
#### **Hardware Configuration**

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain connections. The DS1205S is an open drain part with an internal circuit equivalent to that shown in Figure 15. Ideally, the bus master should also be open drain; but if this is

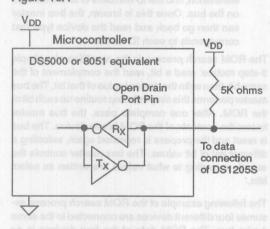
not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 16. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left for more than 560  $\mu$ S, all components on the bus will be reset.

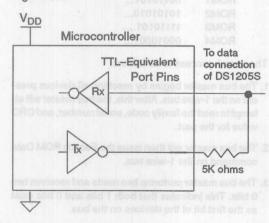
### **EQUIVALENT CIRCUIT Figure 15**



#### BUS MASTER OPEN DRAIN CIRCUIT Figure 16A



## **BUS MASTER STANDARD TTL CIRCUIT**Figure 16B



### **Transaction Sequence**

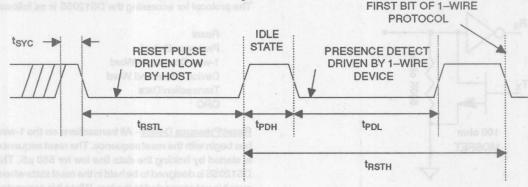
The protocol for accessing the DS1205S is as follows:

Reset
Presence Detect
1-wire Command Word
Device Command Word
Transaction/Data
CRC

Reset/Presence Detect - All transactions on the 1-wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 560  $\mu S$ . The DS1205S is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high, the part is taken out of reset, and the part is ready to issue the presence detect.

After detecting a high state on the data line, the DS1205S waits  $15\,\mu\text{S}$  minimum and issues its presence detect. This presence detect is a low-going pulse that last  $70\,\mu\text{S}$ . This response to the reset pulse lets the bus master know that the DS1205S is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise as the DS1205S is taken on and off the bus. Refer to the timing diagram in Figure 17.

After the DS1205S has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1  $\mu S$ . The 1  $\mu S$  interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 17.



1-Wire I/O Commands - Once the bus master has detected a presence, it can issue one of the four different 1-wire I/O commands. These commands deal with the laser-etched ROM code which has the following format.

Type ID	Unique Serial Number	CRC
8 bits	48 bits	8 bits

All 1-wire commands are eight bits long. A list of these commands are as follows:

#### CCh Pass Thru Mode

This command saves time by allowing direct access to the DS1205S without identifying it by ROMID number. This command can only be used when there is a single slave on the bus. If more than one device is present, there will be bus contention.

#### 33h Read ROM Data

This command allows the bus master to read the DS1205S's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1205S on the bus. If more than one is present, there will be bus contention.

#### 55H Match ROM Data

This mode allows the bus master to single out a specific DS1205S on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple device on the bus.

#### F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the ID numbers of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101
ROM2	10101010
ROM3	11110101
ROM4	00010001

The search process is as follows:

- The bus master begins by resetting all devices present on the 1-wire bus. After this, the bus master will attempt to read the family code, serial number, and CRC value for the part.
- The bus master will then issue the Search ROM Data command on the 1-wire bus.
- 3. The bus master performs two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the first bit of the devices on the bus.

- 4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
- 5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
- The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
- 7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
- The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
- The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired.
   This completes the first pass and uniquely identifies one part on the 1-wire bus.

At this point, the bus master repeats the process described above to determine the address of the remaining devices on the 1-wire bus by repeating steps 1 though 7.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ID is:

$$960 \mu S + 3(8+64) \times 0.06 mS = 13.92 mS$$

The bus master is therefore capable of identifying 60 different 1-wire devices per second.

Additionally, the data obtained from the two reads of each set of three have the following interpretations:

- There are still devices attached which have conflicting bits in this position.
- All devices still coupled have a zero bit in this bit position.
- All devices still coupled have a one bit in this bit position.
- 11 There are no devices attached to the 1-wire bus.

<u>Transmitting/Receiving Data</u> - All communications on the 1-wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1205S is in the listening mode. The bus master must then transmit the 1-wire command to the DS1205S. To transmit the first bit of the 1-wire I/O command, the master pulls the bus low for 1  $\mu$ S. This low-going edge informs the DS1205S that the first bit is being sent. After 1  $\mu$ S, the master does one of two things:

- holds the line low for an additional 70 μS to output a 0 (write a 0) or,
- 2. lets the bus go high for an additional 70 µS (write a 1).

The state of the bus during this 70  $\mu$ S time phase determines the value of the bit. The DS1205S will sense any rising edge during this 70  $\mu$ S time phase as a one. After the 70  $\mu$ S has lapsed, the bus master must then drive the bus high for 1  $\mu$ S. This is the frame sync mentioned earlier. This process is repeated until all the eight bits are transmitted. Refer to the timing diagram in Figure 18.

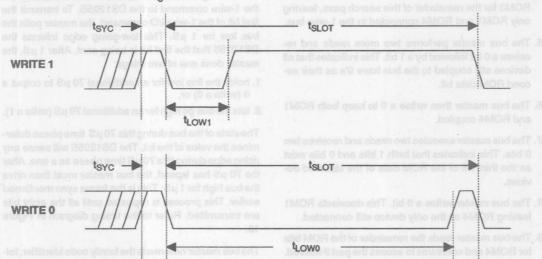
The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1 µS. This informs the DS1205S that it should have data on the bus no later than the 1 µS from the falling edge. After the 1 µS, the bus master lets go of the bus and the DS1205S drives the bus. The slave must hold the data on the bus for an additional 14 µS minimum (59 µS maximum). During the DS1205S holding time, the bus master reads the state of the bus. Ideally, the bus master should read data from the bus 15 µs after the falling edge. The entire cycle time for one bit lasts a minimum of 70 µS (140 µS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1 µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 19 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1205S must be reset.

CRC Generation - To validate the transmitted data from the DS1205S, the bus master must generate a CRC value for the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1205S. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. The CRC is calculated using the following polynomial.

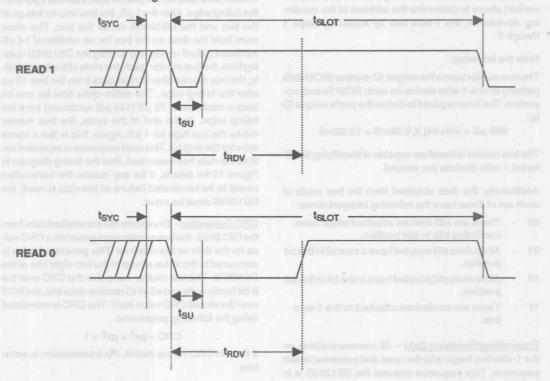
$$CRC = px^{3} + px^{2} + 1$$

If the two CRC values match, the transmission is errorfree.

## 1-WIRE WRITE TIMING Figure 18



## 1-WIRE READ TIMING Figure 19



#### PASS-THRU MODE

A host connected to the 1-wire bus may send function commands directly to the DS1205S without preceding them with 1-wire I/O commands by using the pass-thru command (CCh). This command bypasses the serial number and consequently it can only be used when there is one DS1205S on the 1-wire bus.

#### 1-WIRE/3-WIRE ARBITRATION

The DS1205S can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to +7.0V -40°C to +85°C -55°C to +125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for ext ended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.0	100)		V	889
Logic 0	VIL	-0.3	rw5/	+0.8	V	Wilder   Tal
Supply	V <sub>CC</sub>	4.5	5.0	5.5	V	OVATE

#### DC FLECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>IL</sub> or		o sel	+500	μА	nie Slot P
Output Leakage	I <sub>OL</sub>		surs d	+500	μА	troul I estit
Output Current @ 2.4V	Гон	-1	man d		mA	ws I 0 etri
Output Current @ 0.4V	loL			+1	mA	atell bea
RST Input Resistance	Z <sub>RST</sub>	100		1000	Kohm	eteC has
D/Q Input Resistance	Z <sub>DQ</sub>	100		1000	Kohm	
CLK Input Resistance	Z <sub>CLK</sub>	100	310	1000	Kohm	
Active Current	l <sub>CC1</sub>	-	3	6	mA	5,6
Standby Current	I <sub>CC2</sub>		1809	100	μА	5,6
Batt. Operate Consumption	I <sub>BAT</sub>		200	500	nC	7,8
Batt. Operate Standby Current	I <sub>BATS</sub>	1	30	200	nA	7
Batt. Voltage	V <sub>BAT</sub>	2.0		3.6	V	1
Output Supply Current	Icco			10	mA	11

CAPACITANCE (tA= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	dani se C <sub>IN</sub> disove	undt-eau	g and price	5	pF	e-1 risky m
Output Capacitance	Соит	nortw b	new ed wh	7	pF	bris soder

## AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	35	412/2/20	TA 22 8 8 8 8 8	ns	2
CLK to Data Hold	t <sub>CDH</sub>	40	bni	ive to Gro	ns	2
CLK to Data Delay	tcdd			200	ns	2,3,4
CLK Low Time	abroom t <sub>CL</sub> of O 00	250			ns	2
CLK High Time	t <sub>CH</sub>	250	qo isnolor	only and fu	ns	2
CLK Frequency	t <sub>CLK</sub>	DC	isin emit h	2.0	MHz	2
CLK Rise & Fall	t <sub>R</sub> ,t <sub>F</sub>	мотта	тео оиг	500	ns	2
RST to CLK Setup	tcc tcc	1	SHAS		μѕ	2
CLK to RST Hold	t <sub>CCH</sub> as	40	inV Vini		ns	2
RST Inactive Time	t <sub>CWH</sub>	250	VE		ns	2
RST to I/O High Z	t <sub>CDZ</sub>		hoV .	50	ns	2

## AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (0°C to 70°C, V<sub>CC</sub> = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	tslot	70	JII.	140	μS	SZEGU FUG
Write 1 Low Time	tLOW1	1	301	15	μS	mea modin
Write 0 Low Time	t <sub>L</sub> owo	70	RO	140	μS	HUCZ AKBU
Read Data Valid	t <sub>RDV</sub>	15	301		μS	TOO SERVICE
Read Data Setup	tsu	1			μS	10
Frame Sync	tsyc	1			μS	0.0000154.0
Reset Low Time	t <sub>RSTL</sub>	560			μS	
Reset High Time	t <sub>RSTH</sub>	560			μS	9
Presence Detect High	t <sub>PDH</sub>	15		70	μS	ett Oroccal
Presence Detect Low	t <sub>PDL</sub>	70		280	μS	inches D. Har

#### NOTES:

- 1. All voltages are referenced to ground.
- 2.  $V_{IH} = 2.0 V$  or  $V_{IL} = 0.8 V$  with 10 ns maximum rise and fall time.
- 3.  $V_{OH} = 2.4V$  and  $V_{OL} = 0.4V$ .
- 4. Load capacitance = 50 pF.
- 5. Measured with outputs open.
- 6. (Normal battery backup operation)  $V_{CC1} = 5.0 \text{ Volts} \pm 10\%$ ;  $V_{BAT} = 3.0 \text{ Volts}$ .
- 7. (Battery operate mode) V<sub>CCO</sub> = 3.0 Volts.
- 8. Per transaction (512 bits + protocol).
- 9. An additional reset or communication sequence cannot begin until the reset high time has expired.
- 10. Read data setup time refers to the time the host must pull the 1-wire pin low to read a bit. Data is guaranteed to be valid within 1 μS of this falling edge and will remain valid for 14 μS minimum (15 μS total falling edge on 1-wire).
- 11. V<sub>CCO</sub> = V<sub>CCI</sub> 0.3V



#### **FEATURES**

- Three secure read/write data partitions of 384 bits each
- 64-bit security match and I.D. fields provide positive identification and security for each secure data partition
- One non-secure read/write partition of 512 bits
- Electrical tampering is met with seemingly valid, yet false, responses
- Secure data cannot be deciphered by reverse engineering
- Over 10 years of data retention with no limitations on write cycles
- Access via Dallas 3-Wire Interface
- Applications include software authorization, configuration management, and systems access control

#### PIN ASSIGNMENT







See Mech. Drawing - Sect. 16, Pg. 12

#### DESCRIPTION

The DS1205U MultiKey has three, 384-bit read/write data partitions, each protected by its own 64-bit I.D. and security match fields. The security match field, programmed by the customer, can never be read from the DS1205U. An additional security feature, the Intelligent Response generator, uses invalid security match codes as the "seed" to trigger seemingly valid, yet false responses to electronic attack.

Communication with the DS1205U is via the Dallas 3-Wire Interface (Data, Clock, Reset). These signals are under host software control.

The DS1205U MultiKey is designed to be plugged into a standard 5-pin, 0.1 inch-center SIP receptacle. A guide

is provided to insure proper alignment with the receptacle.

System designers can use the DS1205U to insure that their valuable firmware can only by run when a valid key is present. The MultiKey can also contain data on system configurations and upgrade options. Designers may choose to allow maintenance or diagnostic routines to be run only by an authorized key holder.

See the DS1205S MultiKey Chip data sheet for implementation details.

## 8

# DALLAS

**DS1207** TimeKey

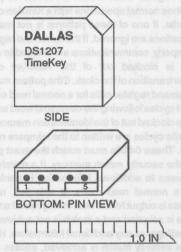
#### **FEATURES**

- Cannot be deciphered by reverse engineering
- Time allotment from one day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit match code virtually prevents discovery by exhaustive search with over 10<sup>19</sup> possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification, security match code and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

#### DESCRIPTION

The DS1207 TimeKey is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 384 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a procedure with a serial format to retrieve or update data. The TimeKey is set to expire from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its count-down from the first access by the end user.

#### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 12

#### **PIN DESCRIPTION**

Pin 1	NC	No connection
Pin 2	RST	Reset
Pin 3	DQ .	Data input/output
Pin 4	CLK	Clock
Pin 5	GND	Ground

Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset (RST) and Data Input/Output (DQ). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

#### OPERATION - NORMAL MODE

The TimeKey has two modes of operation: normal and program. The normal mode of operation provides the functions of reading and writing the 384-bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey, RST is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communications are ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high-to-low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if a normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to write the 384-bit secure memory.

#### **OPERATION - PROGRAM MODE**

The program mode of operation provides the functions of programming the identification and security match memory, and setting and reading the amount of time the TimeKey can be used. The block diagram in Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, RST is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines the program mode for the identification and security match bits or the program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

#### SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time for which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, RST is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20-bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by 220 (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20-bit day clock counter is driven by an internal oscillator that has a period of 82.4 ms. If the command register is properly loaded with the function code for reading the 9-bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If the program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the 9-bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the Time-Key will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24-bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register are ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed, provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24-bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is

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properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24-bit command word only (see Figure 10). This command will only execute prior to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11). First, program the identification and security match bits to the desired value. Use normal mode operation to write the appropriate secure data. Second, write the number days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20-bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. The lock command should be issued, followed by the arm oscillator command. The TimeKey will start the countdown to expiration on the next access. To guarantee security, a locked TimeKey cannot be unlocked. The key cannot be reprogrammed after expiration. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

#### **COMMAND WORD**

Each data transfer for normal and program mode begins with a 3-byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. Eight function codes are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause the transfer to abort. The program mode can be invoked with one of seven function codes: program identification and security match, read the 20-bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining six bits of byte 2 and the first four bits of byte 3 must be written to match one of the five patterns as indicated in Figure 12 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits can be defined by the user as any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 provides a summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode.

Note: Contact the Dallas Semiconductor sales office for special command word code assignment that makes possible an exclusive blank TimeKey.

#### **RESET AND CLOCK CONTROL**

All data transfers are initiated by driving the RST input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the RST signal provides a power source for the cycle to follow. To meet this requirement, a drive source for RST of 2 mA at 3.5 volts is required. Third, the RST signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the clock cycle. Command bits and data bits are input on the rising edge of the clock. Data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the RST pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

#### **TIMEKEY CONNECTIONS**

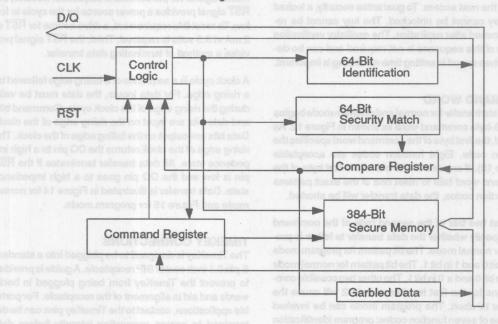
The TimeKey is designed to be plugged into a standard 5-pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to ensure connection integrity before data transfer begins. CLK, RST, and DQ all have 20K ohm pulldown resistors to ground that can be sensed by a reading device.

#### COMMAND WORDS Table 1

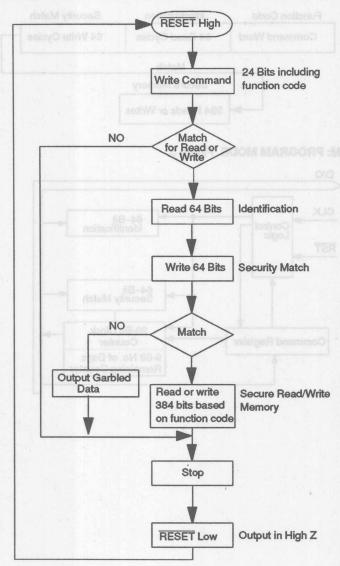
Summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode for the DS1207-G01 only.(See Figure 12 and Figure 13 for detailed command words.)

MODE	FUNCTION	COMMAND WORDS			
	rany rasa pet ve therifolia	MSB		LSB	
NORMAL	READ to sell notes.	B0	01	62	
NORMAL	WRITE	B0	01	9D	
PROGRAM	ed as lambed and WRITE	B0	02	9D	
PROGRAM	READ DAY CLOCK COUNTER	В0	02	F1	
PROGRAM	READ DAYS REMAINING	B0	02	F3	
PROGRAM	WRITE DAYS REMAINING	В0	02	F2	
PROGRAM	ARM OSCILLATOR	В0	02	F5	
PROGRAM	LOCK NUMBER OF DAYS COUNT	В0	02	F6	
PROGRAM	ROGRAM STOP OSCILLATOR		02	F4	

#### **BLOCK DIAGRAM: NORMAL MODE** Figure 1

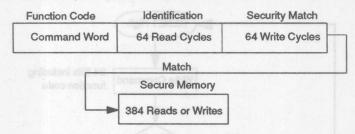


### NORMAL MODE: READ OR WRITE SECURE READ/WRITE MEMORY Figure 2A

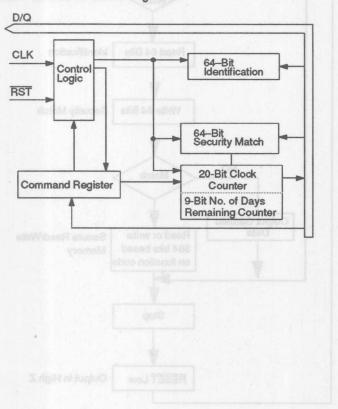


8

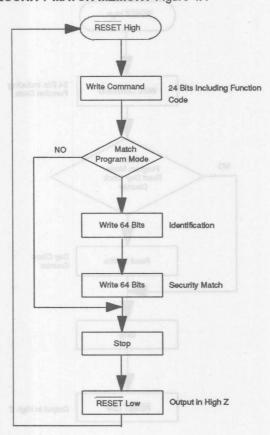
## SEQUENCE: NORMAL MODE, READ OR WRITE SECURE MEMORY Figure 2B



## **BLOCK DIAGRAM: PROGRAM MODE** Figure 3



## PROGRAM MODE: PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 4A

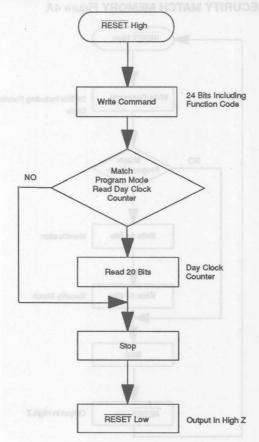


8

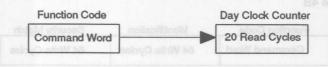
## SEQUENCE: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH BITS Figure 4B

Function Code	Identification	Security Match		
Command Word	64 Write Cycles	64 Write Cycles		

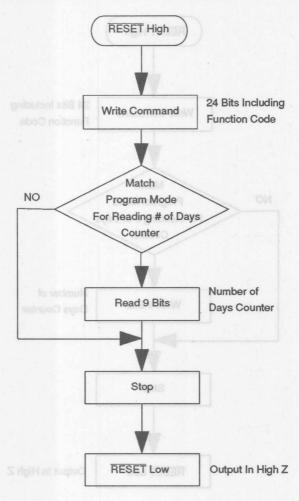
## FLOW CHART: PROGRAM MODE, READING THE 20-BIT DAY CLOCK CALENDAR Figure 5A



## SEQUENCE: PROGRAM MODE, READING THE 20-BIT DAY CLOCK COUNTER Figure 5B



## FLOW CHART: PROGRAM, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6A

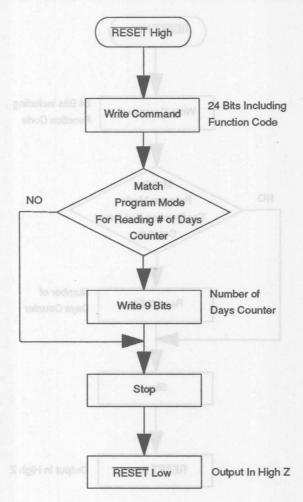


8

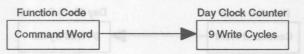
## SEQUENCE: PROGRAM MODE, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6B



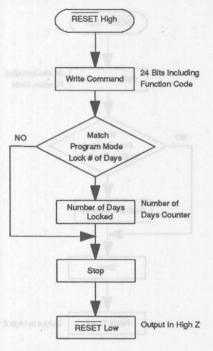
## FLOW CHART: PROGRAM MODE, WRITING TO NUMBER OF DAYS COUNTER Figure 7A



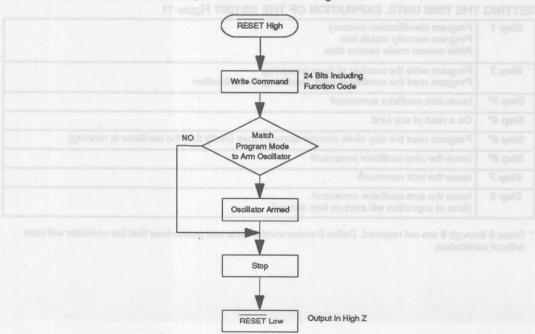
## SEQUENCE: PROGRAM MODE, WRITING THE NUMBER OF DAYS COUNTER Figure 7B



### FLOW CHART: PROGRAM MODE, LOCK NUMBER OF DAYS REGISTER Figure 8

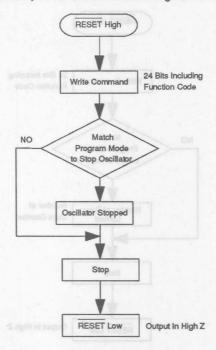


## FLOW CHART: PROGRAM MODE, ARM OSCILLATOR Figure 9



8

## FLOW CHART: PROGRAM MODE, STOP OSCILLATOR Figure 10

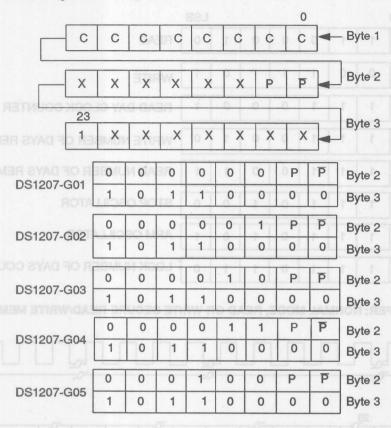


#### SETTING THE TIME UNTIL EXPIRATION OF THE DS1207 Figure 11

Step 1	Program identification memory Program security match bits Write normal mode secure data
Step 2	Program write the number of days remaining Program read the number of days remaining for verification
Step 3*	Issue arm oscillator command
Step 4*	Do a read of any kind
Step 5*	Program read the day clock counter several times (verify that the oscillator is running)
Step 6*	Issue the stop oscillator command
Step 7	Issue the lock command
Step 8	Issue the arm oscillator command (time of expiration will start on first access)

<sup>\*</sup> Steps 3 through 6 are not required. Dallas Semiconductor tests and guarantees that the oscillator will start without verification.

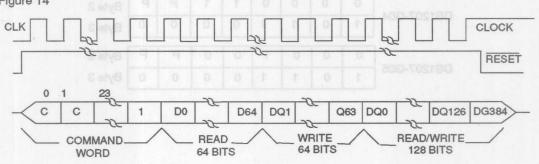
### COMMAND WORD Figure 12 Transpill draw disamilated for STY8 Table 22000 MOITOMUS



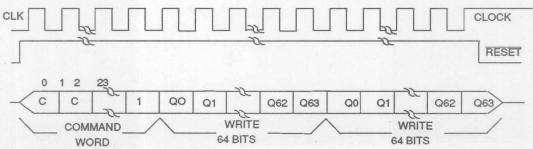
## FUNCTION CODES: FIRST BYTE OF COMMAND WORD Figure 13

MSB	3						LSB	
0	1180	1	0	0	0	1	0	READ
1	0	0	1	1	1	0	1	WRITE
1	1	1	1	0	0	0	1	READ DAY CLOCK COUNTER
1	1	1	1 X	0	0	1	0	WRITE NUMBER OF DAYS REMAINING
1	- <b>1</b> 9h	81	91	0	0	(1	01	READ NUMBER OF DAYS REMAINING
1	1	1	1	0	1	0	0	STOP OSCILLATOR
1	1	1	1	0	1	0	1	ARM OSCILLATOR
1	1	1	q <sup>1</sup>	0	1	1	0	LOCK NUMBER OF DAYS COUNT

## DATA TRANSFER: NORMAL MODE, READ OR WRITE SECURE READ/WRITE MEMORY Figure 14

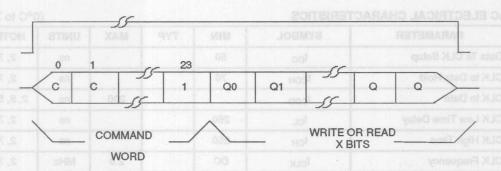


# DATA TRANSFER: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 15A



## DATA TRANSFER: PROGRAM MODE, DAY CLOCK, DAYS REMAINING AND OSCILLATOR CONTROL Figure 15B





NOTE: The number of bits which follow the command word will be either 0, 9, or 20 bits based on the function code.

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature

-1.0V to +7.0V 0°C to 70°C -40°C to +70°C

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.0			V	1
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1
Reset Logic 1	VIHE	3.5	N	611	V NO	010 1

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; RST = 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL			+500	μА	4
Output Leakage	I <sub>LO</sub>			+500	μА	
Output Current @2.4V	Іон	-1			mA	
Output Current @0.4V	loL			+2	mA	THE ST
RST Input Resistance	Z <sub>RST</sub>	10		60	K ohms	I I I Rose
D/Q Input Resistance	Z <sub>DQ</sub>	10	- 100	60	K ohms	
CLK Input Resistance	Z <sub>CLK</sub>	10		60	K ohms	
RST Current @3.5V	I <sub>RST</sub>			2	mA	6, 9

CAPACITANCE O UMA OMIMAMER EYAO DOOLO YAO EIGOM MAROORY SHEREN

 $(t_A = 25^{\circ}C)$ 

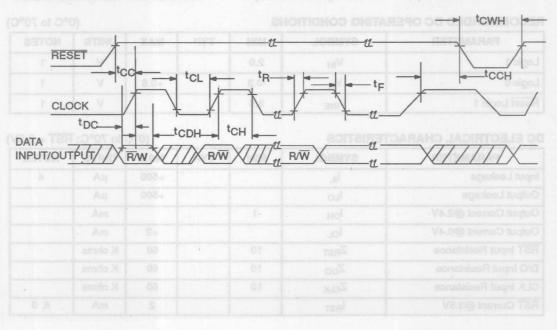
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			5	pF	CUK
Output Capacitance	C <sub>OUT</sub>			7	pF	

#### **AC ELECTRICAL CHARACTERISTICS**

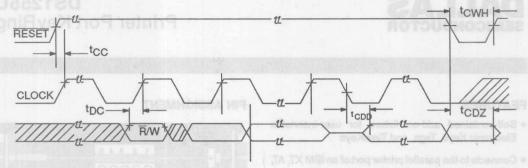
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t <sub>DC</sub>	50	100		ns	2,7
CLK to Data Hold	t <sub>CDH</sub>	70			ns	2,7
CLK to Data	t <sub>CDD</sub>			200	ns	2, 3, 5, 7
CLK Low Time Delay	t <sub>CL</sub>	250			ns	2,7
CLK High Time	tcн	250	0	COMINIA	ns	2,7
CLK Frequency	fclk	DC		2.0	MHz	2,7
CLK Rise & Fall	t <sub>R</sub> , t <sub>F</sub>	blow brismi	oo erit wol	500	ns ns	2,7
RST to CLK Setup	tcc	1			μѕ	2,7
CLK to RST Hold	t <sub>CCH</sub>	60	bai	ive to Gre	ns	2,7
RST Inactive Time	t <sub>CWH</sub>	10			ms	2, 7,
RST To I/O High Z	t <sub>CDZ</sub>			70	ns	2,7

#### **TIMING DIAGRAM - WRITE DATA**



#### TIMING DIAGRAM: READ DATA



#### NOTES:

- 1. All voltages are referenced to GND.
- 2. Measured at VIH = 2.0 or VIL = .8V and 10 ns maximum rise and fall time.
- 3. Measured at VOH = 2.4 volts and VOL = 0.4 volts.
- 4. For CLK, D/Q, and RST.
- 5. Load capacitance = 50 pF.
- 6. Measured with outputs open.
- 7. Measured at VIH of RST greater than or equal to 3.5 volts.
- Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the
  week of manufacture. The expected t<sub>DB</sub> is defined as starting at the date of manufacture.
- 9. Average AC RST current can be determined using the following formula:

ITOTAL = 2 + ILOAD DC + (4 x 10-3)(CL + 280)f

ITOTAL and ILOAD are in mA; CL is in pF; f is in MHz.

Applying the above formula, a load capacitance of 50 pF

running at a frequency of 2.0 MHz gives an I<sub>TOTAL</sub> of 1.6 mA.

8



## DS1255U Printer Port KeyRing

#### **FEATURES**

- Self-contained add-on fixture for user-insertable Electronic Keys, Tags, and TimeKeys
- Connects to the parallel printer port of an IBM XT, AT, PS/2, or compatible computer
- End user installation
- Machine screw SIPS ensure connection to DS1204U key pins
- Two keys may be resident at one time
- Transient suppression circuits protect against electrostatic discharge or accidental connection to serial port
- Key, Tag, and TimeKey communications are totally controlled by software
- Normal computer/printer operation is unaffected
- Applications include software authorization, Key and Tag programmer, computer site identification, and access control

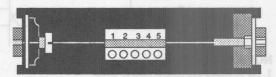
#### DESCRIPTION

The DS1255U Printer Port KeyRing adapts low-pin Electronic Keys (DS1204U), Tags (DS1201), and Time-Keys (DS1207) to the IBM PC parallel printer port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the KeyRing, and reconnecting the printer to the back connector on the KeyRing. Two Keys or Tags can be resident at the same time. Communication with Keys is established by soft ware-controlled sequences to the parallel printer port. The three control signals (Reset, Clock, and Data In/Out) for Keys are generated by the parallel port.

#### **OPERATION**

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals RST, CLK, and D/Q must be software-controlled to du-

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

Pin 1	Vcc	+5 Volts
Pin 2	RST	RESET
Pin 3	D/Q	Data In/Out
Pin 4	CLK	CLOCK
Pin 5	GND	GROUND

plicate the behavior as defined in the respective data sheet for keys. Each signal is a function of a specific output or I/O line of the printer port (Figure 1). Pin 4 on the 25-pin D connector parallel printer port is called Data Out 2 (D2). This signal is used to provide  $\overline{RST}$  for the KeyRing and must be kept at high level when communicating with keys. When  $\overline{RST}$  is driven low, all communication to keys is terminated. The  $\overline{RST}$  signal is also used as a source of power for keys (see respective data sheets).

Pin 5 on the 25-pin D connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of keys. Because the CLK signal provides timing, the relationship between both level and transition is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to keys,

and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will guarantee that data is valid as the CLK changes level.

Pin 17 on the 25-pin D connector parallel printer port is called SLCTIN and is used as the data I/O signal for keys. This is a bidirectional signal. Data is output from this port signal during write cycles and input from keys during read cycles. In addition, Pin 12 on the 25-pin D connector parallel printer port is called PAPER EMPTY and can be used to read data from the keys. This would be required for non-compatible printer ports, with Pin 17 as an output only. Pin 18 on the 25-pin D connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. Example software for IBM PC, XT, AT or compatible computers is available from the factory. In order to avoid having the

printer interpret key communications as printer commands, the strobe signal (Pin 1 on the 25-pin D connector parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

#### INSTALLATION

The parallel Printer Port KeyRing is installed by first removing the printer cable. If the parallel printer port is not being used, this step is not necessary. The printer cable is removed by loosening the top and bottom retaining screws and unplugging the cable. The next step is to install the KeyRing by plugging the male side of the KeyRing into the female printer port. The top and bottom retaining screws should be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer cable is secure, a Key, Tag, or TimeKey can be plugged into either of two receptacles and the computer and KeyRing are now ready for use.

8

9

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

## **Battery Backup and Battery Chargers**

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

## 9

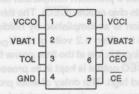


# Nonvolatile Controller Chip

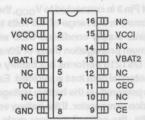
#### **FEATURES**

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V<sub>CC</sub> is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- · Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V<sub>CC</sub> switch
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C

#### **PIN ASSIGNMENT**



DS1210 8-Pin DIP (300 MIL) See Mech. Drawing - Sect. 16, Pg. 1



DS1210S 16-Pin SOIC (300 MIL) See Mech. Drawing - Sect. 16, Pg. 6

#### **PIN DESCRIPTION**

V<sub>CCO</sub> - RAM Supply V<sub>RAT1</sub> - + Battery 1

V<sub>BAT1</sub> -+ Battery 1
TOL - Power Supply Tolerance

GND - Ground

CE - Chip Enable Input CEO - Chip Enable Output

V<sub>BAT2</sub> -+ Battery 2 V<sub>CCI</sub> -+ Supply NC - No Connect

#### DESCRIPTION

The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery

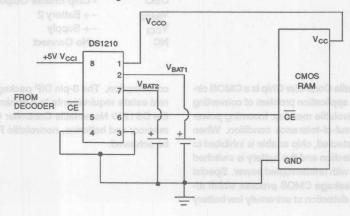
consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

#### **OPERATION**

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V<sub>CCI</sub>) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable (CEO). The third function of write protection is accomplished by holding the CEO output signal to within 0.2 volts of the V<sub>CCI</sub> or battery supply. If CE input is low at the time power fail detection occurs, the CEO output is kept in its present state until CE is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V<sub>CCO</sub>, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions CEO will follow CE with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V<sub>BAT2</sub> pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the CEO and V<sub>CCO</sub> will be forced to VOL. When the batteries are first attached to one or both of the VBAT pins, VCCO will not provide battery back-up until V<sub>CCI</sub> exceeds V<sub>CCTP</sub>, as set by the ToL pin, and then falls below VBAT.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V<sub>CC</sub> is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V<sub>CC</sub> is less than 4.75 volts and to delay its restart on power- up to prevent spurious writes.

#### **SECTION A - BATTERY BACKUP Figure 1**

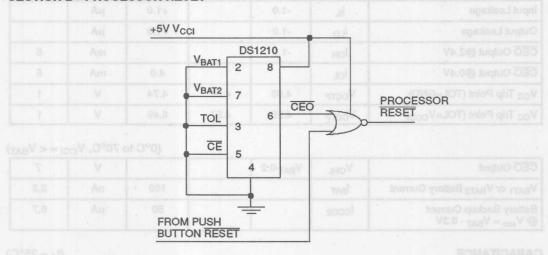


#### BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I<sub>BAT</sub> 100 nA RAM I<sub>CC02</sub> 10 μA Total Drain 10.1 μA

#### SECTION B - PROCESSOR RESET



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V <sub>CCI</sub>	4.75	5.0	5.5	V	1
Pin 3 = V <sub>CCO</sub> Supply Voltage	V <sub>CCI</sub>	4.5	5.0	5.5	QU V O	s (vertpos)
Logic 1 Input	V <sub>IH</sub>	2.2	3)	V <sub>CC</sub> +0.3	new Villets	weld oo
Logic 0 Input	V <sub>IL</sub>	-0.3	क्षर्व	+0.8	Tew VI eta	weld op
Battery Input	V <sub>BAT1</sub> , V <sub>BAT2</sub>	2.0	Al	4.0	reset VI. ets	1,2

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, \text{ V}_{\text{CCI}} = 4.75\text{V to }5.5\text{V}, \text{ Pin }3 = \text{GND})$  $(\text{V}_{\text{CCI}} = 4.5 \text{ to }5.5\text{V}, \text{ Pin }3 = \text{V}_{\text{CCO}})$ 

#### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icci			5 A	r,o mA	3
Supply Voltage	V <sub>cco</sub>	V <sub>CC</sub> -0.2			V	1
Supply Current	I <sub>CCO1</sub>		3.0	80	mA	4
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μА	
Output Leakage	lLO	-1.0		+1.0	μА	
CEO Output @2.4V	Іон	-1.0	JV		mA	5
CEO Output @0.4V	loL	18		4.0	mA	5
V <sub>CC</sub> Trip Point (TOL=GND)	V <sub>CCTP</sub>	4.50	4.62	4.74	V	1
V <sub>CC</sub> Trip Point (TOL=V <sub>CCO</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.49	V	1

(0°C to 70°C, V<sub>CCI</sub> = < V<sub>BAT</sub>)

		All American	(	(* *				
CEO Output	V <sub>OHL</sub>	V <sub>BAT</sub> -0.2		V	7			
V <sub>BAT1</sub> or V <sub>BAT2</sub> Battery Current	I <sub>BAT</sub>		100	nA	2,3			
Battery Backup Current @ V <sub>cco</sub> = V <sub>BAT</sub> - 0.3V	I <sub>CCO2</sub>	T H	50	μА	6,7			

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	f Ve.o-		muon 5 pt go	pF	na egade
Output Capacitance	C <sub>OUT</sub>	010.0		7	pF	or gradated

(0°C to 70°C,  $V_{CCI} = 4.75V$  to 5.5V, Pin 3 = GND)

#### **AC ELECTRICAL CHARACTERISTICS**

(V<sub>CCI</sub> = 4.5 to 5.5V, Pin3 = V<sub>CCO</sub>)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	5
CE High to Power Fail	tpF	CHAN	NOMOJ Đ	0	ns	MINIONE

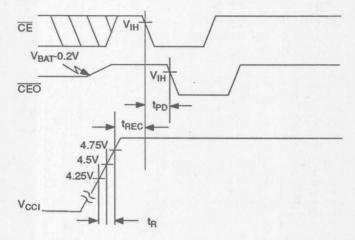
(0°C to 70°C, V<sub>CCI</sub> < 4.75V, Pin 3 = GND; V<sub>CCI</sub> < 4.5, Pin 3 = V<sub>CCO</sub>)

Recovery at Power Up	tREC	2	80	125	ms	Pin S = Vor
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub>	300	Visit		μѕ	Logic 1 Inp
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub>	10	JeV		μѕ	Logic G Inp
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub>	000	VHATE		μѕ	Battery Inp.
CE Pulse Width	t <sub>CE</sub>	1	STARY	1.5	μѕ	8

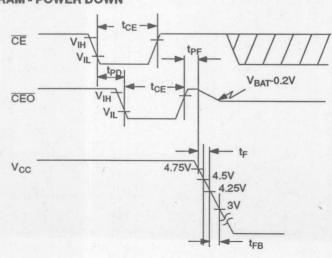
#### NOTES

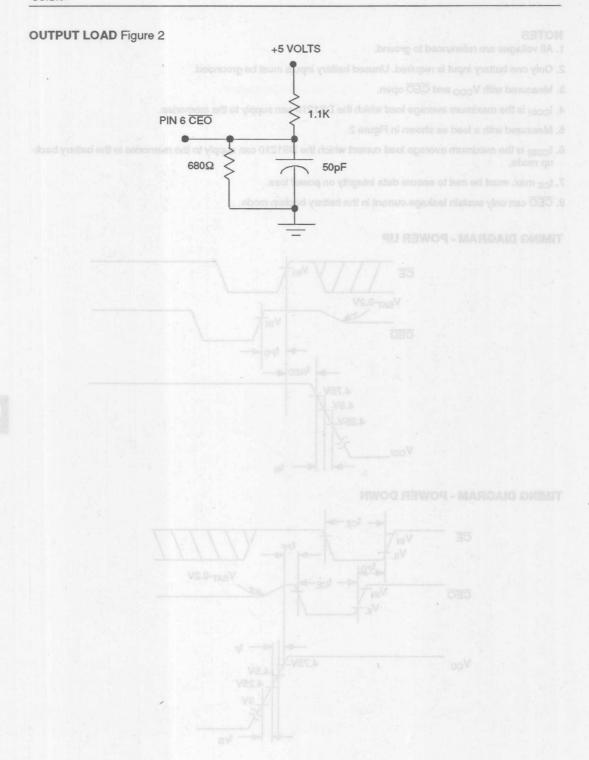
- 1. All voltages are referenced to ground.
- 2. Only one battery input is required. Unused battery inputs must be grounded.
- 3. Measured with V<sub>CCO</sub> and CEO open.
- 4. I<sub>CC01</sub> is the maximum average load which the DS1210 can supply to the memories.
- 5. Measured with a load as shown in Figure 2.
- I<sub>CC02</sub> is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
- 7. t<sub>CE</sub> max. must be met to ensure data integrity on power loss.
- 8. CEO can only sustain leakage current in the battery backup mode.

#### **TIMING DIAGRAM - POWER UP**



#### **TIMING DIAGRAM - POWER DOWN**







# DS1211 Nonvolatile Controller X 8 Chip

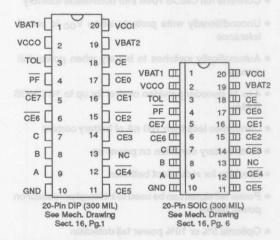
#### **FEATURES**

- · Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V<sub>CC</sub> is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to eight CMOS RAMs
- · Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Powerfail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package
- Optional industrial temperature range of -40° to +85°

#### DESCRIPTION

The DS1211 Nonvolatile Controller x 8 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process

#### PIN ASSIGNMENT



#### **PIN DESCRIPTION**

A, B, C	- Address Inputs
CE	- Chip Enable Input
CE0 - CE7	- Chip Enable Outputs
GND	- Ground
V <sub>BAT1</sub>	- + Battery 1
V <sub>BAT2</sub>	- + Battery 2
TOL	- Power Supply Tolerance
V <sub>CCI</sub>	- +5V Supply
Vcco	- RAM Supply
PF	- Power Fail
NC	- No Connection

which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, nonvolatile RAM operation can be achieved for up to eight CMOS memories.

See the data sheet for the DS1212 Nonvolatile Controller x 16 Chip for electrical specifications and operation.



# DS1212 Olitslovn Nonvolatile Controller X 16 Chip

#### **FEATURES**

- · Converts full CMOS RAM into nonvolatile memory
- Unconditionally write protects when V<sub>CC</sub> is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- · Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Powerfail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package
- Optional industrial temperature range of -40°C to +85°C

#### DESCRIPTION

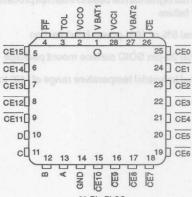
The DS1212 Nonvolatile Controller x16 Chip is a CMOS circuit that solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply the RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process that affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 Nonvolatile Controller chip and lithium batteries, nonvolatile RAM operation can be achieved for up to 16 CMOS memories.

#### **PIN ASSIGNMENT**



28-Pin DIP (600 MIL) See Mech. Drawing - Sect. 16, Pg. 4



28-Pin PLCC See Mech. Drawing - Sect. 16, Pg. 11

#### PIN DESCRIPTION

LIII DESC	RIFTION
A, B, C, D	- Address Inputs
CE	- Chip Enable
CE0-CE15	- Chip Enable Outputs
GND	- Ground
V <sub>BAT1</sub>	- + Battery 1
V <sub>BAT2</sub>	- + Battery 2
TOL	- Power Supply Toleran
11	6)101

V<sub>CCI</sub> -+5V Supply V<sub>CCO</sub> - RAM Supply PF - Power Fail

#### **OPERATION**

The DS1212 performs six circuit functions required to decode and battery back up a bank of up to 16 RAMs. First, the 4 to 16 decoder provides selection of one of 16 RAMs. Second, a switch is provided to direct power from the battery or V<sub>CCI</sub> supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function the DS1212 provides is power fail detection. It constantly monitors the V<sub>CCI</sub> supply. When V<sub>CCI</sub> falls below 4.75 volts, or 4.5 volts, depending on the level of tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the PF signal is driven low. The PF signal will remain low until V<sub>CCI</sub> is back in normal limits.

The fourth function of write protection is accomplished by holding all chip enable outputs ( $\overline{\text{CE0}}\text{-CE15}$ ) to within 0.2 volts of  $V_{\text{CCI}}$  or battery supply. If  $\overline{\text{CE}}$  is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until  $\overline{\text{CE}}$  is driven high. The delay of write protection until the current memory cycle is completed prevents corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with tolerance Pin 3 grounded. If Pin 3 is connected to  $V_{\text{CCO}}$ , then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4-to-16 decoder, shown in Figure 1.

The fifth function the DS1212 performs is a battery status warning so that data loss is avoided. Each time the circuit is powered up, the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted.

The sixth function of the DS1212 provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

#### **NONVOLATILE CONTROLLER/DECODER Figure 1**

- 11	NPUT	S		ALL		- 6		TIT					OUT	PUTS					- mile o	Laure	
CE	D	C	В	A	CE0	CE1	CE2	CE3	CE4	CE5	CE6	CE7	CE8	CE9	CE10	CE11	CE12	CE13	CE14	CE15	PF
Н	X	X	Х	X	Н	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	H	SH	O H	H	H-O	Н
X	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	н	H	Н	Н	H	Н
L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н
L	L	L	Н	Н	Н	Н	Н	L	H	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	H	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	H	Н
L	Н	L	Н	L	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	L	Н	Н	Н	Н	Н
L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

H = High Level

L = Low Level

X = Irrelevant

NOTE: V<sub>CCI</sub> input is 250 mV lower when TOL PIN3 = V<sub>CCO</sub>.

#### ABSOLUTE MAXIMUM RATINGS\*

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature

-0.3V to +7V 0°C to 70°C -55°C to +125°C 260°C for 10 sec

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER 100 100 100 100 100 100 100 100 100 10	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V <sub>CCI</sub>	4.75	5.0	5.5	V	orgon rus
PIN 3 = V <sub>CCO</sub> Supply Voltage	V <sub>cco</sub>	4.5	5.0	5.5	V	1
Logic 1 Input	V <sub>IH</sub>	2.2	fer of (2130	V <sub>CC</sub> +0.3	V	1
Logic 0 Input	No Villament	-0.3	low at the t	+0.8	notic Violo;	Vio afovi
Battery Input	V <sub>BAT1</sub> , V <sub>BAT2</sub>	2.0	oie ourputs iven high.	4.0	V V	1,2

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, \text{V}_{\text{CCI}} = 4.75 \text{ to } 5.5\text{V}, \text{Pin } 3 = \text{GND})$ 

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CCI</sub> = 4.5 to 5.5V, Pin3 = V<sub>CCO</sub>)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Supply Current	Icci	(6)	coder, show	5 3 5	mA	3
Supply Current @ V <sub>ccO</sub> = V <sub>CCI</sub> -0.2	I <sub>CCO1</sub>			80	mA	1,4,10
Input Leakage	I <sub>IL</sub>	-1.0	RECODER	+1.0	μΑ	MACH
Output Leakage	lo	-1.0	850 850 650	+1.0	μА	STURIES D. LO LEG
CE0-CE15,PF Output @ 2.4V	ГОН	-1.0	H M H	HR	mA	5
CE0-CE15,PF Output @ 0.4V	loL	H H	H H H	4.0	mA	5
V <sub>CC</sub> Trip Point (TOL = GND)	V <sub>CCTP</sub>	4.50	4.62	4.74	V	1
V <sub>CC</sub> Trip Point (TOL = V <sub>CCO</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.49	V	11

(0°C to 70°C, VCCI < VBAT)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE0-CE15 Output	V <sub>OHL</sub>	V <sub>BAT</sub> -0.2	<u> </u>	HH	V	3,7
Battery Current	I <sub>BAT</sub>	H R	H H I	0.1	μА	2,3
Battery Backup Current @ V <sub>CCO</sub> =V <sub>BAT1</sub> -0.5V	I <sub>CC2</sub>	H H	H H .	100	μА	6,10,11

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	7-7-	7 7:	5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

(0°C to 70°C, V<sub>CCI</sub> = 4.75 to 5.5V, Pin 3 = GND) (0°C to 70°C, V<sub>CCI</sub> = 4.5 to 5.5V, Pin 3 = V<sub>CCO</sub>)

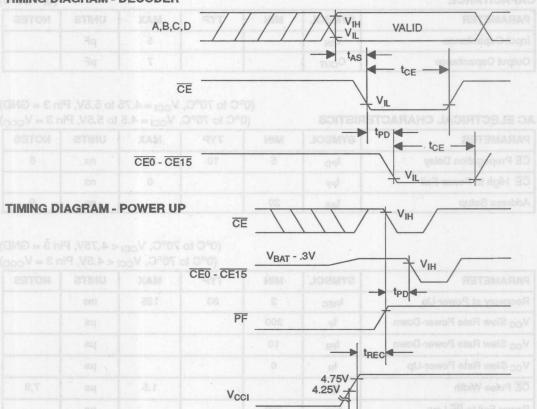
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	5
CE High to Power Fail	t <sub>PF</sub>			0	ns	
Address Setup	t <sub>AS</sub>	20		III gangro	ns	9

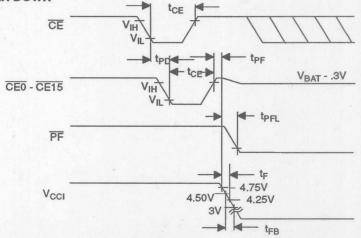
(0°C to 70°C,  $V_{CCI}$  < 4.75V, Pin 3 = GND) (0°C to 70°C,  $V_{CCI}$  < 4.5V, Pin 3 =  $V_{CCO}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	tREC	2	80	125	ms	
V <sub>CC</sub> Slew Rate Power-Down	t <sub>F</sub>	300	14		μѕ	- Edition
V <sub>CC</sub> Slew Rate Power-Down	t <sub>FB</sub>	10			μs	
V <sub>CC</sub> Slew Rate Power-Up	t <sub>R</sub>	0			μѕ	
CE Pulse Width	t <sub>CE</sub>		. Sv	1.5	μs	7,8
Power Fail to PF Low	tpFL	300			μѕ	

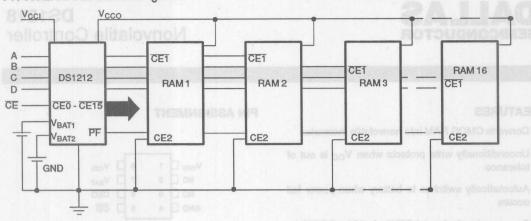
#### **TIMING DIAGRAM - DECODER**



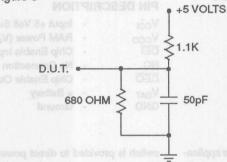
#### **TIMING DIAGRAM - POWER DOWN**



## **TYPICAL APPLICATION Figure 2**



**OUTPUT LOAD** Figure 3



### NOTES:

- 1. All voltages referenced to ground.
- 2. Only one battery input is required.
- 3. Measured with V<sub>CCO</sub> and CE0-CE15 open.
- 4. I<sub>CC01</sub> is the maximum average load which the DS1212 can supply to the memories.
- 5. Measured with a load as shown in Figure 3.
- I<sub>CC02</sub> is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
- 7. Chip enable outputs CE0-CE15 can only sustain leakage current in the battery backup mode.
- 8. t<sub>CE</sub> max. must be met to ensure data integrity on power loss.
- 9. t<sub>AS</sub> is only required to keep the decoder outputs glitch-free. While CE is low, the outputs (CE0-CE15) will be defined by inputs A through D with a propagation delay of t<sub>PD</sub> from an A through D input change.
- For applications where higher currents are required, please see the Battery Manager chip data sheet (DS1259).
- 11. The DS1212 has a 5K ohm resistor is series with the battery input. As current from the battery increases over  $100 \,\mu\text{A}$ , the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path.

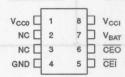


# DS1218 Nonvolatile Controller

### **FEATURES**

- Converts CMOS RAM into nonvolatile memories
- Unconditionally write protects when V<sub>CC</sub> is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin mini-DIP/8-pin 150 mil SOIC
- · Consumes less than 100 na of battery current

### **PIN ASSIGNMENT**



### **PIN DESCRIPTION**

V <sub>CCI</sub>	- Input +5 Volt Supply
Vcco	- RAM Power (V <sub>CC</sub> ) Supply
CEI	- Chip Enable Input
NC	- No Connection
CEO	- Chip Enable Output
VBAT	- + Battery
GND	- Ground

### DESCRIPTION

The DS1218 is a CMOS circuit which solves the application problems of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable output is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1218 nonvolatile controller chip with a full CMOS memory and lithium batteries, ten years of nonvolatile RAM operation can be achieved.

### **OPERATION**

The DS1218 Nonvolatile Controller performs the circuit functions required to battery back up a RAM. First, a

switch is provided to direct power from the battery or  $V_{CCI}$  supply depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1218 constantly monitors the  $V_{CC}$  supply. When  $V_{CCI}$  falls to 1.26 times the battery voltage a precision comparator outputs a power fail detect signal to the chip enable logic. The third function of write protection is accomplished by holding the chip enable output signal to within 0.2V of the  $V_{CCI}$  or battery supply, when a power fail condition is detected.

During nominal supply conditions, the chip enable output will follow chip enable input with a maximum propagation delay of 10 ns.

## **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to 7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

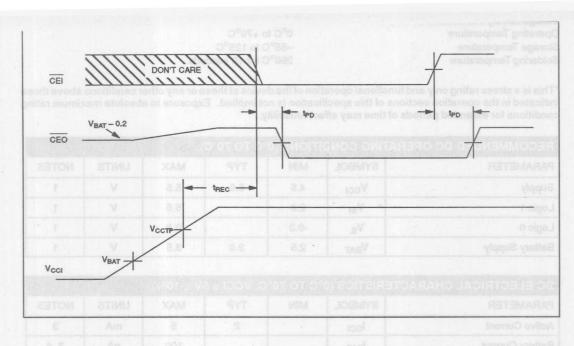
\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

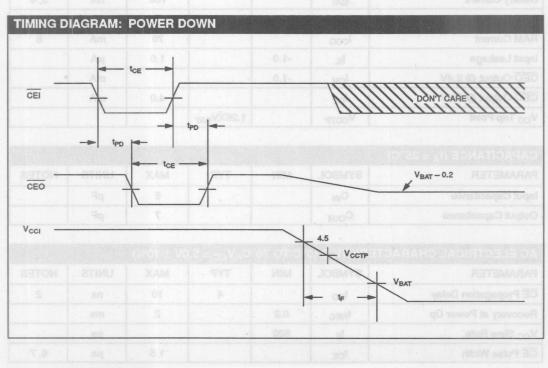
RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Supply	V <sub>CCI</sub>	4.5	5.0	5.5	V	1		
Logic 1	V <sub>IH</sub>	2.0		5.5	V	1		
Logic 0	V <sub>IL</sub>	-0.3		0.8	V	1		
Battery Supply	V <sub>BAT</sub>	2.5	3.0	3.5	V	1		

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, VCCI = 5V $\pm$ 10%)							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Active Current	Icci		2	5	mA	3	
Battery Current	IBAT			100	nA	3, 4	
RAM Supply	V <sub>CCO</sub>	V <sub>CC</sub> -0.2		1 sawos	V	a saldini	
RAM Current	Icco			70	mA	5	
Input Leakage	I <sub>IL</sub>	-1.0		1.0	μА	7	
CEO Output @ 2.4V	ГОН	-1.0		3	mA	QL.	
CEO Output @ 0.4V	loL			4.0	mA	ED	
V <sub>CC</sub> Trip Point	V <sub>CCTP</sub>		1.26XV <sub>BAT</sub>	1			

CAPACITANCE (t <sub>A</sub> = 25	°C)					
PARAMETER SO-100	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		7.	5 /	pF	0,50
Output Capacitance	C <sub>OUT</sub>			7	pF	

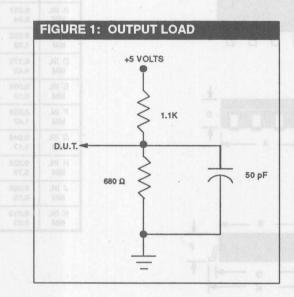
AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, $V_{CC}$ = 5.0V $\pm$ 10%)								
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
CE Propagation Delay	t <sub>PD</sub>		4	10	ns	2		
Recovery at Power Up	t <sub>REC</sub> ·	0.2		2	ms			
V <sub>CC</sub> Slew Rate	t <sub>F</sub>	500			μs			
CE Pulse Width	t <sub>CE</sub>			1.5	μs	6, 7		





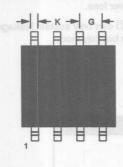
### NOTES

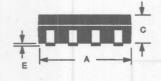
- 1. All voltages referenced to ground.
- 2. Measured with a load as shown in Figure 1.
- 3. Outputs open
- 4. Drain from battery when V<sub>CC</sub> < V<sub>BAT</sub>.
- Maximum amount of current which can be drawn through pin 1 of the controller.
- t<sub>CE</sub> max must be met to ensure data integrity on power loss.
- CEO can only sustain leakage current in the battery backup mode.

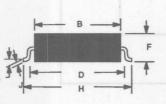


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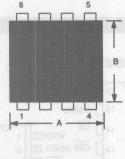
# DS1218S NONVOLATILE CONTROLLER 8-PIN 150 MIL SOIC

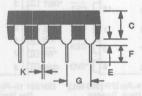


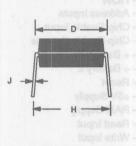




PKG	8-PIN					
DIM	MIN	MAX				
A IN.	0.188	0.195				
MM	4.78	4.95				
B IN.	0.051	0.157				
MM	3.84	3.99				
C IN.	0.052 1.32	0.061 1.55				
D IN.	0.175	0.193				
MM	4.45	4.90				
E IN.	0.004	0.010				
MM	0.10	0.25				
F IN.	0.058	0.068				
MM	1.47	1.73				
G IN.	0.046 1.17	0.054 1.37				
H IN.	0.228 5.79	0.244 6.20				
J IN.	0.006	0.011				
MM	0.15	0.28				
K IN.	0.013 0.33	0.019 0.48				







PKG	8-P	8-PIN			
DIM	MIN	MAX			
A IN. MM	0.345 8.76	0.400 10.16			
B IN. MM	0.240 6.10	0.260 6.60			
C IN.	0.120 3.05	0.140 3.56			
D IN. MM	0.290 7.37	0.310 7.87			
E IN. MM	0.015 0.38	0.040			
F IN. MM	0.110 2.79	0.130 3.30			
G IN. MM	0.090	0.110 2.79			
H IN. MM	0.320 8.13	0.370 9.4			
J IN. MM	0.008 0.20	0.012			
K IN.	0.015 0.38	0,021			

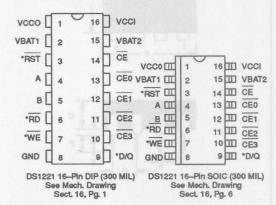


# DS1221/S Nonvolatile Controller x 4 Chip

### **FEATURES**

- Converts CMOS RAMs into nonvolatile memories
- Data is automatically protected during power loss
- 2-to-4 decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power-up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves PC board space
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C available

### **PIN ASSIGNMENT**



#### **PIN DESCRIPTION**

A, B	- Address Inputs
CE	- Chip Enable Input
CE0 - CE3	- Chip Enable Outputs
V <sub>BAT1</sub>	- + Battery 1
V <sub>BAT2</sub>	- + Battery 2
*RST	- Reset
V <sub>CCI</sub>	- +5V Supply
Vcco	- RAM Supply
*RD	- Read Input
*WE	- Write Input
*D/Q	- Data Input/Output

\*Used with optional security circuit only and must be connected to ground in all other cases.

### DESCRIPTION

The DS1221 Nonvolatile Controller x 4 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unau-

thorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, nonvolatile operation can be achieved.

### CONTROLLER /DECODER OPERATION

The DS1221 nonvolatile controller performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2-to-4 decoder provides selection of one of four RAMs (see Figure 1). Second, a switch is provided to direct power from the battery or V<sub>CCI</sub> supply, depending on which is greater, to the V<sub>CCO</sub> pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller provides is power-fail detection. The DS1221 constantly monitors the V<sub>CCI</sub> supply. When V<sub>CCI</sub> falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables (CE0 through CE3). The fourth function of write protection is accomplished by holding all chip enable outputs (CE0 through CE3) to within 0.2 volts of V<sub>CCI</sub> or battery supply. If the Chip Enable Input (CE) is low at the time power-fail detection occurs, the chip enable outputs are kept in their present state until CE is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2-to-4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data

loss. Each time that V<sub>CCI</sub> power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery back-up operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

### **NONVOLATILE CONTROLLER/DECODER Figure 1**

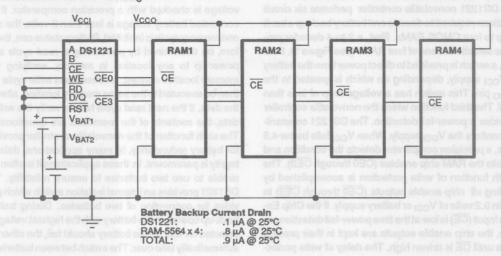
FIE 3 A		INPUTS	e 7.U.O		OUT	OUTPUTS	
V <sub>CCI</sub>	CE	В	A	CE0	CE1	CE2	CE3
>=4.5	Н	X	X	Н	Н	Н	Н
< 4.25	Х	X	X	Н	Н	Н	Н
>=4.5	- L	L	L	L	H	H	Н
>=4.5	L	L	Н	Н	L	Н	Н
>=4.5	L	Н	L	Н	Н	L	Н
>=4.5	L	Н	Н	Н	H	Н	L

H = High Level

L = Low Level

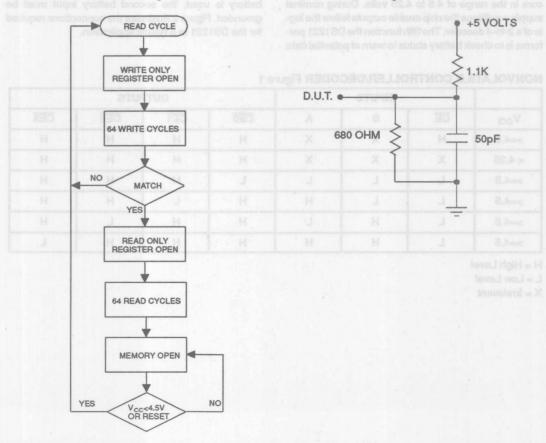
X = Irrelevant

### **TYPICAL APPLICATION Figure 2**



### **SECURITY SEQUENCE** Figure 3

### **OUTPUT LOAD** Figure 4



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature
Soldering Temperature
Short Circuit Output Current

-0.3V to +7.0V
0°C to 70°C
-55°C to +125°C
260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Logic 1 Input	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	1
Logic 0 Input	V <sub>IL</sub>	-0.3	i noanu	+0.8	٧	THINKE
Battery Input	V <sub>BAT1</sub> V <sub>BAT2</sub>	2.0	tees .	4.0	qu V <sub>wo</sub> q	1,2

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub>= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icci		1 301	5	mA	/ 3
Supply Voltage	Vcco	V <sub>CC</sub> -0.2			V	1
Supply Current	I <sub>CCO1</sub>			80	mA	4, 10
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μА	agatlov IIA
Output Leakage	ILO	-1.0		+1.0	μА	d ene yinC
CE0-CE3, DQ Output @ 2.4V	Іон	-1.0	nego	EO - 0EO br	mA	5
CE0-CE3, DQ Output @ 0.4V	loL	1221 can se	anich ma us	4.0	mA	5
V <sub>CC</sub> Trip Point	V <sub>CCTP</sub>	4.25	4.37	4.50	٧	1

(0°C to 70°C, V<sub>CC</sub>< 4.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE0-CE3 Output	V <sub>OHL</sub>	V <sub>CC</sub> -0.2 V <sub>BAT</sub> -0.2	negray on der outputs	ne decire	of bodupa	os mayor as is only
V <sub>BAT1</sub> or V <sub>BAT2</sub> Battery Current	I <sub>BAT</sub>	HAR GOLD IN	eu nouge.	0.1	μА	3
Battery Backup Current @ V <sub>CCO</sub> = V <sub>BAT</sub> - 0.5V	I <sub>CCO2</sub>		401000	100	μА	6, 7, 10

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	+ 5°88-		5	pF	mel egmo
Output Capacitance	C <sub>OUT</sub>	Am 02		7	pF	ort Circuit

### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub>= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE Propagation Delay	t <sub>PD</sub>	5	10	20	ns	5
CE High to Power-Fail	t <sub>PF</sub>	T MESA	Livernie	0	ns	TORRES
Address Setup	t <sub>AS</sub>	20			ns	9

(0°C to 70°C, V<sub>CC</sub>< 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t <sub>REC</sub>	200	5	10	ms	edied jubile
V <sub>CC</sub> Slew Rate 4.5 - 4.25V	t <sub>F</sub>	300	1 - 1	3	μѕ	
V <sub>CC</sub> Slew Rate 4.25 - 3V	°O) t <sub>FB</sub>	10	STICS	RACTER	μѕ	PLECTE
V <sub>CC</sub> Slew Rate 4.25 - 4.5V	t <sub>R</sub>	0	TOBINA		μѕ	THEARIA
CE Pulse Width	t <sub>CE</sub>		lool	1.5	μѕ	7,8

### NOTES:

- 1. All voltages are referenced to ground.
- 2. Only one battery input is required.
- 3. Measured with V<sub>CCO</sub> and CE0 CE3 open.
- 4. I<sub>CCO1</sub> is the maximum average load which the DS1221 can supply to the memories.
- 5. Measured with a load as shown in Figure 4.
- I<sub>CCO2</sub> is the maximum average load current which the DS1221 can supply to the memories in the battery back-up mode.
- 7. Chip enable outputs CE0 CE3 can only sustain leakage current in the battery back-up mode.
- 8. t<sub>CE</sub> max. must be met to ensure data integrity on power loss.
- 9. t<sub>AS</sub> is only required to keep the decoder outputs glitch-free. While  $\overline{\text{CE}}$  is low, the outputs ( $\overline{\text{CE0}}$   $\overline{\text{CE3}}$ ) will be defined by inputs A and B with a propagation delay of t<sub>PD</sub> from an A or B input change.
- For applications where higher currents are required, please see the DS1259 Battery Manager Chip data sheet.

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 3). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal (WE), the chip enable signal (CE), and the data input/ output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead, a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third

part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register can be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V<sub>CC</sub> falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.

### NOTE:

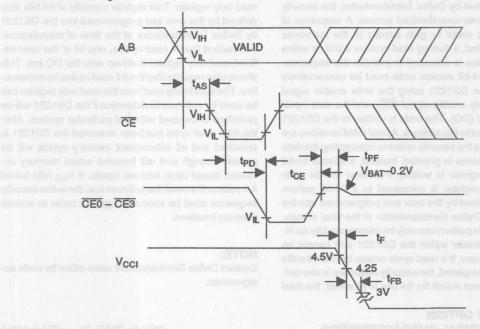
Contact Dallas Semiconductor sales office for code assignments.

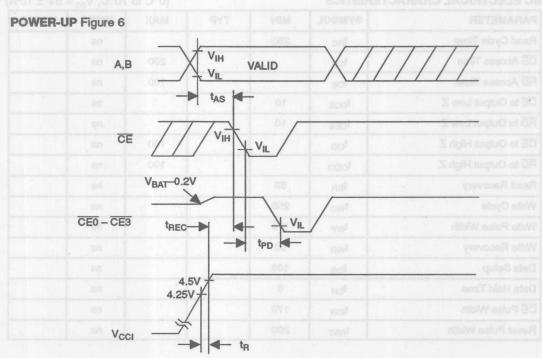
# SECURITY OPTION AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{cc} = 5\text{V} \pm 10\%)$ 

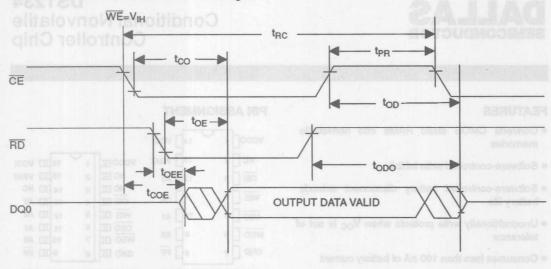
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	250	السنا		ns	
CE Access Time	tco	CILIAN	HIV D	200	A ns	
RD Access Time	t <sub>OE</sub>			100	ns	
CE to Output Low Z	tcoe	10	P GAI I		ns	
RD to Output Low Z	toee	10	KXX	7	ns	
CE to Output High Z	t <sub>OD</sub>	VaV.	Na. /	100	ns	
RD to Output High Z	topo			100	ns	
Read Recovery	t <sub>RR</sub>	50	Y Y	LO-TABV	ns	
Write Cycle	t <sub>WC</sub>	250			ns	
Write Pulse Width	t <sub>WP</sub>	170	p   44-	panf	ns	
Write Recovery	t <sub>WR</sub>	50			ns	
Data Setup	t <sub>DS</sub>	100			ns	
Data Hold Time	t <sub>DH</sub>	0	TA'S	10.0	ns	
CE Pulse Width	tcw	170			ns	
Reset Pulse Width	t <sub>RST</sub>	200		Kain .	ns	

POWER-DOWN Figure 5

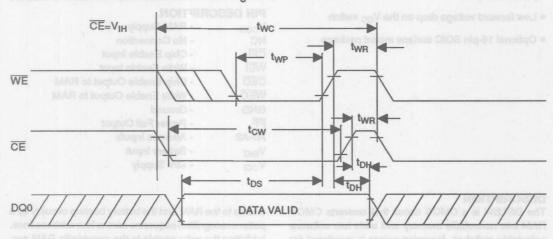




# **READ CYCLE TO SECURITY OPTION Figure 7**



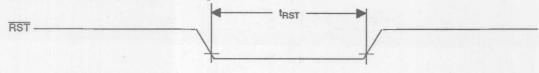
# WRITE CYCLE TO SECURITY OPTION Figure 8



### NOTES:

- 1.  $t_{DH}$  and  $t_{DS}$  are functions of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 2. t<sub>WR</sub> is a function of the latter occurring edge of WE or CE.

# **RESET FOR SECURITY OPTION** Figure 9



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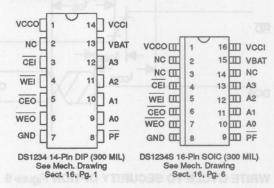


# DS1234 Conditional Nonvolatile Controller Chip

#### **FEATURES**

- Converts CMOS static RAMs into nonvolatile memories
- Software-controlled write inhibit
- Software-controlled battery disconnect extends battery life
- Unconditionally write protects when V<sub>CC</sub> is out of tolerance
- · Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V<sub>CC</sub> switch
- Optional 16-pin SOIC surface mount package

#### PIN ASSIGNMENT



#### **PIN DESCRIPTION**

Vcco	- RAM Supply	
NC	- No Connection	
CEI	- Chip Enable Input	
WEI	- Write Enable Input	
CEO	- Chip Enable Output to RAM	
WEO	- Write Enable Output to RAM	
GND	- Ground	
PF	- Power Fail Output	
A0-A3	- Address Inputs	
VBAT	- Battery Input	
V <sub>CCI</sub>	- +5V Supply	

### DESCRIPTION

The DS1234 is a CMOS circuit that converts CMOS RAM into nonvolatile memory and adds two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable and write enable to the RAM are inhibited to accomplish write protection, and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write

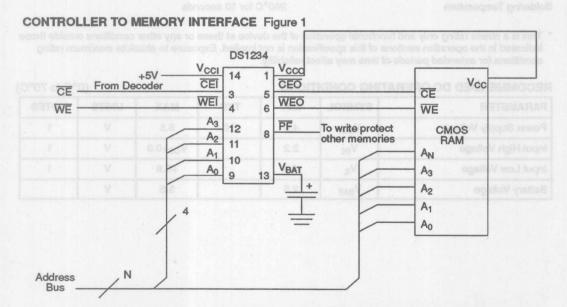
enable to the RAM and the battery backup circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery backup is not needed.

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply ( $V_{\rm COI}$ ), depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out-of-tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage,  $V_{\rm TP}$ , at which power fail is detected is defined as 1.26 times  $V_{\rm BAT}$ . The third function of write protection is accomplished by holding the CEO and WEO output signals to within 0.2 volts of the  $V_{\rm CCI}$  or battery supply.

In addition to the nonvolatile controller functions, the DS1234 supplies two software-selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence that will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer of clock zero. Each four-bit compare word

is clocked into the DS1234 on the negative edge of CEI. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven; the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch that inhibits the write enable to the RAM (WEO). A logic one in this location allows read/write operations so that WEO will follow WEI and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 thorough 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010 activates the nonvolatile controller; data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation.

At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 though 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial  $V_{\rm CC}$  power, the write enable will be set in read/write operation (WEI=WEO).



9

### **ADDRESS INPUT PATTERN** Table 1

	CYCLE NUMBER															
Address Inputs	0	1.	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A3	1	0	1	0	0	0	1	1	0	1	0			111 10 100 100		
A2 wells no	0	11	0	g1)	1	1)1	0	0	1	0	i tol	0	0	0	11.0	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	01)	0	n1 y	no1be	-1	0	0	q1a	0	irt s	0	0	0	od at	-1

### **CONTROL SELECT Table 2**

	WEIE	Battery C	ontrol	RAN is mainta	Operation
11	12	13	14	15	oi er battery supply.
0	Х	Х	X	X	Read Only Operation
e1me	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

\*Any other combination turns controller off

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Input High Voltage	V <sub>IH</sub>	2.2	· R JA	V <sub>CC</sub> +0.3	V	1
Input Low Voltage	VIL	-0.3	n oA	+0.8	V	1
Battery Voltage	V <sub>BAT</sub>	2.5		3.5	V	

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CCI</sub>=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icci	8,)		5	mA	2
Supply Current @ V <sub>CCO</sub> = V <sub>CCI</sub> - 0.2	Icco	£		80	mA	3
Input Leakage	Iμ	-1.0		+1.0	μА	IS IS
Output Leakage	I <sub>LO</sub>	-1.0	\	+1.0	μА	
Output Current @ 2.4V	Іон	-1.0			mA	4
Output Current @ 0.4V	loL			4.0	mA	4

(0°C to 70°C; V<sub>CCI</sub>=< V<sub>BAT</sub>)

(ta=25°C)

CEO, WEO Output	V <sub>OHL</sub>	V <sub>BAT</sub> -0.2		V	6
Battery Current	I <sub>BAT</sub>		0.1	μА	7
Battery Backup Current @ V <sub>CCO</sub> = V <sub>BAT</sub> - 0.3V	I <sub>CCO1</sub>	1.7.7.7.7.67.7	100	μА	5

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	MIN	111	5	pF	NOTES
Output Capacitance	C <sub>OU</sub>			7	pF	

### AC ELECTRICAL CHARACTERISTIC

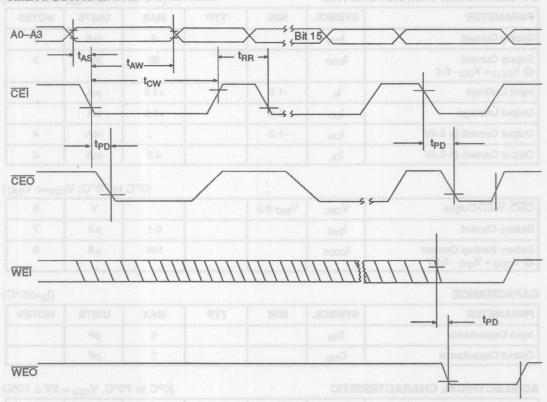
 $(0^{\circ}\text{C to } 70^{\circ}\text{C}, V_{\text{CCI}} = 5\text{V} \pm 10\%)$ 

AO ELEO IIIIOAL OIIAII	ACTEMICITY			10000	0 0, 1001.	-01 - 10.
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	tas	0	1881	OQ REWO	ns	IG DHIMI
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	40		V 160	ns	JIW .
CEI Pulse Width	tcw	110		- 31V	ns	
Propagation Delay	t <sub>PD</sub>			20	ns	

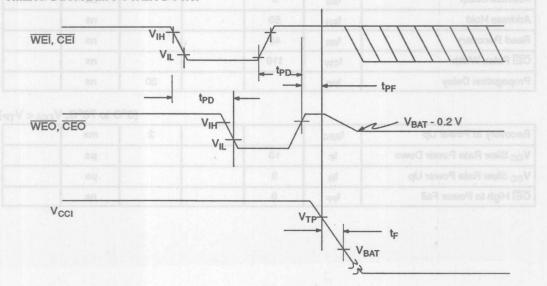
(0°C to 70°C, V<sub>CCI</sub> < V<sub>TP</sub>)

and the second s				,		001
Recovery at Power Up	tREC		X.	2	ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub>	10			μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub>	0			μs	
CEI High to Power Fail	tpF	0			ns	

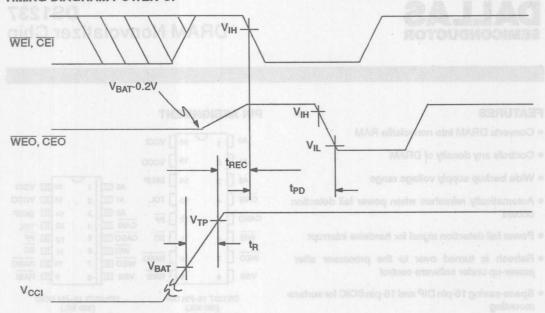
### **TIMING DIAGRAM-SWITCH SETTING**



### **TIMING DIAGRAM-POWER DOWN**



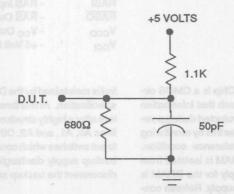
### **TIMING DIAGRAM-POWER-UP**



### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with V<sub>CCO</sub>, CEO and WEO open.
- 3. I<sub>CCO</sub> is the maximum average load that the DS1234 can supply to the memories.
- 4. Measured with a load as shown in Figure 2.
- I<sub>CC01</sub> is the maximum average load current that the DS1234 can supply to the memories in the battery backup mode.
- 6. CEO and WEO, outputs can only sustain leakage current in the battery backup mode.
- 7. IBAT is the total load current that the DS1234 uses from the battery input pin with VCCO, CEO, and WEO open.

# **OUTPUT LOAD** Figure 2



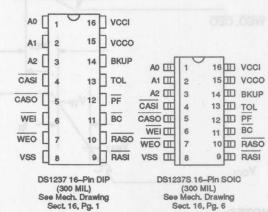


# DS1237 DRAM Nonvolatizer Chip

### **FEATURES**

- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power-up under software control
- Space-saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low-power CMOS
- Built-in backup condition circuit warns of impending backup supply failure
- Software-controlled backup supply disconnects switch for storage and shipment
- Software-controlled counter measures backup supply discharge time
- Optional refresh periods of 8 ms, 16 ms, 32 ms, and 64 ms are available to support extended refreshing at reduced power levels

### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

- Backup Supply
- Backup Condition
- V <sub>CCI</sub> Trip Point Select
- Power Fail Output
- Address Inputs
- Ground
- Write Enable Input
- Write Enable Output
- CAS Input from System
- CAS Output to DRAM
- RAS Input from System
- RAS Output to DRAM
- V <sub>CC</sub> Output to DRAM
- +5 Volt Input

### DESCRIPTION

The DS1237 DRAM Nonvolatizer Chip is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out-of-tolerance condition. When such a condition occurs, DRAM is isolated from system control and the power supply for the DRAM is switched from  $V_{\rm CC}$  to the backup supply. Refresh con-

trol is maintained by the DS1237 until the power is within specification. At this time refresh is returned to the system after a highly structured serial sequence on address lines A0, A1, and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply discharging and electrically connect or disconnect the backup supply.

# OPERATION - NORMAL POWER CONDITIONS

Under normal operation, system +5 volt power is supplied within the tolerance limits set by pin 13 (TOL). If pin 13 is connected to VCCO, the DS1237 will operate in the normal mode down to 4.75 volts. When pin 13 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the RAS, CAS, and WE inputs are directly routed to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargeable capacitor or battery; however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output (PF) is at high level and address inputs A0, A1, and A2 are monitored for software-driven sequences. The backup condition output BC will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts on V<sub>CCI</sub> and the backup counter has not reached zero.

# OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt V<sub>CC</sub> power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 13, a power fail signal will be generated as V<sub>CCI</sub> falls below 4.75 volts or 4.5 volts. At this time, the DS1237 enters a data retention mode provided that the backup supply is enabled. The power fail output signal will remain low until V<sub>CCI</sub> is restored to normal conditions. While entering the data retention mode, the DS1237 isolates all control inputs and starts driving the RAS, CAS, and WE outputs. In addition, if RAS = 1, the DS1237 immediately takes control and issues the first refresh burst 62.5 µs later. If RAS = 0, the DS1237 will wait for RAS to go to a logic 1 level and then take control and issue the first refresh burst 62.5 µs later. If RAS = 0 and remains low for more than 10 us after Power Fail Detect, the DS1237 will take control and drive RASO = 1, then issue the first refresh burst 62.5 µs later. The V<sub>CCI</sub> input is disconnected from V<sub>CCO</sub> and the regulated backup supply is connected. A burst CAS before RAS refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles, depending on the dash number of the device (see Table 1). After the burst

refresh is complete, subsequent burst refreshing continues at 8, 16, 32, or 64 ms intervals until  $V_{\rm CCI}$  returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The  $\overline{\rm WE}$  output is held at the high (inactive) level from the time control is taken by the DS1237 until the system assumes refresh duties. If the DS1237 enters a power loss condition without the backup supply enabled, no refresh activity occurs and data stored into connected DRAMs is lost.

# OPERATION – RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds the level determined by the TOL pin, the V<sub>CCI</sub> input is immediately reconnected to the V<sub>CCO</sub> output pin while the regulated backup supply is internally disconnected from V<sub>CCO</sub>. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software-controlled switch is set by sending a specific pattern on address lines A0, A1, and A2 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked, LSB first, into the DS1237 on the falling edge of CAS provided that setup and hold times are met. When the 24th cycle is correctly entered, the DS1237 will issue a final refresh burst and then return control to the host system. At this point, the host system will be responsible for handling all refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

### **ACTIVATION OF BACKUP SUPPLY**

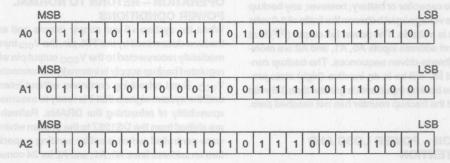
A software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. On the initial connection of the battery, the backup supply switch will be off. Under this condition, no refresh activity will occur when V<sub>CCI</sub> is out of tolerance. The bit patterns presented in Figure 2 show how the backup supply can be activated or deactivated under software control.

### **REFRESH INTERVALS Table 1**

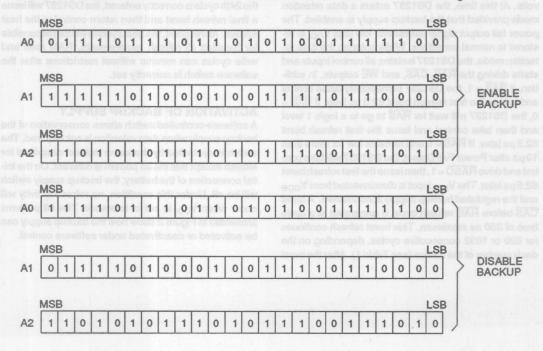
NUMBER OF CYCLES	Six Jound	REFRESH INTERVAL (ms)*					
	N.). If 8 is not dy to	16	32	64			
256K DRAM: 520	igin walls -1 mon	-2	-3	-4			
1 Meg DRAM: 1032	-5 sport	-6	17 TEST 7-11 open	-8			

<sup>\*</sup>Refresh intervals have a tolerance of ±12.5%.

# SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER-UP Figure 1



### SOFTWARE CONTROLLED SWITCH FOR ACTIVATION OF BACKUP SUPPLY Figure 2



### **BATTERY CONDITION**

The DS1237 has two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V<sub>CCI</sub>, the backup condition output pin (BC) is driven to the active state (low) and will remain in this state until the backup supply voltage is restored to a level above Vcci. This feature is active only while Vcci. is applied within nominal limits. Whenever the backup supply is supplying power, the BC pin remains at a logic 0 state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one-second intervals whenever the backup supply is supplying power. This counter is set with a number while V<sub>CCI</sub> is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1, and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when the CASI line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the BC pin will be low even though the V<sub>CCI</sub> supply is within nominal limits. The BC pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in ampere hours of the backup supply by the average load current of the DRAMs and converting this value into seconds (see Figure 5). The value in the counter can be read at any time while V<sub>CCI</sub> is within nominal limits by sending the 24-bit sequence shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 CASI cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the BC pin. A logic 0 on BC while CAS is low is a logic 0 for that bit.

### **BACKUP CONDITION APPLICATIONS**

The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the Vcc comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargeable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

#### NOTE:

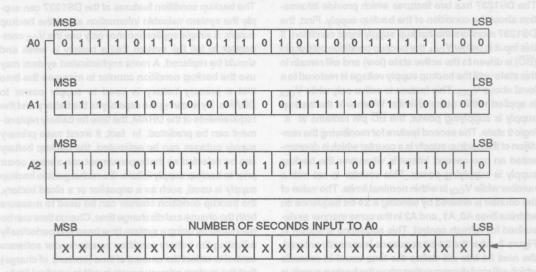
The DS1237 requires capacitive bypassing techniques between  $V_{\rm CCO}$  and GND for proper operation. A bypass capacitor between  $V_{\rm CCI}$  and BKUP is also essential for proper operation. While applications vary, a 10  $\mu$ F capacitor value is typically required.

### **DATA RETENTION TIMES**

The equations in Figure 5 are used to find the data retention time of DRAMs using the DS1237 DRAM Nonvolatizer Chip.

Calculating the actual current consumption of the DRAMs requires special attention since they are placed into the standby mode and then activated only when refreshing is required. This means that the current consumption of the DRAMs will be an average of the standby current and the active currents weighted in proportion to the refresh cycle time and duration.

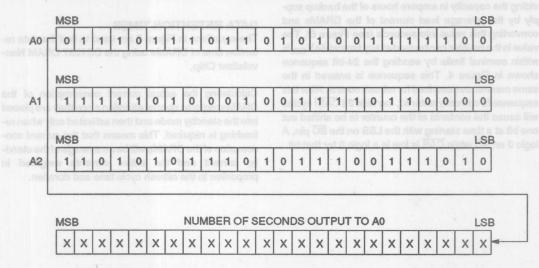
## **SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER Figure 3**



### NOTE:

The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of  $2^{24}$  seconds with an accuracy of  $\pm 20\%$ .

# SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER Figure 4



# **DS1237 NONVOLATIZER DRAM DATA RETENTION TIMES** Figure 5

I <sub>datareten</sub> = (# of DRAMs) X [ (I <sub>act</sub> + I <sub>std</sub> ) / 8E–3 ] + 4 mA	I <sub>std</sub> = (8E-3 - (520 X 350E-9)) X I <sub>standby</sub> 8E-3 => refresh period
where,	520 => number of refresh cycles (burst)
I <sub>act</sub> = 520 X 350E–9 X I <sub>active</sub> 520 => number of refresh cycles	350E-9=> access cycle time of DRAM, and
(burst) 350E-9=> access cycle time of DRAM,	I <sub>standby</sub> => standby current draw of DRAM  The foregoing equations can then be used to directly
and lactive => active current draw of DRAM	calculate the data retention time:
40070	t <sub>datareten</sub> = Q <sub>bat</sub> / I <sub>datareten</sub>

## **ABSOLUTE MAXIMUM RATINGS \***

Voltage on Battery Input Pin Relative To Ground Voltage on any Other Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +12V -0.3V to +7V 0°C to +70°C -55°C to +125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>CCI</sub>	4.5	5.0	5.5	V	1
Voltage Input Logic 1	V <sub>IH</sub>	2.0	BAPTER TO	V <sub>CC</sub> +0.3V	V	Hast I
Voltage Input Logic 0	V <sub>IL</sub>	-0.3		+0.8	٧	1
Backup Supply	BKUP	6.0V	8.0V	10.0	٧	2,3

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 4.50\text{V to }5.5\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-1.0		+1.0	μА	
Output Current @ 2.4V	l <sub>OH</sub>	-2.0		1/	mA	1,5
Output Current @ 0.4 V	loL	+8.0			mA	1,5
Input Supply Current	Icci		3	7	mA	6
Output Supply Current V <sub>CCO</sub> =V <sub>CCI</sub> -0.2 V	Icco			200	mA	4
PF Detect TOL = V <sub>CCO</sub>	V <sub>TP</sub>	4.5	4.62	4.75	V	7
PF Detect TOL = GND	V <sub>TP</sub>	4.25	4.37	4.5	V	7
Output Supply Current V <sub>CCI</sub> < V <sub>TP</sub>	Іссов			30	mA	8
Backup Supply Leakage	I <sub>BKUP</sub>			1	μА	9

CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	5	7	1 + psl) ] X-	pF	nelmakar

AC ELECTRICAL CHARACTERISTICS - RAPID REFRESH

(0°C to 70°C, V<sub>CCI</sub> < V<sub>TP</sub>)

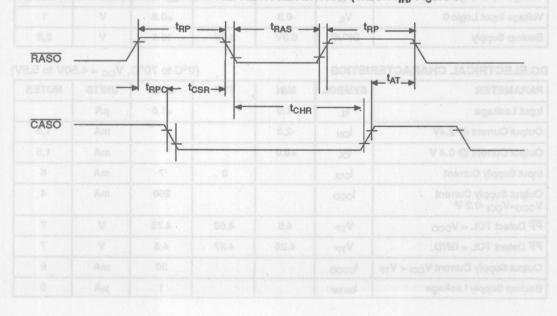
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RASO Precharge Time	t <sub>RP</sub>	90	MARG to	nii elovo sas	ns	380
RASO Precharge to CASO Hold Time	t <sub>RPC</sub>	60	MASIC to va	ob inemo e	ns	time stoal
CASO Setup Time	tcsR	30			ns	
CASO Hold Time	t <sub>CHR</sub>	60		DHITARIM	ns	rujosi
RASO Pulse Width	t <sub>RAS</sub>	0.120	bnuorië) d	10	μѕ	lage on B
Elapsed Time Between Rapid Refresh Burst	t <sub>AT</sub>	al 0°0	SEE TABLE	1	ms	erating Tel

**AC ELECTRICAL CHARACTERISTICS** 

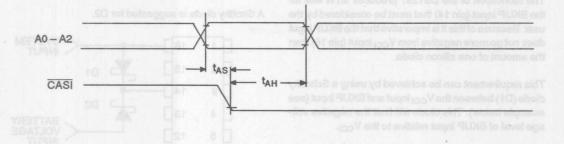
(0°C to 70°C, V<sub>CCI</sub> > V<sub>TP</sub>)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t <sub>AS</sub>	0	sette year en	periods of D	ns	enotibnoo
Address Hold Time	t <sub>AH</sub>	20	пемоо в	BTARB90	ns	ECOMMI
Propagation Delay	t <sub>PD</sub>	Mad	7	15	ns	MANAEY

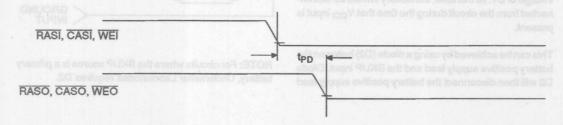
# REFRESH CYCLE DURING BURST REFRESH RETENTION (WEO=VIH) Figure 6



## SOFTWARE SEQUENCE ENTRY (WEI=VIH) Figure 7



### **PROPAGATION DELAY - NORMAL OPERATION Figure 8**



### **NOTES**

- 1. All voltages are referenced to ground.
- 2. The BC pin will be driven active whenever V<sub>CC</sub> is within nominal limits and the backup supply is below V<sub>CC</sub>.
- Backup input voltage is internally regulated within the DS1237 such that V<sub>CCO</sub> is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
- I<sub>CCO</sub> is the maximum current which the DS1237 can supply to RAM through the V<sub>CCO</sub> pin with a voltage drop of less than 0.2 volts.
- 5. Load capacity is 300 pF.
- 6. Measured with all outputs open.
- 7. V<sub>TP</sub> is the trip point where the internal switching circuits disconnect V<sub>CCI</sub> and connect the internally regulated backup supply to V<sub>CCO</sub>. Rapid refresh is also initiated at this time, and the PF output is driven active.
- 8. I<sub>CCOB</sub> is the maximum current the DS1237 can supply to RAM through the V<sub>CCO</sub> pin from the internally regulated supply while in the data retention mode.
- Backup leakage is the internal current consumed by the DS1237 in the data retention mode, with battery backup disabled.

9

# APPLICATION NOTE: DIODE CONTROL OF BACKUP INPUT

The fabrication of the DS1237 produces an N well for the BKUP input (pin 14) that must be considered by the user. Because of this it is imperative that the BKUP input does not go more negative from V<sub>CCI</sub> input (pin 16) than the amount of one silicon diode.

This requirement can be achieved by using a Schottky diode (D1) between the V<sub>CCI</sub> input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V<sub>CCI</sub>.

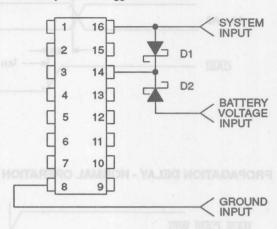
A Shottky diode is required for D1.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V<sub>CCI</sub> input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive supply lead

from the BKUP input when the battery output voltage has decreased.

A Shottky diode is suggested for D2.



**NOTE:** For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.

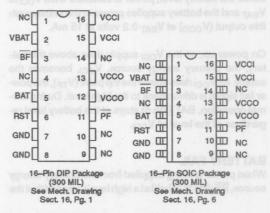
# DALLAS

# DS1259 Battery Manager Chip

### **FEATURES**

- Facilitates uninterruptible power
- Uses battery only when primary V<sub>CC</sub> is not available
- Low forward voltage drop
- Powerfail signal interrupts processor or write protects memory
- · Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V<sub>CC</sub> is applied
- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

### **PIN ASSIGNMENT**



### **PIN DESCRIPTION**

NC	- No Connection
VBAT	- Battery Input Connection
BF	- Battery Fail Output Signa
BAT	- Battery Output
RST	- Reset Input
GND	- Ground
PF	- Power Fail Output Signal
Vcco	- RAM Supply
Vcci	- +5V Supply

#### DESCRIPTION

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V<sub>CCO</sub> pins. When power is supplied from the bat-

tery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

### **OPERATION**

During normal operation,  $V_{CCI}$  (Pins 15 and 16) is the primary energy source and power is supplied to  $V_{CCO}$  (Pins 12 and 13) through an internal switch at a voltage level of  $V_{CCI}$ -0.2 volts at 250 mA. During this time the power fail signal ( $\overline{PF}$ ) is held high, indicating valid  $V_{CCI}$  voltage (see Figure 1). However, if the  $V_{CCI}$  falls below the trip point ( $V_{TP}$ ), a level of 1.26 times the battery level ( $V_{BAT}$ ), the power fail signal is driven low. As  $V_{CCI}$  falls below the battery level, power is switched from  $V_{CCI}$  to  $V_{BAT}$  and the battery supplies power to the uninterruptible output ( $V_{CCO}$ ) at  $V_{BAT}$ -0.2 volts at 15 mA.

On power-up, as the  $V_{CCI}$  supply rises above the battery, the primary energy source,  $V_{CCI}$ , becomes the supply. As  $V_{CCI}$  rises above the trip point ( $V_{TP}$ ), the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level regardless of the level of  $V_{CCI}$ .

### BATTERY FAIL

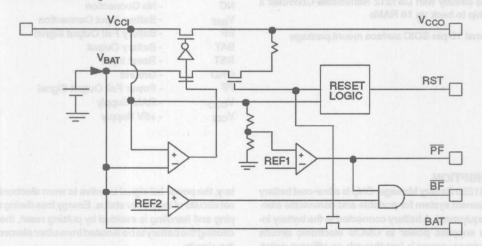
When power is being supplied from the primary energy source, BF (Pin 3) is held at a high level provided that the

attached battery ( $V_{BAT}$ ) is greater than 2 volts. If the battery level should decrease to below 2 volts, the  $\overline{BF}$  signal is driven low, indicating a low battery. The  $\overline{BF}$  signal is always low when the  $\overline{PF}$  signal is low.

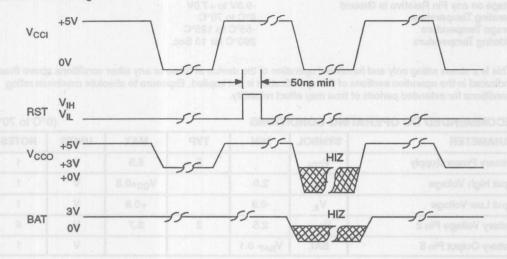
### RESET

The reset input can be used to prevent the battery from supplying power to  $V_{CCO}$  and BAT even if  $V_{CCI}$  falls below the level of the battery. This feature is activated by applying a pulsed input on RST to high level for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the  $V_{CCO}$  output and BAT will go to high impedance. The next time primary power is applied such that  $V_{CCI}$  is greater than  $V_{BAT}$ , normal operation resumes and  $V_{CCO}$  will be supplied by the battery or  $V_{CCI}$ . The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

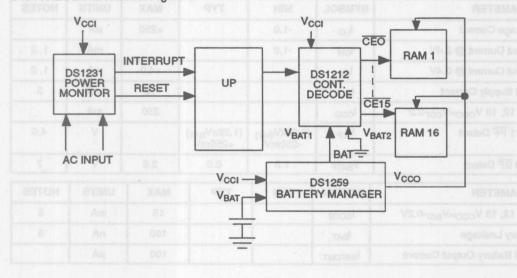
### **BLOCK DIAGRAM** Figure 1



### **RESET TIMING Figure 2**



# **TYPICAL APPLICATION Figure 3**



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to 70°C -55°C to 125°C 260°C for 10 Sec.

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>CCI</sub>		5	5.5	Vs+	1
Input High Voltage	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3		+0.8	V	1
Battery Voltage Pin 2	V <sub>BAT</sub>	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	V <sub>BAT</sub> - 0.1			V	1

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}; V_{\text{CC}} = 4.5 \text{ to } 5.5\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	ILO	-1.0		+250	μА	
Output Current @ 2.4V	Іон	-1.0			mA	1,2
Output Current @ 0.4V	loL	7		+4.0	mA	1,2
Input Supply Current	Icci	a l	455-	10	mA	3
Pins 12, 13 V <sub>CCO</sub> =V <sub>CCI</sub> -0.2	Icco			250	mA	
Pin 11 PF Detect	V <sub>TP</sub>	(1.26xV <sub>BAT)</sub> -250mV	(1.26xV <sub>BAT</sub> ) +250mV		٧	4,6
Pin 3 BF Detect	V <sub>BATF</sub>	1.5	2.0	2.6	V	7

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pins 12, 13 V <sub>CCO</sub> =V <sub>BAT</sub> -0.2V	I <sub>CCO2</sub>			15	mA	5
Battery Leakage	I <sub>BAT</sub>		1	100	nA	8
Pin 5 Battery Output Current	IBATOUT		-	100	μА	

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

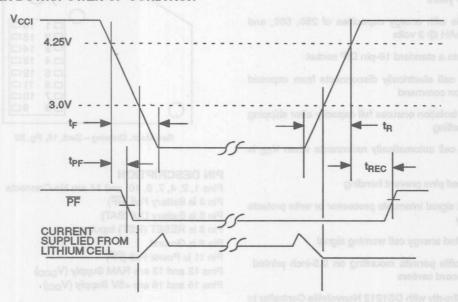
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Output Capacitance	C <sub>OUT</sub>		5	10	pF	

### AC ELECTRICAL CHARACTERISTICS

(0	°C	to	709	C;	٧	CC	=	4.0	) 1	to	5.	5	V
----	----	----	-----	----	---	----	---	-----	-----	----	----	---	---

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CCI</sub> Slew Rate	t <sub>F</sub>	300		- 30	μs	COME
V <sub>CCI</sub> Slew Rate	t <sub>R</sub>	1			μѕ	
Power-Down to PF Low	tpF	0	a francisco		μs	
PF High after Power-Up	t <sub>REC</sub>	A ROMANIA		100	μs	9

### POWER-DOWN/POWER-UP CONDITION



### NOTES:

- 1. All voltages are referenced to ground.
- 2. Load capacity is 50 pF.
- 3. Measured with Pins 11, 12, 13, and 3 open.
- 4. V<sub>TP</sub> is the point that PF is driven low.
- 5. ICCO2 may be limited by the capability of the battery.
- 6. Trip Point Voltage for Power Fail Detect:  $V_{TP} = 1.26 \times V_{BAT} \pm 250 \text{ mV}$  For 5% operation:  $V_{BAT} = 3.7 \text{V max}$ . For 10% operation:  $V_{BAT} = 3.5 \text{ V max}$ .
- 7. V<sub>BATF</sub> is the point that BF is driven low. These limits are for 0°C to 70°C operation.
- 8. Battery leakage is the internal energy consumed by the DS1259.
- 9. V<sub>CC</sub> = +5 volts, t<sub>A</sub> = 25°C.

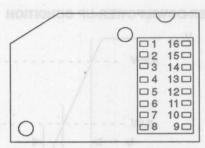


DS1260 Smart Battery

### **FEATURES**

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 mAH @ 3 volts
- Plugs into a standard 16-pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation ensures full capacity after shipping and handling
- Lithium cell automatically reconnects when V<sub>CC</sub> is applied
- · Recessed pins prevent bending
- V<sub>CC</sub> fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5-inch printed circuit board centers
- Mates directly with DS1212 Nonvolatile Controller to back up 16 SRAMs
- Uninterruptible supply for CMOS and portable devices

### **PIN ASSIGNMENT**



See Mech. Drawing - Sect. 16, Pg. 20

### PIN DESCRIPTION

Pins 1, 2, 4, 7, 9, 10, and 14 are No-Connects
Pin 3 is Battery Fail (BF)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST) Input
Pin 8 is Ground
Pin 11 is Power Fail (PF)
Pins 12 and 13 are RAM Supply (V<sub>CCO</sub>)
Pins 15 and 16 are +5V Supply (V<sub>CCI</sub>)

#### DESCRIPTION

The DS1260 SmartBattery is a low-cost, backup energy supply for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic

(RESET) circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin, low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

### **OPERATION**

During normal operation  $V_{CCI}$  (pins 15 and 16) is the primary energy source and power is supplied to  $V_{CCO}$  (pins 12 and 13) through an internal switch at a voltage level of  $V_{CCI}$ -0.2 volts @ 250 mA. During this time the power fail signal ( $\overline{PF}$ ) is held high, indicating valid primary voltage (see Figure 1). However, if the  $V_{CCI}$  falls below the level of 4.25 volts, the power fail signal is driven low. As  $V_{CCI}$  falls below the level of the lithium supply ( $V_{BAT}$  = 3 volts), power is switched and the lithium energy source supplies power to the uninterruptible output ( $V_{CCO}$ ) at  $V_{BAT}$ -0.2 volts @ 5 mA.

On power-up, as the  $V_{CCI}$  supply rises above 3 volts, the primary energy source,  $V_{CCI}$ , becomes the supply. As the  $V_{CCI}$  input rises above 4.25 volts, the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of  $V_{CCI}$ .

### **BATTERY FAIL**

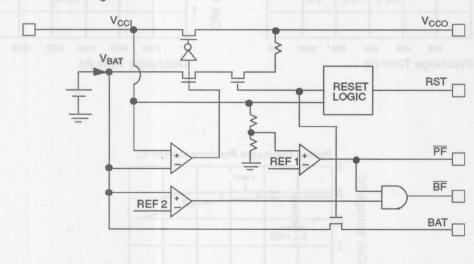
When power is being supplied from the primary energy source, BF (Pin 3) is held at a high level (V<sub>OH</sub>) provided

that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the  $\overline{BF}$  signal is driven low (V<sub>OL</sub>), indicating an exhausted lithium battery. The  $\overline{BF}$  signal is always low when power is being supplied by the lithium energy source.

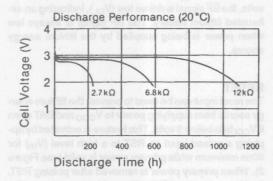
### RESET

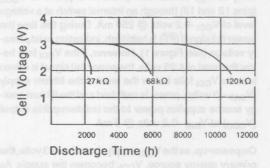
The reset input can be used to prevent the lithium energy source from supplying power to  $V_{CCO}$  and BAT even if  $V_{CCI}$  falls below 3 volts. This feature is activated by applying a pulsed input on RST to a high level ( $V_{IH}$ ) for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the  $V_{CCO}$  output and BAT will go to high impedance. The next time primary power is applied such that  $V_{CCI}$  is greater than  $V_{BAT}$ , normal operation resumes and  $V_{CCO}$  will be supplied by the lithium energy source when  $V_{CCI}$  again falls below 3 volts. BAT will also return to the level  $V_{BAT}$ . Figure 3 shows how the SmartBattery is used in a system application.

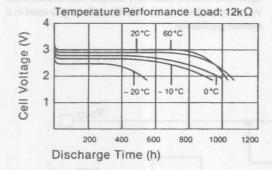
**BLOCK DIAGRAM Figure 1** 

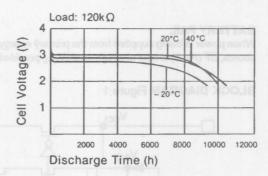


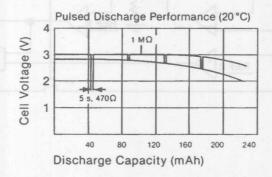
### **BATTERY PERFORMANCE DS1260-25**



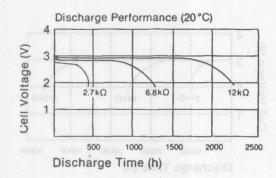


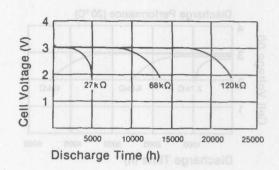


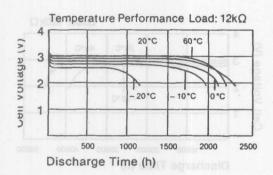


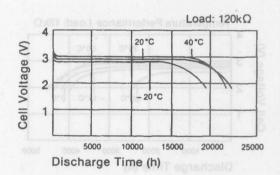


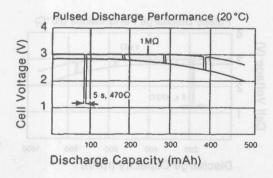
### **BATTERY PERFORMANCE DS1260-50**



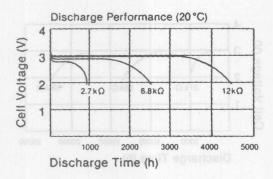


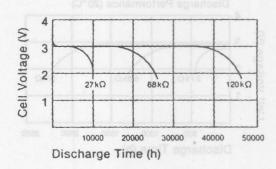


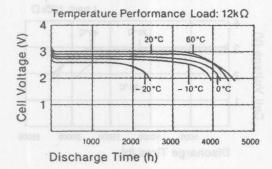


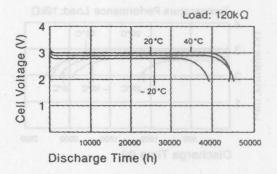


### **BATTERY PERFORMANCE DS1260-100**









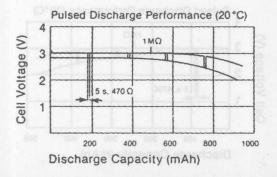
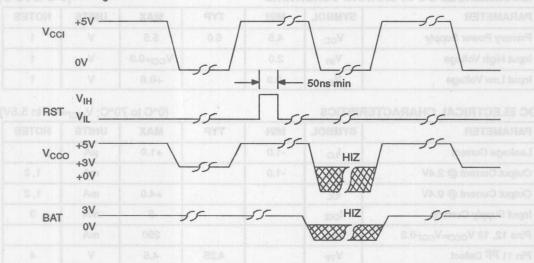


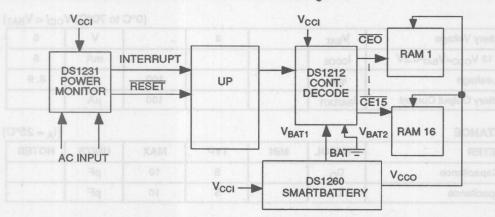
Table 1

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 mAH	3 volts
DS1260-50	480 mAH	3 volts
DS1260-100	960 mAH	3 volts

### **RESET TIMING Figure 2**



### **INTEGRATED BATTERY BACKUP - APPLICATIONS Figure 3**



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

260°C for 10 sec.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>cc</sub>	4.5	5.0	5.5	٧	1 Vee
Input High Voltage	V <sub>IH</sub>	2.0	1	V <sub>CCI</sub> +0.3	V <sub>V0</sub>	1
Input Low Voltage	V <sub>IL</sub>	-0.3	-	+0.8	V	1

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CCI</sub>=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	ILO	-1.0	\	+1.0	μА	Voo
Output Current @ 2.4V	l <sub>OH</sub>	-1.0			mA	1,2
Output Current @ 0.4V	l <sub>OL</sub>			+4.0	mA	1,2
Input Supply Current	Icci			5	mA	AE 3
Pins 12, 13 V <sub>CCO</sub> =V <sub>CCI</sub> -0.2	Icco			250	mA	
Pin 11 PF Detect	V <sub>TP</sub>		4.25	4.5	V	4
Pin 3 BF Detect	V <sub>BATF</sub>	aucurse	2.0	MAR VO	V	7

(0°C to 70°C; V<sub>CCI</sub> < V<sub>BAT</sub>)

Pin 5 Battery Voltage	V <sub>BAT</sub>	3	10-	V	6
Pins 12, 13 V <sub>CCO</sub> =V <sub>BAT</sub> -0.2V	I <sub>CCO2</sub>		19.15	mA	5
Battery Leakage	I <sub>BAT</sub>	(QU	100	nA	8, 9
Pin 5 Battery Output Current	IBATOUT		100	μА	

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	Co		5	10	pF	
Input Capacitance	CI	AMB M	5	10	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

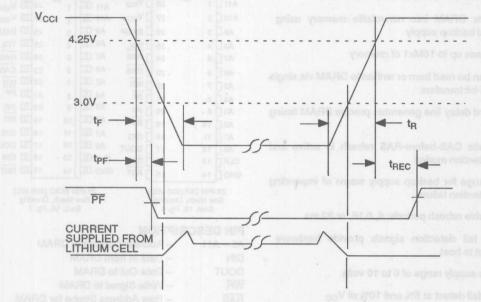
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### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CCI</sub>=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CCI</sub> Slew Rate	t <sub>F</sub>	300		R	μs	EMBCO
V <sub>CCI</sub> Slew Rate	t <sub>R</sub>	1			μs	
Power-Down to PF Low	t <sub>PF</sub>	0			μѕ	
PF High after Power-Up	t <sub>REC</sub>			100	μѕ	

### POWER-DOWN/POWER-UP CONDITION



### **WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

### NOTES:

- 1. Voltages are referenced to ground.
- 2. Load capacity is 50 pF.
- 3. Measured with Pins 11, 12, 13, and 3 open.
- 4. V<sub>TP</sub> is the point that PF is driven low.
- 5. Sustained I<sub>CCO2</sub> currents above 1 mA cause a significant drop in battery voltage.
- 6. V<sub>BAT</sub> is the internal lithium energy source voltage.
- 7. VBATE is the point that BF is driven low.
- 8. Battery leakage is the internal energy consumed by the DS1260.
- 9. Storage loss is less than 1% per year at 25°C.
- 10.  $V_{CCI} = +5 \text{ volts}; t_A = 25^{\circ}\text{C}.$



# Serial DRAM Nonvolatizer Chip

### **FEATURES**

- Provides 3-wire serial access to DRAM
- Converts DRAM into nonvolatile memory using external backup supply
- Addresses up to 16Mx1 of memory
- Data can be read from or written to DRAM via single or multi-bit transfers
- Onboard delay line generates precise DRAM timing signals
- Automatic CAS-before-RAS refresh in active and data retention modes
- Gas gauge for backup supply warns of impending data retention failure
- · Selectable refresh periods: 4, 8,16, or 32 ms
- Power fail detection signals provide hardware interrupt to host
- Backup supply range of 6 to 10 volts
- Power fail detect at 5% and 10% of V<sub>CC</sub>
- 28-pin DIP and SOIC (DS1262S) packages available

### PIN ASSIGNMENT

A11 🛚	1	28	Vcci	A11 III	1	28 🔟	Vcci
A10 [	2	27	Vcco	A10 III	2	27	
A9	3	26	BKUP	A9 III	3	26 🎹	BKUP
A8 [	4	25	TOL	A8 III	4	25 🔟	TOL
A7 [	5	24	RAS	A7 III	5	24 🞹	RAS
A6 [	6	23	CAS	A6 III	6	23 🔟	CAS
A5	7	22	WR	A5 III	7		WR
A4	8	21	PF	A4 III	8		PF
A3 T	9	20	F PF	A3 [[[	9	-	PF
A2 [	10	19	BC	A2 III	10	19 Ш	
A1	11	18	DA	A1 III	11	18 🞹	
AOT	12	17	DOUT	A0 III	12		DOUT
CLK	13	16	DIN	CLK I	13	16 🖽	
GND	14	15	RST	GND I	14	15 111	RST

28-PIN DIP (600 MIL) See Mech. Drawing Sect. 16, Pg. 4 8-PIN SOIC (330 MIL) See Mech. Drawing Sect. 16, Pg. 7

### PIN DESCRIPTION

A0 - A11 - Address Outputs to DRAM DIN - Data In from DRAM DOUT - Data Out to DRAM WR - Write Signal to DRAM RAS - Row Address Strobe for DRAM CAS - Column Address Strobe for DRAM -+5V Primary Supply VCCI - V<sub>CC</sub> Output for DRAM Vcco CLK - Serial Clock Input RST - Serial Reset Input D/Q - Serial Port Data I/O **BKUP** - Backup Supply Input TOL -5% or 10% V<sub>CC</sub> Supply Select BC - Backup Supply Condition Pin PF. PF - Power Fail Signals

### DESCRIPTION

The DS1262 Serial DRAM Nonvolatizer Chip enables read/write access of DRAM from a simple 3-wire serial port. Refresh and RAS/CAS timing for the DRAM is performed automatically, transparent to the operation of the serial port. In addition, the DS1262 performs all of the power switching and refresh duties necessary to retain

DRAM data when the primary power supply fails. The backup supply input accepts a wide voltage range, suitable for use with rechargeable batteries. The DS1262 also provides an electronic "gas gauge" which can predict the condition of the backup supply. It can be used with DRAM densities of 256Kx1 to 16Mx1.

- Ground

GND

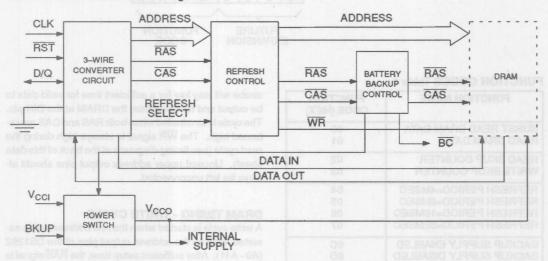
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## OPERATION – SERIAL PORT INTERFACE

The main elements of the DS1262 are shown in Figure 1. Three signals control sending or retrieval of data using the 3-wire converter circuit. The signals CLK, RST, and D/Q comprise a 3-wire serial port. To transfer data into the DS1262, RST is first driven high while CLK is low. After sufficient setup time from RST, one bit of data is placed onto the D/Q line. With valid data on D/Q the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred into the 3- wire converter. Since the serial port can only accept data one bit at a time, address information must always be sent first to inform the 3-wire converter of the destination of the data that will follow. Address information is always entered starting with the least significant bit of the logical address field and ending with the most significant bit of the address field. Twenty-four address bits are always written to the 3-wire converter regardless of the RAM being used (Figure 2).

After the 24-bit address field is sent, an 8-bit function code is written to instruct the 3-wire converter of the action to be taken on data that will follow. The function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from the DRAM or the control registers within the battery backup control unit. Function codes that control the backup supply or refresh period cause further data transfer to terminate until  $\overline{RST}$  is driven low and then high again to begin a new cycle. Data is always written in the same manner as the address and function code information. Data is read by driving the clock low while  $\overline{RST}$  is high. Data becomes valid on the D/Q line after sufficient time is allowed for access. The read cycle is terminated when  $\overline{RST}$  is returned low.

### DS1262 BLOCK DIAGRAM Figure 1



### DRAM REFRESH CONTROL

Refresh cycles are always sent to the attached DRAM, regardless of activity on the serial port. When a proper DRAM read/write access code has been entered at the serial port, a normal DRAM read/write cycle will be interlaced with the refresh burst cycles. When V<sub>CCI</sub> goes to an out-of-tolerance condition (see "DC Electrical Specifications" for details), the DS1262 sends out 258 refresh

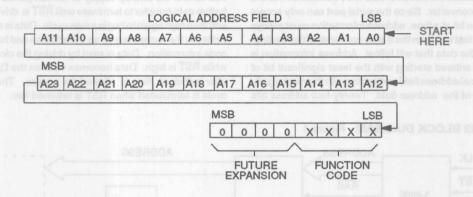
cycles for each refresh period as selected by the user (4, 8, 16, or 32 msec). The 258 refresh cycles occur at a 500 ns rate for about 129 µsec. All refresh cycles are the CAS-before-RAS type and are sufficiently long to meet the refresh requirements of most DRAM densities. After the refresh burst, the DS1262 remains quiet for the remainder of the refresh period to conserve power, except for DRAM read/write cycles initiated by the serial port.

### **BURST MODE**

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. While low density DRAMs do not require the entire 24-bit address field, 24

bits must be always entered; unused upper address bits should always be the same value (0's are recommended). The DS1262 will always produce the appropriate RAS and CAS address. Burst mode is terminated when  $\overline{\text{RST}}$  is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers

### **SERIAL PORT PROTOCOL** Figure 2



### **FUNCTION CODES Table 1**

FUNCTION NAME	FUNCTION CODE (HEX)
BURST READ DRAM DATA	00
READ DRAM DATA	01
READ BKUP COUNTER	02
WRITE BKUP COUNTER	03
REFRESH PERIOD=4MSEC	04
REFRESH PERIOD=8MSEC	05
REFRESH PERIOD=16MSEC	06
REFRESH PERIOD=32MSEC	07
BACKUP SUPPLY ENABLED	OC
BACKUP SUPPLY DISABLED	OD
WRITE DRAM DATA	0E
BURST WRITE DRAM DATA	0F,FF

### **DRAM TIMING - READ CYCLE**

A read cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the RAS signal is asserted low and the row addresses are latched into the DRAM. Next the column addresses are asserted valid and after setup time the column address strobe (CAS) goes active, latching the column address. The CAS

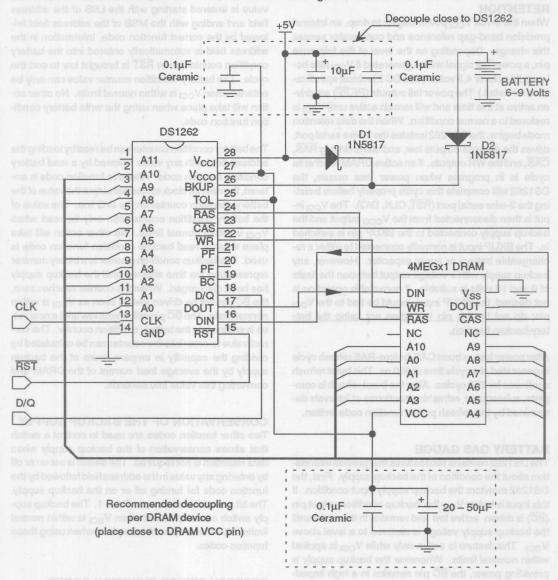
strobe will stay low for a sufficient time for valid data to be output and received from the DRAM at the DIN pin. The cycle is terminated when both RAS and CAS are returned high. The  $\overline{\rm WR}$  signal is always high during the read cycle (see timing diagrams at the back of this data sheet). Unused upper address output pins should always be left unconnected.

### **DRAM TIMING - WRITE CYCLE**

A write cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the RAS signal is asserted low and the row addresses are latched into the DRAM. At the same time, valid data is placed on the data output pin (DOUT). Next the WRITE signal is asserted low. At the same time, the column address is asserted valid on the address bus. After setup time, the CAS is asserted low.

All signals (RAS, CAS, A0-A11, WR, and DOUT) remain active and valid until the write cycle is complete. The cycle is terminated when RAS, CAS, and WR are returned back high and the data out pin (DOUT) returns to a high impedance state.

### DS1262 APPLICATION CIRCUIT WITH 4MX1 DRAM Figure 3



### NOTES:

- BKUP input must not be allowed to go 0.7 volts more negative than V<sub>CCI</sub>; otherwise an internal silicon diode in the DS1262 will short V<sub>CCI</sub> to ground. D1 clamps BKUP so that it can only go 0.3 volts below V<sub>CCI</sub>.
- D2 prevents reverse-charging of battery and may be required for UL approval if battery source is the primary source for the user's system.
- The decoupling capacitors attached to the DRAM V<sub>CC</sub> input(s) are required because of the switching noise of the regulated V<sub>CCO</sub> supply from the DS1262. Also, this capacitance satisfies fast rise-time current demands of the DRAM.

## OPERATION – POWER LOSS AND DATA RETENTION

When the 5-volt V<sub>CCI</sub> power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V<sub>CCI</sub> falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF, PF) are driven active at this time and will remain active until Vccı is restored to a normal condition. When the data retention mode begins, the DS1262 isolates the 3-wire serial port, drives the address outputs low, and starts driving RAS, CAS, and the WR outputs. If an active DRAM read/write cycle is in progress when power loss occurs, the DS1262 will complete this cycle properly before isolating the 3-wire serial port (RST, CLK, D/Q). The VCCI input is then disconnected from the V<sub>CCO</sub> output and the backup supply connected to the BKUP pin is switched in. The BKUP input is normally connected to either a rechargeable battery or super capacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be tied to the V<sub>CCI</sub> pin; do not tie this pin low when not using the battery-backup function.

After power loss, a burst CAS-before-RAS refresh cycle is generated at a cycle time of 500 ns. This burst refresh continues for 258 cycles. After the burst refresh is complete, subsequent refreshing continues at intervals determined by the refresh period function code written.

### **BATTERY GAS GAUGE**

The DS1262 contains two features that provide information about the condition of the backup supply. First, the DS1262 monitors the backup supply input condition. If this input is below  $V_{\rm CCI}$  the backup condition output pin  $(\overline{\rm BC})$  is driven active low and remains in this state until the backup supply voltage is restored to a level above  $V_{\rm CCI}$ . This feature is active only while  $V_{\rm CCI}$  is applied within nominal limits. Whenever the backup supply is providing power, the  $\overline{\rm BC}$  pin remains in a high impedance state.

The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while  $V_{\rm CCI}$  is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field,

followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field followed by the correct function code. Information in the address field is automatically entered into the battery condition counter when RST is brought low to end the cycle. The battery condition counter value can only be entered when V<sub>CCI</sub> is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V<sub>CCI</sub> is within normal limits. No other action will take place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the BC pin will be driven low as soon as V<sub>CCI</sub> is within normal limits. The BC pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

### **CONSERVATION OF THE BACKUP SUPPLY**

Two other function codes are used to control a switch that allows conservation of the backup supply when data retention is not required. The switch is set on or off by entering any value in the address field followed by the function code for turning off or on the backup supply. The bit patterns are shown in Table 1. The backup supply switch can only be set when V<sub>CCI</sub> is within normal limits. No other action will take place when using these function codes.

#### REFRESH PERIOD FUNCTION CODES

Four function codes are used to set the refresh period for the attached DRAM; all refresh periods contain 258 cycles. As such, most DRAMs will use 256 cycles per 4 msec refresh regardless of the density of the RAM attached. For example, a 1Mx1 DRAM requires 512 cycles in 8 ms while a 4Mx1 DRAM requires 1024 cycles in a 16 ms period. Both devices are satisfied using a 4 msec refresh period since a 4Mx1 DRAM is satisfied in 4

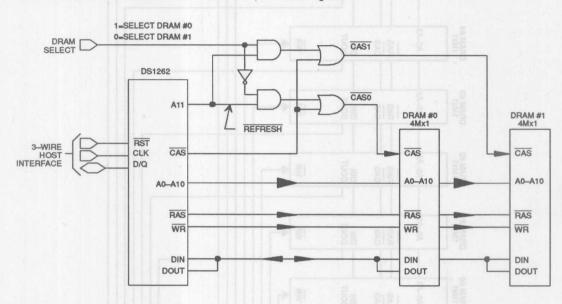
refresh periods (4 x 256 = 1024). However, extended refresh periods can be used in cases where DRAMS have been screened and tested for longer data retention between refresh bursts.

Whenever a function code is written to select the refresh period, the logic address field is ignored by the serial port and can be set to any value; however, all 24 address bits must be entered. Function codes other than proper DRAM read /write codes do not cause any data to be written to the attached DRAM; the RST pin must be

reset low and then brought high to access the DRAM data after entering these codes. Data sent through the serial port after one of these functions codes is sent will be ignored until RST is driven low and then high again to begin a new cycle.

Function codes for backup supply control or refresh control need only be written once after the BKUP supply is attached. The BKUP supply will preserve these codes as long it remains within specified limits.

### BANK SELECT SCHEME FOR TWO 4MX1 DRAMS Figure 4



### NOTES:

- 1. In this application, the A11 address output serves as a refresh indicator, going low whenever the DS1262 is in a refresh cycle. During refresh cycles, all address outputs are forced to the last row address state. Therefore, the user must program A23 = 0 and A22 = 1; that is, A23 maps to the row address output of A11 while A22 maps to the column address output of A11.
- Caution must be taken to never program A23, A22 to any state other than 01 nor to allow the DS1262 to inadvertently reach this address in the burst read/write mode.

BANK SELECT SCHEME FOR EIGHT 1MX1 DRAMS Figure 5

021492 7/11

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground

Voltage on BKUP Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

Voltage on BKUP Pin Relative to Ground

O°C to 70°C

-55°C to +125°C

260°C for 10 sec.

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V <sub>CCI</sub>	4.5	5.0	5.5	٧	anbb/q wo
Input Logic High	V <sub>IH</sub>	2.0	SBA	V <sub>CC</sub> +0.3	٧	oà nquis
Input Logic Low	V <sub>IL</sub>	-0.3	HADÍ	+0.8	V	DA najulo
Backup Supply	BKUP	5.5	8.0	10.0	V	1,2,3

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CCI</sub> = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-1.0	duct.	+1.0	μА	oute 2 SA
DQ Leakage	lLO	-1.0	ated	+1.0	μА	MS Hold
Output Current @ 2.4V	Іон	-1.0	and.		mA	1,5
Output Current @ 0.4V	l <sub>OL</sub>	2.0	and		mA	1,5
Input Supply Current	lcci	201	3.0	15	mA	6
Output Supply Current V <sub>CCO</sub> = V <sub>CCI</sub> - 0.2V	Icco	109	ogl	100	mA	4
TOL pin = V <sub>CCO</sub>	V <sub>TP</sub>	4.50	4.62	4.75	V	7
TOL pin = GND	V <sub>TP</sub>	4.25	4.37	4.50	V	7
Output Supply Current V <sub>CCI</sub> < V <sub>TP</sub>	Іссов	500	Hol	30	mA	8
Backup Supply Leakage	I <sub>BKUPL</sub>	B [	2	4	μА	9
Backup Supply Quiescent	IBKUPQ		2.0		mA	10

### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	7	pF	DIG OF 151
Output Capacitance	C <sub>OUT</sub>		7	10	pF	
I/O Capacitance	C <sub>VO</sub>		7	10	pF	1310

### AC ELECTRICAL CHARACTERISTICS

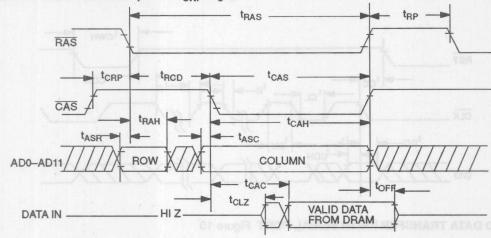
 $(t_A = 25^{\circ}C, V_{CC} = 5V \pm 5\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RAS Pulse Width	t <sub>RAS</sub>	200		350	ns	of gnutated
RAS Precharge	t <sub>RP</sub>	125		200	ns	oldering Te
CAS to RAS Precharge	t <sub>CRP</sub>	125	snago lanoi	200	ns	s e el alif.T
RAS to CAS Delay	t <sub>RCD</sub>	70	Na yam em	125	ns	enotibnes
CAS Pulse Width	t <sub>CAS</sub>	100	амоэ ан	275	ns	ECONEM
Row Address Setup	tasr	25	TOSHIA		ns	TEMARA
Row Address Hold	t <sub>RAH</sub>	25	Veres		ns	dmany Po
Column Address Setup	tasc	20	wW.		ns	oipoul tuer
Column Address Hold	tcah	100	nV		ns	placy tunn
Access Time From CAS	tcac	8.8	PAUDA	200	ns	ua guba
CAS to Output In Low Z	t <sub>CLZ</sub>				ns	1
Output Turn Off Delay	toff		80118	BIOARA	ns	2848
RAS to CAS Precharge	t <sub>RPC</sub>	20	-PUBLISTS	175	ns	T DESCRIPTION
CAS Setup Time	t <sub>CSR</sub>	10	A.	50	ns	NEON INSE
CAS Hold Time	t <sub>CHR</sub>	200	0.4	350	ns	DIVIDED I LA
Write Pulse Width	t <sub>WP</sub>	125	MOI	300	ns	maru migita
Data Setup	t <sub>DS</sub>	50	, KOL		ns	STATE STATES
Data Hold	t <sub>DH</sub>	125	1001	DIE EL	ns	ddne me
D/Q to CLK Setup	t <sub>DC</sub>	100	500 <sup>1</sup>		ns	oV a cono
CLK to D/Q Delay	t <sub>CDD</sub>	08.8	gyV	300	ns	= hig_EO
CLK Low Time	t <sub>CL</sub>	500	er-V		ns	= alg_JO
CLK High time	t <sub>CH</sub>	500	enni		ns	Sutput Sus
CLK Frequency	fclk	DC		- 1	MHz	97¥ > 100
CLK Rise & Fall	t <sub>R</sub> ,t <sub>f</sub>	3	10	20	ns	ne quinn
RST to CLK Setup	tcc	1	CHUSE!	10	μs	us quos
CLK to RST Hold	t <sub>CCH</sub>	200			ns	COMPANIE A
RST Inactive Time	t <sub>CWH</sub>	1.0	Laon	ya I	μѕ	rigues des
RST to D/Q In High Z	t <sub>CDZ</sub>			100	ns	

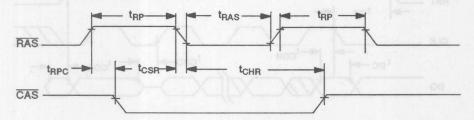
### NOTE:

1. See DRAM data sheet.

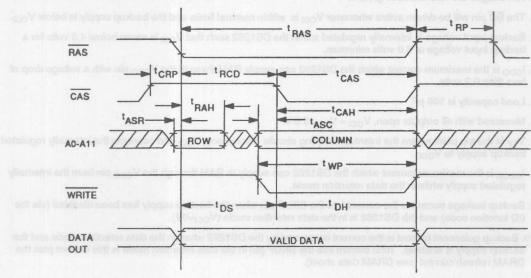
### READ CYCLE FROM RAM (WR = V<sub>OH</sub>) Figure 6



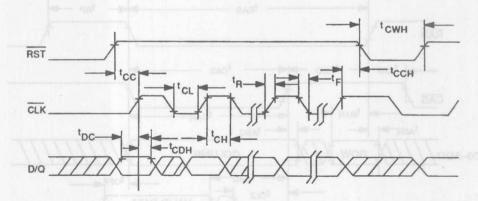
### REFRESH CYCLE (WR = VOH) Figure 7



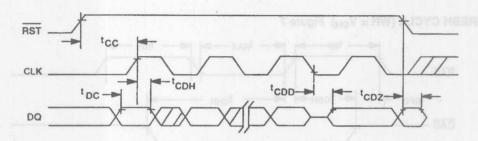
### WRITE CYCLE OUTPUT TO RAM Figure 8



### WRITE DATA TRANSFER FROM SERIAL PORT Figure 9



### **READ DATA TRANSFER FROM SERIAL PORT** Figure 10



### NOTES:

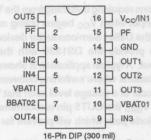
- 1. All voltages are referenced to ground.
- 2. The BC pin will be driven active whenever V<sub>CCI</sub> is within nominal limits and the backup supply is below V<sub>CCI</sub>.
- Backup input voltage is internally regulated within the DS1262 such that V<sub>CCI</sub> is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
- I<sub>CCO</sub> is the maximum current which the DS1262 can supply RAM through the V<sub>CCO</sub> pin with a voltage drop of less than 0.2 volts.
- 5. Load capacity is 100 pF.
- 6. Measured with all outputs open, V<sub>CCI</sub> = V<sub>IH</sub> = 5.5 V.
- V<sub>TP</sub> is the trip point where the internal switching circuits disconnects V<sub>CCI</sub> and connects the internally regulated backup supply to V<sub>CCO</sub>.
- I<sub>CCOB</sub> is the maximum current which the DS1262 can supply to RAM through the V<sub>CCO</sub> pin from the internally regulated supply while in the data retention mode.
- Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS1262 is in the data retention mode (V<sub>CCI</sub>=0V).
- 10. Backup quiescent current is the current consumed by the DS1262 when in the data retention mode and the backup supply is enabled. Total current into the BKUP pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

### **DS1336** Afterburner Chip

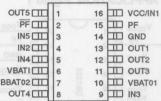
### **FEATURES**

- · Provides power switching of up to 1.5 amps at voltages between 3 and 5 volts
- Five separate power switches
- Selectable battery switches for use with battery-backed systems
- Very low on impedance of 0.7Ω
- Battery backup current of 4 mA
- Diode-isolated battery path
- Available in 16-pin DIP or 16-pin SOIC surface mount package
- Low voltage drop battery path
- · Connects directly to a variety of Dallas Semiconductor devices adding increased switching capability for large battery backup current applications

### **PIN ASSIGNMENT**



16-Pin DIP (300 mil) See Mech. Drawing - Sect. 16, Pg. 1



16-Pin SOIC (300 mil) See Mech. Drawing - Sect. 16, Pg. 6

### PIN DESCRIPTION

GND

- +5V Input and Input 1 V<sub>CC</sub>/IN1 IN2 - IN5 Inputs 2 - 5

OUT1 - 5 Outputs 1 - 5

External Battery Input VBATIN

Ground

**Diode Protected Battery Output** VBAT01 V<sub>BAT02</sub> Low Voltage Drop Battery Output

PF. PF Power Fail Inputs

### DESCRIPTION

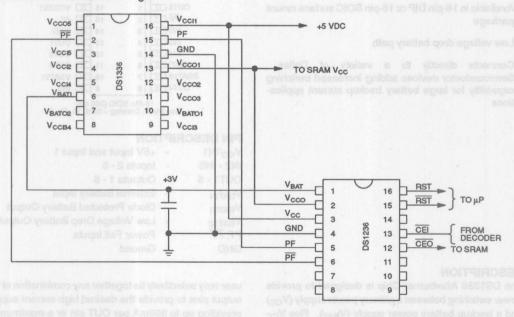
The DS1336 Afterburner Chip is designed to provide power switching between a primary power supply (V<sub>CC</sub>) and a backup battery power supply (VBAT). Five VCC and two battery paths are provided which can be used individually or in parallel to supply uninterrupted power in applications such as SRAM networks. When used with one of the Dallas power monitoring devices listed in Section 10, Page 119, Table 1, the DS1336 allows a load to be switched from its main power supply V<sub>CC</sub> to a battery backup supply when V<sub>CC</sub> falls out of tolerance. A user may selectively tie together any combination of the output pins to provide the desired high current supply, providing up to 300mA per OUT pin or a maximum of 1.5A. Depending upon the user's backup supply load requirements, either of the VBAT outputs may be tied to the OUT pins to supply current when V<sub>CC</sub> is out of tolerance. The DS1336 switches back to the higher current V<sub>CC</sub> from battery current when PF and PF become inactive.

### **OPERATION**

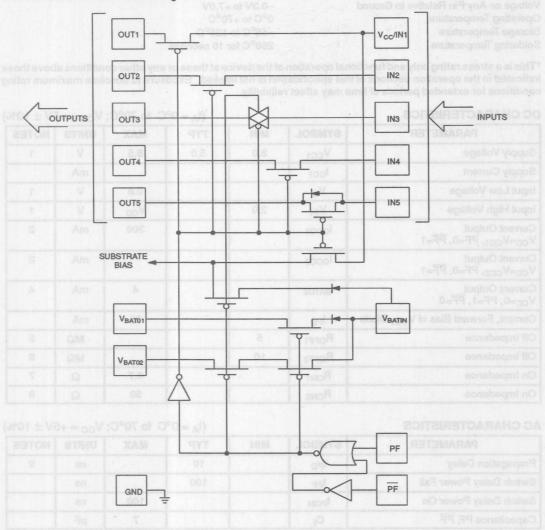
The required PF or PF input which controls the switching between the main V<sub>CC</sub> and backup battery can be supplied by any of the devices listed in Table 1. All of the devices provide the DS1336 with a PF or PF signal, switching between a main supply V<sub>CC</sub> and backup supply V<sub>BAT</sub> when V<sub>CC</sub> falls out of tolerance. For applications requiring switching from the V<sub>CC</sub> supply inputs to VBAT, the required PF or PF input to the DS1336 can be provided by the DS1236, DS1239, DS5001, or DS5340. For applications requiring switching from the V<sub>CC</sub> inputs to the VBAT input when VCC begins falling out of tolerance, any of the Dallas Semiconductor devices listed in Table 1 can provide the DS1336 with the required switching input. A typical application is shown in Figure 1. For applications where switching between V<sub>CC</sub> and V<sub>BAT</sub> must occur at a voltage level such that V<sub>CC</sub> is still greater than VBAT, the OUT5 pin is recommended as it provides a diode path which will provide for a gradual transition between  $V_{CC}$  and  $V_{BAT}$ . OUT5 can be tied to the other OUTPUT pins to provide a gradual transition for all five current paths. In applications where tri-state switching is desired, OUT5 should be omitted. Only the  $\overline{PF}/PF$  pin is required for switching. In cases where the PF input will not be used, it should be connected to GND.

When either PF or  $\overline{PF}$  is active, either of the  $V_{BAT0X}$  outputs is available, although they should not be tied together (Figure 2, "DS1336 Block Diagram").  $V_{BAT01}$  is recommended for sensitive applications such as providing backup current to timekeepers, because its diode isolated path provides for increased protection.  $V_{BAT02}$  is not recommended for applications where it would be tied to an OUTPUT pin supplying a voltage greater than that of the backup battery because  $V_{BAT02}$  is not a diode isolated current path.

### **TYPICAL APPLICATION** Figure 1



### DS1336 BLOCK DIAGRAM Figure 2



DALLAS SEMICONDUCTOR DEVICES WHICH PROVIDE PF OR PF INPUT TO DS1336 Table 1

DEVICE	SWITCH > VBAT	SWITCH AT 3.0V	DEVICE	SWITCH > V <sub>BAT</sub>	SWITCH AT 3.0V
DS1211	X		DS1239	X	X
DS1212	X		DS1259	X	NOV B FIRM SIGTAL
DS1231	X		DS1260	X	
DS1232	X		DS1610	X	and of sales
DS1234	X		DS1632	X	roma V pt zeilor
DS1236	of a mer X ry device	X X	DS5001	ley when X and as only	X coop d
DS1237	X	THE ROOD Y OF DRIE	DS5340	X	X

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground

Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### DC CHARACTERISTICS

 $(t_A = 0^{\circ}C \text{ to } 70^{\circ}C; V_{CC} = +5V \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC1</sub>	3.0	5.0	5.5	V	1
Supply Current	I <sub>CC1</sub>				mA	
Input Low Voltage	VIL			0.8	V	1
Input High Voltage	VIH	2.0		V <sub>CC</sub>	V	1
Current Output V <sub>CC</sub> =V <sub>CC1</sub> , PF=0, PF=1	I <sub>CCO1</sub>			300	mA	2
Current Output V <sub>CC</sub> =V <sub>CC2</sub> , PF=0, PF=1	I <sub>CCO2</sub>			BSTRATE BLAS	mA	2
Current Output V <sub>CC</sub> =0, PF=1, PF=0	I <sub>BATO2</sub>			4	mA	4
Current, Forward Bias of V <sub>CC5</sub> Diode	I <sub>FB</sub>		Maria	20	mA	
Off Impedance	R <sub>OFF1</sub>	5			MΩ	5
Off Impedance	R <sub>OFF2</sub>	10		Vantes	MΩ	6
On Impedance	R <sub>ON1</sub>		5 0	0.7	Ω	7
On Impedance	R <sub>ON2</sub>			50	Ω	8

### **AC CHARACTERISTICS**

 $(t_A = 0^{\circ}C \text{ to } 70^{\circ}C; V_{CC} = +5V \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay	t <sub>PD</sub>		10		ns	9
Switch Delay Power Fail	tpF		100		ns	
Switch Delay Power On	t <sub>PON</sub>			100	ns	
Capacitance PF, PF	CI			7	pF	

#### NOTES

- 1. All voltages referenced to ground.
- 2. I<sub>CCO</sub> with a voltage drop of 0.2V from any V<sub>CCO</sub> output.
- 3. IBATO1 with a voltage drop of 0.2V.
- 4. VBATO2 with a voltage drop of 1.0V.
- 5. Roff1 applies to Vcco1,2,3,4.
- 6. ROFF2 applies to VBATO1.2.
- 7. Applies to V<sub>CCO1-5</sub>, 300 mA.
- 8. Applies to VBATO1-2, 4 mA.
- V<sub>CCI3</sub> to V<sub>CCO3</sub> delay when used as chip enable control for write protection of a memory device. In this application a current 8 mA source current on V<sub>CCI3</sub> with 50 pF load on V<sub>CCO3</sub> can be accommodated.

## 9



# DS1610 Partitioned NV Controller

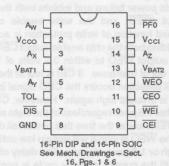
### **FEATURES**

- Converts CMOS RAMs into nonvolatile memories
- SOIC version is pin compatible with the Dallas Semiconductor DS1210 NV Controller
- Unconditionally write protects all of memory when V<sub>cc</sub> is out of tolerance
- Write protects selected blocks of memory regardless of V<sub>cc</sub> status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Provides for multiple batteries
- Consumes less than 100 nA of battery current
- Test battery on power up by inhibiting the second memory cycle
- Optional 5% or 10% Power Fail Detection
- 16-pin DIP or 16-pin SOIC Surface Mount Package
- Low forward voltage drop on the V<sub>CC</sub> switch with currents of up to 150 mA
- Optional industrial temperature range of -40°C to +85°C

#### DESCRIPTION

The DS1610 is a low power CMOS circuit which solves the application problems of converting CMOS RAMS into nonvolatile memories. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The power supply incoming voltage at the V<sub>CCI</sub> input pin is constantly monitored for an out of tolerance condition. When such a condition is detected, both the chip enable and write enable outputs are inhibited to protect stored data. The battery inputs are used to supply V<sub>CCO</sub> with power when V<sub>CCI</sub> is less than the battery input voltages. Special circuitry uses a low leakage CMOS process which affords

### PIN ASSIGNMENT



### PIN DESCRIPTION

001		The second secon
V <sub>BAT1</sub>	BRUEL	+ Battery 1 Input
V <sub>BAT2</sub>	a wol	+ Battery 2 Input
Vcco	COULD	RAM Power (V <sub>CC</sub> ) Supply
GND	OHOL	Ground
CEI	HORDIN	Chip Enable Input
CEO	-	Chip Enable Output
WEI	100 4	Write Enable Input
WEO	000 70	Write Enable Output
TOL	ov et	Power Supply Tolerance Select
Aw - Az	4 -	Address Inputs
DIS	atlo +	Memory Partition Disable

- Input +5 Volt Supply

precise voltage detection at extremely low current consumption. By combining the DS1610 Partitioned NV Controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

Power Fail Output

The DS1610 Partitioned NV Controller functions like the Dallas Semiconductor DS1210 NV controller when the ( $\overline{DIS}$ ) disable pin is grounded. An internal pulldown resistor to ground on the  $\overline{DIS}$  pin of the DS1610S allows it to retrofit into DS1210S applications. When the  $\overline{DIS}$  pin is grounded the address inputs  $A_W$  -  $A_Z$  and the write enable input  $\overline{WEI}$  are ignored. Also the power fail output  $\overline{PFO}$  and the write enable output  $\overline{WEO}$  are tristated.

## OPERATION - DISABLE PIN CONNECTED

TO VCCO The DS1610 performs five circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V<sub>CCI</sub>) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function provided by the DS1610 is power fail detection. The incoming supply (V<sub>CCI</sub>) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits both the chip enable output (CEO) and the write enable output (WEO). A third function of write protection is accomplished by holding both the chip enable output CEO and write enable output WEO to within 0.2 volts of VCCO when V<sub>CCI</sub> is out of tolerance. If CEI is low at the time that power fail detection occurs the CEO signal is kept low until CEI is brought high again. However, CEO is forced high after 1.5 usec regardless of the state of CEI. Similarly, if WEI is low at the time that power fail detection occurs, the WEO is signal will remain low until WEI is brought high or 1.5 µsec elapses. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin TOL grounded. If the tolerance pin is connected to VCCO then power fail detection occurs in the range of 4.5 volts to 4.25 volts. The PFO signal is driven low and remains low until V<sub>CCI</sub> returns to nominal conditions. During nominal supply conditions CEO will follow CEI and WEO will follow WEI. The fourth function which the DS1610 performs is a battery status warning so that potential data loss is avoided. Each time V<sub>CCI</sub> is applied to the device battery status is checked with a precision comparator. If during battery backup, no switch occurred from one battery to the other, the voltage of the battery supplying power when V<sub>CCI</sub> is applied is checked. If this voltage is less than 2.0 volts the second chip enable cycle after power is applied is inhibited. If any switch from one battery to another did occur the voltage of both batteries is checked. If either voltage is less than 2.0 volts the second chip enable cycle will be inhibited. Battery status can therefore be determined by performing a read cycle after power up to any location in memory, verifying that memory location's contents. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data then the data is in danger of being corrupted. The fifth function of the DS1610 provides for battery redundancy. When data integrity is extremely important it is wise to use two batteries to insure reliability. The DS1610 controller provides an internal isolation switch which allows the connection of two batteries. When entering battery backup operation, the battery with the highest voltage is selected for use. If one battery should fail, the other would then supply energy to the connected load. The switch to a redundant battery is transparent to circuit operation and to the user. In applications where battery redundancy is not a major concern a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. When batteries are first connected to one or both of the  $V_{\rm BAT}$  pins  $V_{\rm CCO}$  will not show the battery potential until  $V_{\rm CCI}$  is applied and removed for the first time.

## OPERATION – WRITE PROTECTION PROGRAMMING MODE

When the disable pin is connected to V<sub>CCI</sub> or V<sub>CCO</sub>, the DS1610 performs all of the functions described earlier with the addition of a partition switch which selectively write protects blocks of memory. The state of the DIS pin is strobed and latched as V<sub>CCI</sub> crosses the power fail trip point so that the DS1610 maintains its configuration during power loss. If the strobed value of DIS is a high the internal pulldown resistor on the DIS pin will be disconnected in the power fail state to eliminate the possibility of battery discharge. The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines Aw-Az. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions, the size of each partition is determined by the size of the memory. For example, a 128K X 8 memory would be divided into 16 partitions of 128K/16 or 8K X 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by Aw through Az and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin Ax was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1610 to inhibit WEO from going low as WEI goes low whenever AzAyAxAw=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM. Also note that on initial battery attach the partition register can power up in any state.

TABI	ABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A <sub>W</sub>	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A <sub>X</sub>	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
Ay	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
Az	1	1	0	0	0	1	1	1	0	0	1	0	0	.0	1	0	1	0	0	0	X	X	X	X

ABLE 2:	PARTITION REG	ISTER MAPPING	
Address Pin	Bit number in pattern match sequence	Partition Number	71001000 01010 711100100
Aw	BIT 21	PARTITION 0	0000
Ax	BIT 21	PARTITION 1	0001
Ay	BIT 21	PARTITION 2	0010
Az	BIT 21	PARTITION 3	0011
Aw	BIT 22	PARTITION 4	0100
Ax	BIT 22	PARTITION 5	0101
Ay	BIT 22	PARTITION 6	0110
Az	BIT 22	PARTITION 7	0111
Aw	BIT 23	PARTITION 8	1000
A <sub>X</sub>	BIT 23	PARTITION 9	1001
Ay	BIT 23	PARTITION 10	1010
Az	BIT 23	PARTITION 11	1011
Aw	BIT 24	PARTITION 12	1100
Ax	BIT 24	PARTITION 13	1101
Ay	BIT 24	PARTITION 14	1110
Az	BIT 24	PARTITION 15	1111

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature

Soldering Temperature

-0.5V to 7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 6 = GND Supply Voltage	V <sub>CCI</sub>	4.75	5.0	5.5	٧	- 1
Pin 6 = V <sub>CCO</sub> Supply Voltage	V <sub>CCI</sub>	4.5	5.0	5.5	٧	1
Logic 1 Input	V <sub>IH</sub>	2.0	Up the base of	V <sub>CC</sub> + 0.3	٧	1
Logic 0 Input	V <sub>IL</sub>	-0.3	KELLES F	+0.8	٧	1
Battery Input	V <sub>BAT1</sub> V <sub>BAT2</sub>	2.0	Pal	4.0	V	1,2

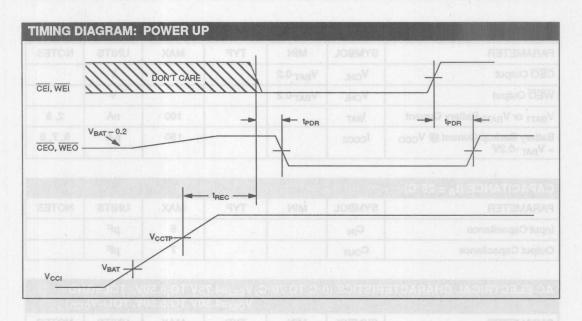
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I <sub>CC1</sub>	ENORMER		5	mA	3,14
Standby Current	I <sub>CC2</sub>	e NOLLIUM		200	μА	3, 15
Supply Voltage	V <sub>CCO</sub>	V <sub>CC</sub> -0.2		22.169	V	1
Supply Current	I <sub>CCO1</sub>	S PRUITING		150	mA	4
Input Leakage	IIL	-1.0		+1.0	μА	
Output Leakage	ILO	-1.0		+1.0	μА	
V <sub>CC</sub> Trip Point (TOL=GND)	V <sub>CCTP</sub>	4.50	4.62	4.75	٧	1,16
V <sub>CC</sub> Trip Point (TOL=V <sub>CC</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.50	V	1,16
CEI to CEO Impedance	Z <sub>CE</sub>	L MOHILLIA		30	Ω	5
WEI to WEO Impedance	Z <sub>WE</sub>	I NOTTINA		30	Ω	5
DIS Pulldown Resistance	R <sub>DIS</sub>	50K		250K	Ω	

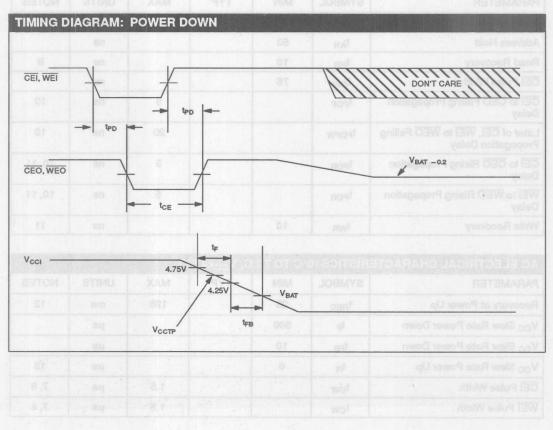
DC ELECTRICAL CHARACTI	DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V <sub>CCI</sub> <v<sub>BAT)</v<sub>											
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES						
CEO Output	V <sub>OHL</sub>	V <sub>BAT</sub> -0.2	11/1/	SAAD THOSE	V							
WEO Output	V <sub>OHL</sub>	V <sub>BAT</sub> -0.2	DETELL		V	(BW,BD						
V <sub>BAT1</sub> or V <sub>BAT2</sub> Battery Current	I <sub>BAT</sub>	nost -tel		100	nA	2, 3						
Battery Backup Current @ V <sub>CCO</sub> = V <sub>BAT</sub> -0.2V	I <sub>CCO2</sub>	4		150	μА	6, 7, 8						

CAPACITANCE (t <sub>A</sub> = 25°	°C)	1118				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

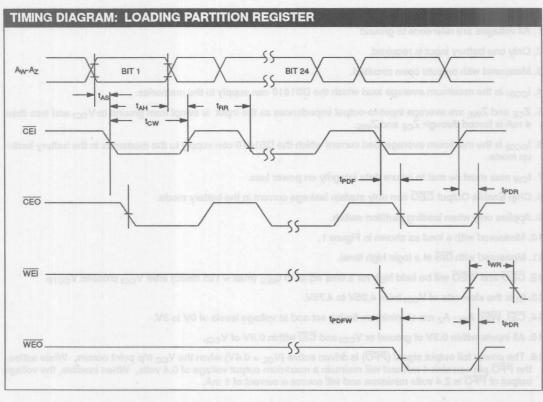
AC ELECTRICAL CHARACTE	ERISTICS (0	°C TO 70°	C; V <sub>CCI</sub> =4.7 V <sub>CCI</sub> =4.5	5V TO 5.50 0V TO 5.50	OV, TOL=G OV, TOL-V	ND co)
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	tas	0	MWC	O HEWO	ns	пынкар
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	10			ns	9
CEI Pulse Width	t <sub>CW</sub>	75			ns	oil, Wife
CEI to CEO Falling Propagation Delay	t <sub>PDF</sub>		-60	5	ns	10
Later of CEI, WEI to WEO Falling Propagation Delay	t <sub>PDFW</sub>			20	ns	10
CEI to CEO Rising Propagation Delay	t <sub>PDR</sub>			5	ns	10, 11
WEI to WEO Rising Propagation Delay	t <sub>PDR</sub>		100	5	ns	10, 11
Write Recovery	t <sub>WR</sub>	10			ns	11

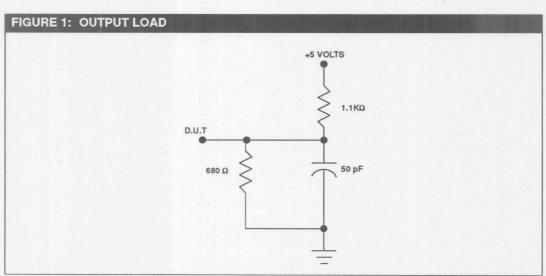
AC ELECTRICAL CHARAC	TERISTICS (0	°C TO 70°	C, V <sub>CC</sub> <4.5	(V)		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t <sub>REC</sub>	25		125	ms	12
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub>	300	er .	Veem	μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub>	10			μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub>	0			μs	13
CEI Pulse Width	t <sub>CW</sub>			1.5	μs	7, 8
WEI Pulse Width	t <sub>CW</sub>			1.5	μѕ	7, 8





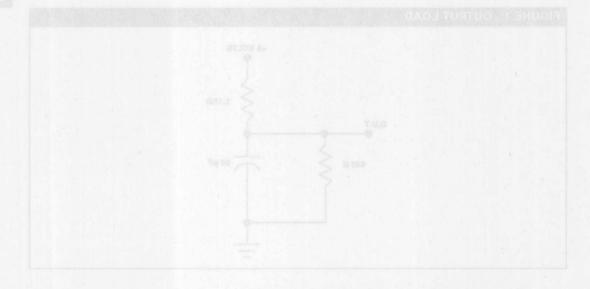






### NOTES

- 1. All voltages are reference to ground
- 2. Only one battery input is required.
- 3. Measured with outputs open circuited.
- 4. I<sub>CC01</sub> is the maximum average load which the DS1610 can supply to the memories.
- 5.  $Z_{CE}$  and  $Z_{WE}$  are average input-to-output impedances as the input is swept from ground to  $V_{CCI}$  and less than 4 mA is forced through  $Z_{CE}$  and  $Z_{WE}$ .
- I<sub>CC02</sub> is the maximum average load current which the DS1610 can supply to the memories in the battery backup mode.
- 7. t<sub>CW</sub> max must be met to insure data integrity on power loss.
- 8. Chip Enable Output CEO can only sustain leakage current in the battery mode.
- 9. Applies only when loading partition switch.
- 10. Measured with a load as shown in Figure 1.
- 11. Measured with DIS at a logic high level.
- 12. CEO and WEO will be held high for a time equal to t<sub>REC</sub> (max = 125 msec) after V<sub>CCI</sub> crosses V<sub>CCTP</sub>.
- 13. t<sub>R</sub> is the slew rate of V<sub>CCI</sub> from 4.25V to 4.75V.
- 14. CEI, WEI, Aw Az run at minimum timing set and at voltage levels of 0V to 3V.
- 15. All inputs within 0.3V of ground or VCCI and CEI within 0.3V of VCCI.
- 16. The power fail output signal (PFO) is driven active (V<sub>OL</sub> = 0.4V) when the V<sub>CC</sub> trip point occurs. While active, the PFO pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of PFO is 2.4 volts minimum and will source a current of 1 mA.



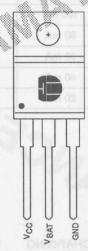
### DALLAS SEMICONDUCTOR

### DS1633x High Speed Battery Recharger

### **FEATURES**

- Recharges lithium batteries and NiCad batteries
- · Cuts in half normal battery charge time
- Accepts open circuit power supply voltages between 4.75 and 6.0 V, and battery voltages between 0 and 3.75 V
- Retains battery and power supply limits in on-board memory
- · Part is programmed and tested in the factory
- 3-pin TO-220 package
- Operating range—10°C to 85°C
- Applications include consumer electronics, portable/ cellular phones, pagers, medical instruments, backup memory systems, security systems
- Supplies a maximum of 100 mA to a charging battery, as DC or pulsed charging current

### PIN ASSIGNMENT (DIP PKG)



### **PIN DESCRIPTION**

Vcc

Input Voltage, +

V<sub>BAT</sub> GND Battery Voltage Input, +

Ground

#### DESCRIPTION

The DS1633 High Speed Battery Recharger automatically provides a constant current recharge to a battery as long as the battery's voltage is below the specified minimum voltage. The DS1633 charges the battery using its V<sub>CC</sub> input as a source. When V<sub>CC</sub> is floated, the DS1633 is dormant. When V<sub>CC</sub> is reapplied, the DS1633 begins charging.

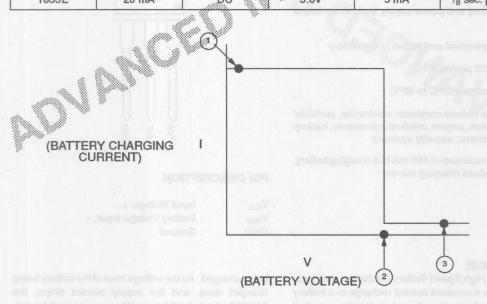
Although a variety of load curves may be used to charge a battery, most do not take advantage of the fact that a battery can accept its maximum (or above) current rating for charging purposes over its entire voltage range. The DS1633 takes advantage of this opportunity by constantly readjusting its current supply to the battery being charged. As the voltage level of the battery being charged rises, and the supply current drops, the DS1633 adjusts itself to boost the current supply back to its maximum. This feature greatly decreases the recharge time required to fully charge a lithium or NiCad cell.

The DS1633 provides a designer with the ability to use a customized battery load line for currents up to 100 mA by selecting a pre-programmed DS1633 from Dallas Semiconductor. A DS1633 solution provides a self contained charging system which requires no backup memory support, user programming, or external interface circuitry.

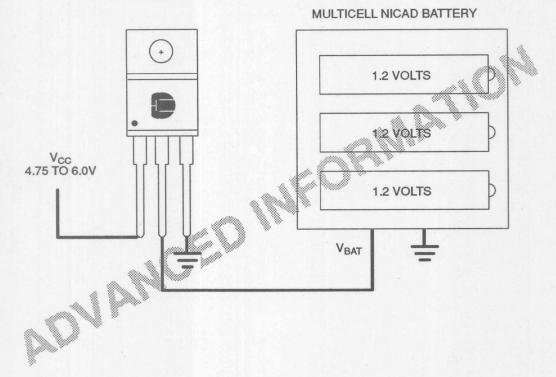
The Profile Characteristics table lists charge curves and part reference designators for the pre-programmed curves that Dallas Semiconductor will initially offer.

For requirements which cannot be met by one of the initial charge curve programs listed, please contact the nearest Dallas Semiconductor Sales Office.

		PROFILE CH	ARACTERISTICS	S	
DS1633 CHARGE PROFILE	(1) MAXIMUM CURRENT	(1A) MAXIMUM CURRENT FREQUENCY	(2) CUTOFF VOLTAGE	(3) TRICKLE CURRENT	(3A) TRICKLE PREQUENCY
1633A	100 mA	DC	3.6V	17 mA	1/8 sec. pulse/1 sec
1633B	80 mA	DC	3.6V	9 mA	1/8 sec. pulse/1 sec
1633C	60 mA	DC	3,6V	7 mA	1/8 sec. pulse/1 sec
1633D	40 mA	DC	3.6V	5 mA	1/8 sec. pulse/1 sec
1633E	20 mA	DC	3.6V	5 mA	1/8 sec. pulse/1 sec



### TYPICAL APPLICATION



**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

Timekeeping

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

## **System Extension**

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 

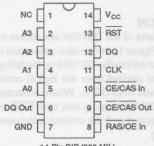


# DS1206 Phantom Serial Interface Chip

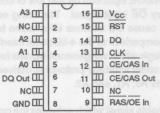
#### **FEATURES**

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as ten DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

#### PIN ASSIGNMENT



14-Pin DIP (300 MIL) See Mech. Drawing -Sect. 16, Pg. 1



16-Pin SOIC (300 MIL) See Mech. Drawing – Sect. 16, Pg. 6

#### IN DESCRIPTION

NC – No connection

A0-A3 - Memory address bus
DQ Out - Data out to memory bus

GND - Ground

RAS/OE In - Output Enable or RAS input from

memory bus

CE/CAS In - Chip enable or CAS from memory bus CE/CAS Out - Chip enable or CAS to memory circuit

CLK - Clock for serial port
DQ - Data I/O for serial port
RST - Reset for serial port

V<sub>CC</sub> - +5 Volts

## DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control

the serial port. A sequence of software-generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the CE/CAS signal and RAS/OE signal without affecting

address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via  $\overline{\text{CE}}/\overline{\text{CAS}}$  output. An additional address sequence is required to generate the 3-wire port signals:  $\overline{\text{RESET}}$  ( $\overline{\text{RST}}$ ), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

#### **OPERATION**

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of CE/CAS In and RAS/OE In. When redirecting information from a DRAM memory bus, both RAS and CAS inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a  $\overline{\text{CE}}$  input is required and the  $\overline{\text{RAS/OE}}$  input can be tied low or connected to the memory  $\overline{\text{OE}}$  input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

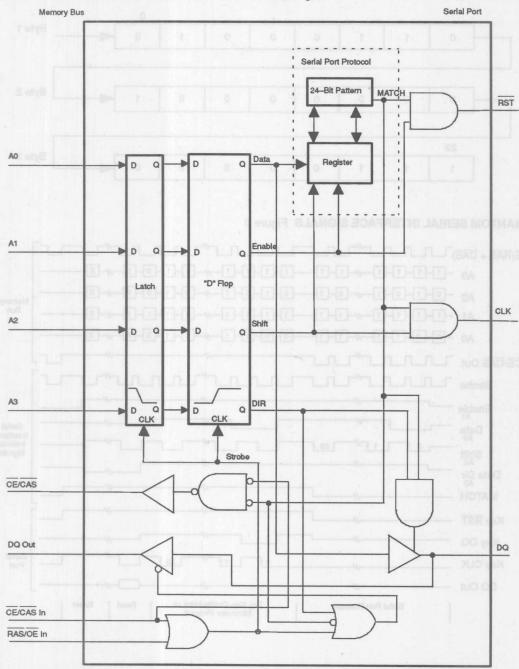
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

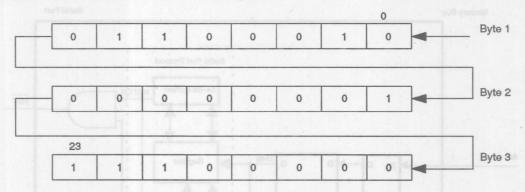
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the RST signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When RST is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

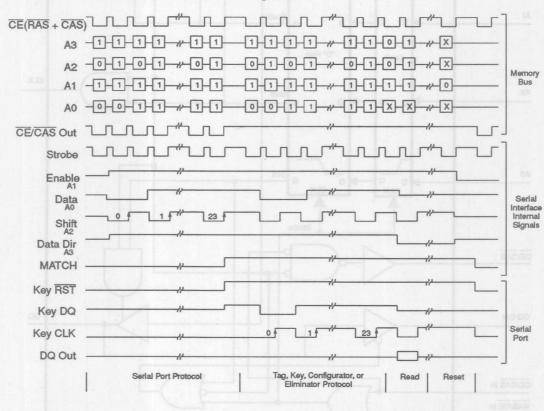
### PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



## **PHANTOM SERIAL INTERFACE SIGNALS** Figure 3



# 10

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature -0.5V to +7.0V 0°C to 70°C -55°C to +125°C

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> + 0.3	V	1
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1
Supply	Vcc	4.5	5.0	5.5	V	1

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{DD} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-1		1	μА	
Output Leakage	lLO			1	μА	
Output Current @ 2.4V	loh	-1		RST, CLK	mA	
Output Current @ .4V	loL	+4			mA	
RST Output Current @ 3.8V	I <sub>OHR</sub>	16		725	mA	
Supply Current	Icc	2008		6	mA	2

#### CAPACITANCE

(ta=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	DG LIELDIN
Input/Output	C <sub>I/O</sub>		5	10	pF	

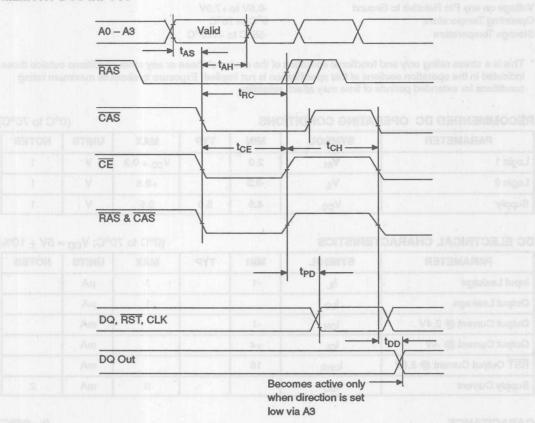
#### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0			ns	
Address Hold	t <sub>AH</sub>	50	T.U.Q		ns	
RAS to CAS Overlap	t <sub>RC</sub>	60			ns	
CE Pulse Width	t <sub>CE</sub>	60	3		ns	
Key Signals Valid	t <sub>PD</sub>		3	60	ns	3
Key Data Out	t <sub>DD</sub>	10			ns	3
CE Inactive	t <sub>CH</sub>	30			ns	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

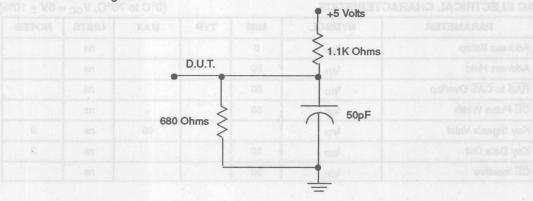
#### **MEMORY BUS INPUTS**



#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. Measured with a load as shown in Figure 4.

# **OUTPUT LOAD** Figure 4



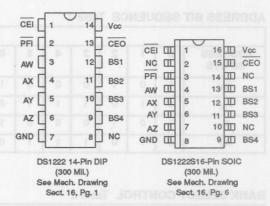
# **DALLAS**SEMICONDUCTOR

# DS1222 BankSwitch Chip

#### **FEATURES**

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ± 10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

I III DECO	III HOIL	
Aw-Az	Address Inputs	
CEI	Chip Enable Input	
CEO	Chip Enable Output	
NC	No Connection	
BS1,BS2,	Bank Select Outputs	
BS3,BS4	Bank Select Outputs	
PFI	Power Fail Input	
Vcc	+5 Volts	
GND	Ground	

#### DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

#### **OPERATION - BANK SWITCHING**

Initially, on power-up all four bank select outputs are low and the chip enable output ( $\overline{\text{CEO}}$ ) is held high. (Note: the power fail input [ $\overline{\text{PFI}}$ ] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs AW through AZ should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when  $\overline{\text{CEI}}$  is driven

low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses AX, AY, and AZ. However, address line AW defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of  $\overline{\text{CEI}}$  when the last set of bits is input and a

match has been established. After bank selection  $\overline{\text{CEO}}$  always follows  $\overline{\text{CEI}}$  with a maximum propagation delay of 15ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

#### **ADDRESS BIT SEQUENCE** Table 1

							BI	TSEC	DUEN	CE						
ADDRESS INPUTS	0	1	2	3	4	5	6	7	8	9	10	11 ed 8	12	13	14	15
Aw	1	0	1	0	0	0	1	1	0	1	0	X	x	×	X	×
A <sub>X</sub>	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
Ay	1	0	1	0	0	0	1	1	0	1	0	1	1.00	1	0	0
Az	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

#### **BANK SELECT CONTROL** Table 2

Bank		Aw	Bit Seque	ence			Out	puts	
Selected	11	12	13	14	15	BS1	BS2	BS3	BS4
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	ndtsor	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1001	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1 .	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	fluctio 8	High	High	High	Low
Bank 8	Soft aug	o elfane	0	0	0	Low	Low	Low	High
Bank 9	1111	1	0	0	stations	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	treu1ee	-0 / 1 mm	0	1 1	1.0	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	0 001	SATERIA	es da es	0	1	High	Low	High	High
Bank 14	0 fld1fllw	1	are <b>t</b> egts	1 1 old	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

\*CEO = VIH independent of CEI

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature

-0.3V to +7.0V 0°C to 70°C -55°C to +125°C

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	1
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	1

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C: Vcc = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	IIL	-1.0		+1.0	μА	
I/O Leakage Current	ILO	-1.0	X	+1.0	μА	wA.
Output Current @ 2.4V	Гон	-1.0			mA	2
Output Current @ 0.4V	loL			+4.0	mA	2
Operating Current	Icc			15	mA	

#### CAPACITANCE

 $(t_{\Delta} = 25^{\circ}C)$ 

						(A -
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	B5 -

#### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CC</sub> = 5V± 10%)

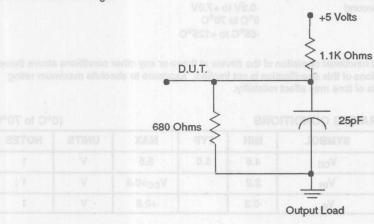
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	5			ns	88
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	40			ns	
Propagation Delay	t <sub>PD</sub>			15	ns	2
Power Fail Input to First CEI	tpF	50			ns	
Chip Enable Low	tcw	110			ns	

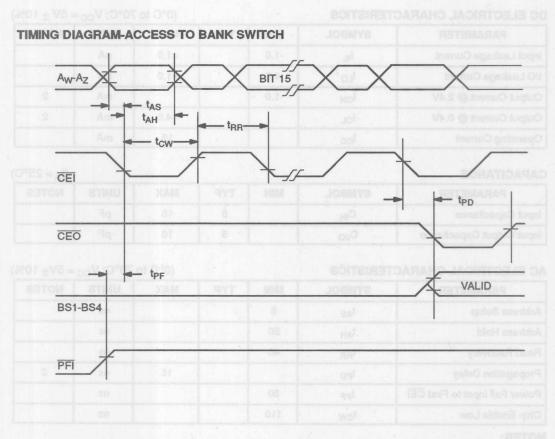
#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 1.

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### **OUTPUT LOAD** Figure 1





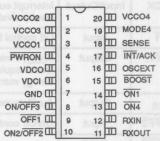
#### **FEATURES**

- Provides step-up regulation and microenergy management for battery-operated systems
- Converts +3V to +6V DC input power source to +5V DC out for system power
- "Kickstarts" system power upon detection of external stimuli:
  - Clock/calendar alarm
  - Sensor trip; such as from a photo diode
  - Incoming activity to a serial port
  - Any low-level signal transition
- Shuts down microcontroller power under software control when operation complete
- Provides 3 auxiliary power outputs for independent powering of system functions
- · Allows design of "power on demand" systems
- Insures maximum life of main power source
- Ideally suited for DS5000-based systems
- Available in 20-pin DIP or SOIC packages

#### PIN ASSIGNMENT



20-Pin DIP (300 Mil) See Mech. Drawing - Sect. 16, Pg. 1



20-Pin SOIC (300 Mil) See Mech. Drawing - Sect. 16, Pg. 6

#### ORDERING INFORMATION

DS1227: 20-Pin DIP DS1227S: 20-Pin SOIC

#### DESCRIPTION

The DS1227 Kickstarter is a unique CMOS circuit which combines power conversion and microenergy management functions for battery operated systems. Using its integral DC-DC converter, the DS1227 supplies +5V on demand from either a 3– or 6–volt battery input. The primary +5V output, typically tied to the microcontroller's V<sub>CC</sub> pin, is "kickstarted" on in response to any one of

several possible momentary, external signal transitions. Two auxiliary +5V power supply outputs can then be independently enabled or disabled under software control. When the primary power supply output is disabled, also under software control, the auxiliary power supply outputs remain in the state selected. In this manner, individual portions of the system can be powered only

when they are required, minimizing the energy consumption of the system.

The Kickstarter activates or kickstarts the primary V<sub>CC</sub> output in response to external momentary low-going signals. Examples of such signals include a clock/calendar alarm from a DS1283 Watchdog Timekeeper, or an incoming asynchronous serial data word from a host PC via the DS1275 Line Powered Transceiver, or a simple pushbutton switch.

In addition, the DS1227 kickstarts primary system power in response to activity detected by an external sensor circuit. In this case, the Kickstarter can be signalled at regular intervals, typically from a DS1283 Watchdog Timekeeper, to momentarily apply power to the sensor and monitor an input for an active response.

An application using the Kickstarter has the capability to wake-up from a ultra-low power state, perform a task using minimum energy, and then go back to sleep until the DS1227 is signalled to kickstart system operation once again.

#### PIN DESCRIPTION

PIN	1/0	DESCRIPTION
BOOST	Input	Regulation mode control.
V <sub>DCO</sub>	Output	Main DC supply voltage output.
V <sub>DCI</sub>	Input	Main DC supply voltage input.
GND	7º 님칙	System ground.
V <sub>CCO1</sub>	Output	Primary switched supply voltage output.
ŌN1	Input	On control for $V_{CCO1}$ . $\overline{ON1}$ is negative edge triggered and internally pulled high via a weak resistor.
INT/ACK	Input/Output	Interrupt output/input; internally pulled low via a weak resistor during output; level activated via strong high voltage for input.
OFF1	Input	Off control for V <sub>CCO1</sub> ; edge-triggered active low.
PWRON1	Output	V <sub>CCO1</sub> Power On signal output; Indicates when V <sub>CCO1</sub> is powered on; Sometimes required for controlling external tri-state buffers in systems where microenergy management techniques are employed.
V <sub>CCO2</sub>	Output	Auxiliary switched supply voltage outputs.
ON2/OFF2	Input	On/Off controls for V <sub>CCO2</sub> /V <sub>CCO3</sub> ; level activated.
ON3/OFF3	Input	
V <sub>CCO4</sub>	Output	Momentarily switched VCC output.
ON4	Input	V <sub>CCO4</sub> trigger; edge activated; active low.
SENSE	Input	Sense input sampled just prior to $V_{\text{CCO4}}$ off; turns on $V_{\text{CCO1}}$ if active; active high.
MODE4	Input/Output	Selects V <sub>CCO4</sub> on time; level sensitive input/current source output.
RXIN	Input	Serial I/O input; On control for V <sub>CCO1</sub> when serial activity detected; edge activated.
RXOUT	Output	Serial I/O output; Echos incoming serial data from RXIN when V <sub>CCO1</sub> is turned on.
OSCEXT	Output	Oscillator Signal Output; Gated by internal comparator when BOOST is enabled. Continuous when BOOST is disabled.

#### INPUT SUPPLY VOLTAGE

The Kickstarter is capable of operating either in a regulated step-up DC-to-DC conversion (boost) mode or in a non-regulated supply voltage Pass-Through mode.

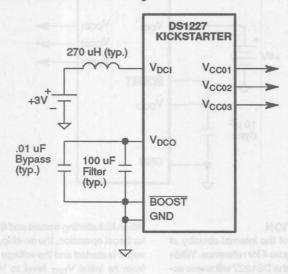
In boost mode, the Kickstarter is designed to provide a regulated +5V output on the V<sub>CCO1</sub>, V<sub>CCO2</sub>, or V<sub>CCO3</sub> voltage supply output pins from a +3V lithium source. Figure 1 illustrates the standard configuration for use of this mode. The  $\overline{\text{BOOST}}$  pin should be tied low in order to enable step-up DC-to-DC conversion. V<sub>DCI</sub> is used for the DC power supply input and is tied through an inductor (270  $\mu\text{H}$  typical) to a +3V lithium cell. V<sub>DCO</sub> is the main DC output which is switched to the V<sub>CCO1</sub>, V<sub>CCO2</sub>, and V<sub>CCO3</sub> outputs. This pin requires a large capacitor (typically 100  $\mu\text{F}$ ) to ground for the boost regulation low pass output network. Further details of the boost voltage regulator operation are given in the "Boost Mode Operation" section of this data sheet.

Figure 2 and Figure 3 illustrate the required configurations to select the supply voltage Pass-Through mode of operation. In both of these configurations the BOOST pin should be strapped directly to the V<sub>DCO</sub> pin. This connection causes the BOOST pin to remain at a high level at all times that a battery is connected. As a result, the internal boost regulator will be disabled when kick-starting occurs. When a +5V supply is used as the input DC power source, it should be directly connected to the V<sub>DCO</sub> in parallel with a filter capacitor as shown in Figure 2. The V<sub>DCI</sub> input itself should be grounded in this configuration.

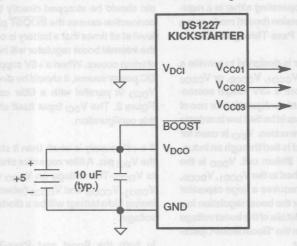
If a +6V supply is used, then it should be connected to the  $V_{DCI}$  pin. A filter capacitor should still be connected to  $V_{DCO}$ . The voltage on  $V_{DCO}$  and subsequently on  $V_{CCO1}$ ,  $V_{CCO2}$ , and  $V_{CCO3}$  (when they are enabled following kickstarting) will be a diode drop below the  $V_{DCI}$  voltage.

In both the Boost and Pass-Through modes, the DS1227 uses the voltage on  $V_{DCO}$  as its own internal supply.

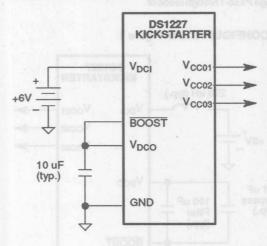
#### **DS1227 BOOST MODE CONFIGURATION** Figure 1



## DS1227 +5V PASS-THROUGH MODE CONFIGURATION Figure 2



# DS1227 +6V PASS-THROUGH MODE CONFIGURATION Figure 3



#### KICKSTARTER OPERATION

A conceptual block diagram of the internal circuitry of the DS1227 is illustrated in Figure 4 for reference. While in an initial power down state, the DS1227 will sense activity from an external stimulus applied to one of three input pins and kickstart system power by applying voltage from the input power source to the primary  $V_{\rm CCO}$  output ( $V_{\rm CCO1}$ ). Activity detected on any of the  $\overline{\rm ON1}$ , RXIN, and SENSE pins initiates the kickstarting action.

When kickstarting occurs and the DS1227 is configured for boost operation, the on-chip, step-up DC-to-DC converter is started and the voltage on  $V_{DCO}$  will be boosted from its initial  $V_{BAT}$  level to  $V_{DCON}$  before  $V_{CCO1}$  is turned on. If the DS1227 is configured for voltage Pass-Through operation, then the DC-to-DC converter will remain disabled and voltage on the  $V_{DCO}$  line will be switched to the  $V_{CCO1}$  pin immediately following the detection of an active transition on a stimulus input.

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Initially, when V<sub>CCO1</sub> is off, the INT/ACK pin is collapsed to ground. At the time that voltage is switched to the V<sub>CCO1</sub> output pin during kickstarting, the INT/ACK pin will be latched such that it will remain in a low state. This signals the microcontroller that a power on reset has occurred. The OFF1, ON2/OFF2, and ON3/OFF3 inputs are all ignored until the microcontroller acknowledges this power on reset condition. This acknowledgement is performed via the same INT/ACK pin, which also performs the function of an interrupt acknowledge input. This is made possible due to the fact that the pin has a weak NMOS pulldown which forms a latch. When INT/ ACK is externally driven with a sufficiently strong high signal (as described in the "Electrical Characteristics" section) the state of the latch will be switched and as a result the interrupt condition will be reset.

After the power on reset interrupt has been acknowledged and the DS1227 is in a power on condition, the INT/ACK pin will be again taken low to signal the detection of active signalling on the ON1 or SENSE inputs. Further activity on the RXIN input will not cause a subsequent interrupt condition. The INT/ACK can be returned to its high (reset) state again by externally driving it with a sufficiently strong high signal.

The  $\overline{\text{OFF1}}$  input is used to turn off the  $V_{\text{CCO1}}$  output under software control. It is typically interfaced to the system microcontroller via a port pin configured as an output. As noted above, it is active only when  $V_{\text{CCO1}}$  is on and  $\overline{\text{INT}}/\text{ACK}$  has been set high.

#### STIMULUS INPUTS

ON1 is a simple TTL-level compatible input which is designed to detect a negative-going edge. V<sub>CCO1</sub> is kick-started whenever an active edge is detected on this pin.

The RXIN input can be used to initiate the kickstarting action in response to the detection of incoming serial data. In this configuration, the RXIN pin is interfaced to an incoming serial data line, typically from an RS232 transceiver. RXOUT is the corresponding output and is used to route the serial data to the microcontroller. RXIN remains internally disconnected from RXOUT until VCCO1 is powered on. At that time, the two lines are connected and serial data is passed straight through the device to the microcontroller.

The SENSE pin is intended to be connected to an external sensor circuit which is powered from V<sub>CCO4</sub>. This

circuit is then momentarily powered from the Kickstarter's  $V_{CCO4}$  output in response to a negative going edge applied to the  $\overline{ON4}$  input.  $V_{CCO4}$  will stay powered for an amount of time determined by the circuitry on the MODE4 pin. During the time that  $V_{CCO4}$  is on, the SENSE pin has an internal pulldown device which is activated. SENSE is sampled just prior to the  $V_{CCO4}$  output being disconnected. If SENSE is externally driven high  $(V_{IH})$  at this time, it kickstarts  $V_{CCO1}$  power. Any time that  $V_{CCO4}$  power is off, the SENSE pin appears as a high impedance to external circuitry.

The amount of time that  $V_{CCO4}$  is on is determined by the configuration of the MODE4 pin. MODE4 is intended to either be tied high (typically to  $V_{DCO}$ ) or tied to an external capacitor. The  $V_{CCO4}$  on time is thereby determined either by the amount of time between falling edges on  $\overline{ON4}$  or by the value of the capacitor.

If the MODE4 pin is tied high at the time that  $\overline{\text{ON4}}$  is activated, then  $V_{\text{CCO4}}$  will remain on until the next falling edge is detected on  $\overline{\text{ON4}}$ . Figure 5 illustrates the timing associated with this mode of operation. If the Kickstarter is also configured for boost regulation and  $V_{\text{CCO1}}$ ,  $V_{\text{CCO2}}$ , and  $V_{\text{CCO3}}$  are turned off, the DC-DC converter will be briefly enabled so that +5V will be supplied on  $V_{\text{CCO4}}$  for the duration of the time that it is on.

The alternative MODE4 configuration is illustrated in Figure 6A. As shown in the figure, it is recommended for most applications that a large resistor also be connected between MODE4 and ground in addition to the capacitor. For the configuration shown, the MODE4 pin will be sensed low by the Kickstarter just following the negative-going edge at ON4. Following this condition, a constant current specified as IM4ON is supplied out of the MODE4 pin. This will cause the voltage on MODE4 to rise linearly. V<sub>CCO4</sub> will remain on until the voltage on MODE4 reaches a threshold specified as VM4OFF (approximately 0.5 V<sub>DCO</sub>). At this time, V<sub>CCO4</sub> will be shut off. At the same time, the constant current source on the MODE4 pin will be disconnected and an internal resistive element (specified as R<sub>M4DIS</sub>) will be connected between the MODE4 pin and ground. This internal resistive element along with any external resistance will cause the voltage on the capacitor to decay exponentially until it reaches a threshold specified as V<sub>M4DIS</sub> (approximately 0.1 V<sub>DCO</sub>). When this condition is reached, the internal resistive element will be disconnected, and the MODE4 pin will appear as a high impedance until the next active transition occurs on ON4. The external resistor (if present) will then cause the voltage on MODE4 to further decay until it reaches ground or until the next ON4 negative transition, whichever comes first.

When MODE4 is initially grounded as described above,  $V_{CCO4}$  power is switched from the  $V_{DCO}$  pin, regardless of whether or not  $V_{CCO1}$ ,  $V_{CCO2}$ , or  $V_{CCO3}$ , are powered on. This means that  $V_{CCO4}$  will be switched with the voltage present on  $V_{DCO}$ , which could be from +3V to +5V depending on the configuration, input battery voltage used, and whether or not  $V_{CCO1}$ ,  $V_{CCO2}$ , or  $V_{CCO3}$  are switched on.

The above described sampling operation of  $V_{CCO4}$  and SENSE in response to  $\overline{ON4}$  also takes place when a kickstart has already occurred and  $V_{CCO1}$  is on. If SENSE is found to be active in this condition, an interrupt will be signalled on the INT/ $\overline{ACK}$  pin.

#### MICRO ENERGY MANAGEMENT

In addition to the kickstarting features described above, the DS1227 allows sections of system circuitry to be individually powered up or down under command of the microcontroller. This capability is referred to as the Micro Energy Management feature of the DS1227.

 $V_{\rm CCO2}$  and  $V_{\rm CCO3}$  are auxiliary power supply outputs which may be switched on or off via the ON2/OFF2 and ON3/OFF3 pins, respectively. The ON2/OFF2 and ON3/OFF3 control pins are intended for connection to two microcontroller's port pins configured as outputs. The corresponding  $V_{\rm CCO}$  output pins can then be turned

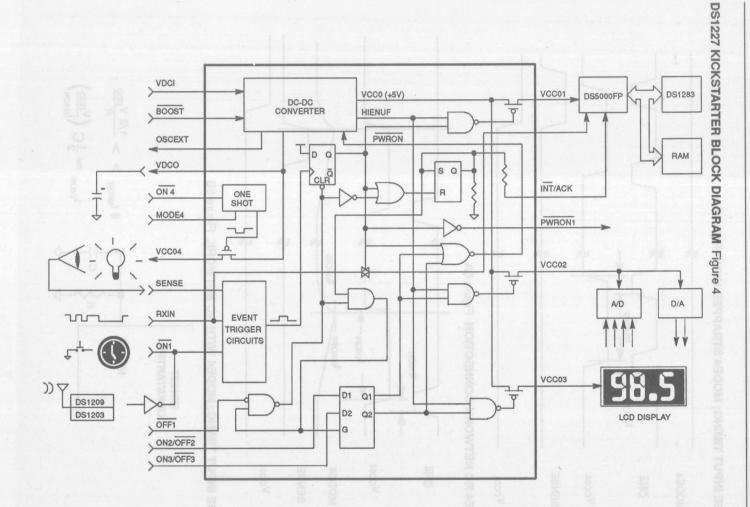
on or off as desired under control of the system application software.

The ON2/OFF2 and ON3/OFF3 inputs are level activated. The corresponding V<sub>CCO</sub> output therefore turns on when the on/off pin is high and off when it is low. These inputs are active only if the V<sub>CCO1</sub> output is on and the INT/ACK output has been set to a high state signalling a power on reset condition.

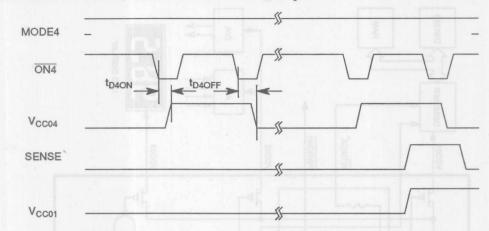
When V<sub>CCO2</sub> or V<sub>CCO3</sub> are turned on, they will remain on until the corresponding control input is taken low by the software. This is true even if the OFF1 input is taken to its active low state at the time that either ON2/OFF2, ON3/OFF3, or both, are high.

Once OFF1 is activated, the current states of ON2/OFF2 and ON3/OFF3 are internally latched and further activity on these pins is ignored. If both of the corresponding outputs (VCCO2 and VCCO3) are turned off at this time and boost operation has been selected, then the internal oscillator is killed and the DC-to-DC converter will be shut down. If either VCCO2 and/or VCCO3 are left switched on when OFF1 is activated, they will remain switched on even after V<sub>CCO1</sub> has been turned off. If the DS1227 has been configured for boost operation, the DC-to-DC converter will remain operational during the entire time that V<sub>CCO1</sub> is turned off so that +5 volts will continue to be supplied on either or both of these output pins. These pins can be shut off only when kickstarting occurs once again and V<sub>CCO1</sub> is switched on and INT/ACK has been set high.

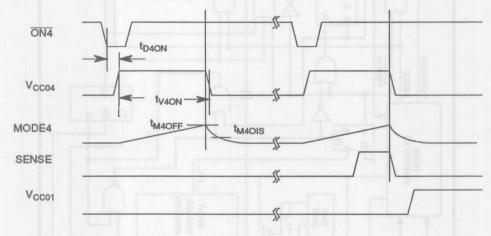
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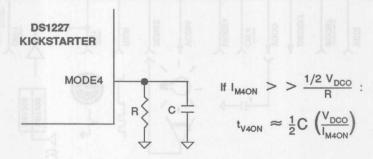
# SENSE INPUT TIMING; MODE4 STRAPPED HIGH Figure 5



## MODE4 RC NETWORK CONNECTION Figure 6A



# SENSE INPUT TIMING; MODE4 WITH RC NETWORK Figure 6B



# 10

#### **BOOST MODE OPERATION**

The DS1227 Kickstarter incorporates all of the necessary control and power switching functions required for its +3V to +5V step-up DC-to-DC converter. These functions include a bandgap reference, oscillator, voltage comparator, catch diode and an N-channel MOSFET. The only external components required are an output filter capacitor and a low cost inductor. The block diagram shown in Figure 7 illustrates the DC-to-DC converter.

When kickstarting occurs from an initial powered down state (i.e., V<sub>CCO1</sub>, V<sub>CCO2</sub>, and V<sub>CCO3</sub> turned off), an internal start sequence is initiated within the DS1227. During this sequence, the V<sub>CCO1</sub> output remains shut off and the BOOST pin is sampled in order to determine if the DS1227 is configured for boost mode operation. If BOOST is low, then boost mode operation is enabled and the DC-to-DC converter is started.

The internal DC-to-DC converter is started by enabling the on-chip 40 KHz oscillator. It then begins to build up the voltage on the  $V_{\rm DCO}$  filter capacitor. Internal counter logic insures that the DC-to-DC converter stays in start mode for a minimum of six clock periods (nominally  $150\,\mu s$ @40 KHz). After this initial delay time, the  $V_{\rm DCO}$  output is monitored by the internal Error Comparator as it slews up to  $V_{\rm DCON}$ . As long as the  $V_{\rm DCO}$  voltage remains below the preset value, the Error Comparator will be switched high and the internal 40 KHz oscillator will be connected to the gate of the  $V_{\rm DCI}$  driver.

The V<sub>DCI</sub> driver is a large N-channel MOSFET with a typical ON resistance of less than 4 Ohms and is capable of supplying a peak current of 450 mA. The output device is turned on during each ON half-cycle generated by the internal square-wave oscillator, and is turned off during each OFF half-cycle. During each ON half-cycle, the current through the inductor rises linearly, storing energy in the coil. When the output device is turned off, the external inductor's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at VDCI then rises until the internal diode is forward biased, delivering power to the V<sub>DCO</sub> output. The converter is thereby powered from its own V<sub>DCO</sub> output. This is often referred to as "bootstrapped" operation, since the circuit figuratively "lifts" itself up. In order to guarantee that the Kickstarter can bootstrap itself up to operating voltage, the VDCI voltage must be at the minimum level of VDCISU as listed in the DC characteristics section of this data sheet.

When the voltage on  $V_{DCO}$  rises to the  $V_{DCON}$  threshold, the internal signal called "HIENUF" will be active and the  $V_{CCO1}$  PMOS device is switched on. As noted above, internal circuitry insures that this device will not be switched on for a minimum of 6 clock cycles from the time that the DC-to-DC converter is started. However, since the recommended values for the external LC components result in a time constant which is much longer than six cycles, the actual slew rate will in practice be much longer than this delay time.

If loading of the V<sub>CCO</sub> outputs causes V<sub>DCO</sub> to drop below V<sub>DCOFF</sub> the DS1227 will deactivate HIENUF and the V<sub>CCO1</sub> PMOS device as well as the other V<sub>CCO</sub> PMOS devices will be switched off. The VDCO voltage will then be monitored for the V<sub>DCON</sub> trip point before reconnecting the load. As a result, the power control regulation loop could oscillate between these two states until the V<sub>CCO1</sub> node had sufficient charge to remain above the V<sub>DCOFF</sub> threshold. To prevent this from occurring, the value of the filter capacitor must be sufficiently large. For large capacitive loads on V<sub>CCO1</sub> the output may dip below VDCOFF as a result of charge sharing and a larger regulation capacitor at VDCO may be required. For large resistive loads the inductance and capacitance values may need to be adjusted using a smaller inductor value and large capacitance. In order not to violate the peak V<sub>DCI</sub> current it may be necessary to use the external oscillator OSCEXT to drive an additional switchmode boost regulator, as shown in Figure 8.

Following the above described start sequence, normal boost operation is performed by the converter.  $V_{DCO}$  output voltage is constantly monitored by the error comparator. When  $V_{DCO}$  voltage drops below the preset value, the error comparator switches high and connects the internal 40 KHz oscillator to the gate of the  $V_{DCI}$  output driver. When the output voltage reaches the desired level, the error comparator inhibits the  $V_{DCI}$  output driver until the load on  $V_{CCO1}$  discharges the output filter capacitor to less than the desired output level.

#### **INDUCTOR SELECTION**

The available output current from the Kickstarter's on-chip DC-DC boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most applications, the inductor is the only design variable since the internal oscillator is preset to a fixed value of 40 KHz. The proper inductor must have the following characteristics:

- 1) the correct inductance value must be selected.
- 2) the inductor must be able to handle the required peak currents.
- 3) the inductor must have acceptable series resistance and must not saturate.

When the internal N-channel MOSFET turns on, the current through the inductor rises linearly since:

$$\frac{di}{dt} = \frac{V}{L}$$
 where L is the inductance value

At the end of the on-time, ton, the peak current, lpK is:

$$I_{PK} = \frac{V t_{ON}}{L} \text{ where : } t_{ON} = \frac{1}{2f_{O}}$$

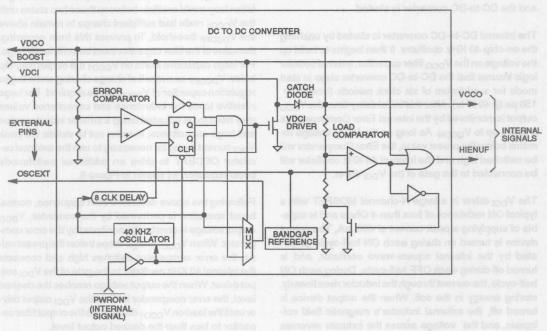
The energy in the inductor is:

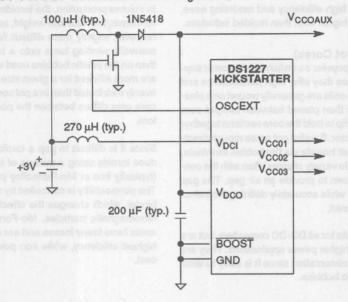
$$E_L = \frac{L I_{PK}^2}{2}$$

At maximum load this cycle is repeated  $f_0$  (typically 40 KHz) times per second, and the power transferred through the coil is  $P_L = f_0 \times E_L$ . Since the coil only supplies the voltage above the input voltage:

$$I_{OUT} = \frac{P_L}{V_{OUT} - V_{IN}}$$

## **DC-DC CONVERTER** Figure 7





The DC-DC converter's output current is provided both by the inductor and directly from the battery. If the load draws less than the maximum current, the V<sub>DCI</sub> n-channel MOSFET is turned on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the DS1227 will not be able to deliver the desired output power, even with the MOSFET turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

$$\begin{split} \mathsf{L}_{\mathsf{MAX}} \ &= \frac{\mathsf{V_{IN}}^2}{8 \; \mathsf{f_O} \; \mathsf{P_L}} \\ \\ \mathsf{since} : \; \mathsf{P_L} \ &= \frac{\mathsf{L} \; \mathsf{I_{PK}}^2 \; \mathsf{f_O}}{2} \; \mathsf{and} : \; \mathsf{I_{PK}} \ &= \frac{\mathsf{V_{IN}}}{2} \; \mathsf{f_O} \; \mathsf{L} \end{split}$$

The required output power must include what is dissipated in the forward drop of the catch diode and each of the  $V_{\rm CCO1}$ ,  $V_{\rm CCO2}$ , and  $V_{\rm CCO3}$  pass transistors. This can be expressed as follows:

where:

If the inductance value is too low, the current at V<sub>DCI</sub> may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}}{2 f_0 I_{MAX}} (I_{MAX} + 450 mA)$$

#### TYPES OF INDUCTORS

The following is a brief discussion of various types of inductors which may be typically used with the DS1227 Kickstarter to facilitate boost mode operation. Table 1 lists some typical manufacturers of these types of inductors. Table 2 summarizes performance of the circuit for various inductors.

#### **Molded Inductors**

These are cylindrically wound coils which look similar to 1-watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types of inductors.

#### **Potted Toroidal Inductors**

A typical 1 mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685 in diameter by 0.385 high and

mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

#### **Ferrite Cores (Pot Cores)**

Pot cores are very popular as switch-mode power supply applications since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

#### Toroldal Cores

In volume production, the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective core area differs between the post, side, top, and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permally powder (MFP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

**COIL AND CORE MANUFACTURERS** Table 1

TYPE	TYPICAL MANUFACTURER	PART#	DESCRIPTION	
Molded	Dale	1HA-104	500 μH, 0.5 ohms	
ang, mer manum	Cadell-Burns	7070-29	220 μH, 0.55 ohms	
11	Gowanda	1B253	250 μH, 0.44 ohms	
* (Am. 03)	Nytronics	WEE-470	470 μH, 10 ohms	
"	TRW	LL-500	500 μH, 0.75 ohms	
Potted Toroidal	Dale	TE-3Q4TA	1 mH, 0.82 ohms	
o asovi acciss vio no	Gowanda	050AT1003	100 μH, 0.05 ohms	
used with the DS1	the local a TRW related and solve	MH-1	600 μH, 1.9 ohms	
ede operation. Tabl	Torotel Prod.	PT 53-18	500 uH, 5 ohms	
Toroidal Core	Allen Bradley	T0451S100A	500 nH/T <sup>2</sup>	
" SUPERING	Siemans	B64290-K38-X38	4 μH/T <sup>2</sup>	
**	Magnetics	555130	53 nH/T <sup>2</sup>	
Ferrite Core	Stackpole	57-3215	14 mm x 8 mm	
olls which look almite	Magnetics	G-41408-25	14 x 8, 250 nH/T <sup>2</sup>	

Note: This list does not constitute an endorsement by Dallas Semiconductor and is not intended to be a comprehensive list of all manufacturers of these components.

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#### **INDUCTOR SELECTION FOR COMMON DESIGNS** Table 2

VIN	V <sub>DCO</sub>	I <sub>OUT</sub>	EFF.	INDUCTOR		
(V)	(V)	(mA)	(%)	PART#	uH	Ohms
2	5	5	78	CB 6860-21	470 0	
2	5	10	74	G 1B253	250 0.4	
2	5	15	61	G 1B103	03 100	
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55

Note:

CB = Cadell-Burns, NY (516) - 746 -2310

G = Gowanda Electronics Corp., NY (716) - 532-2234

Other manufacturers listed in Table 1.

#### **OUTPUT FILTER CAPACITOR**

In boost regulation mode, the DS1227's output voltage ripple on  $V_{\rm DCO}$  has two components, with approximately  $90^{\rm o}$  phase difference between them. One component is created by the change in the capacitor's stored charge with each output pulse. The other ripple component is the product of the capacitor's charge/discharge current and its ESR (Effective Series Resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than that caused by the change in charge.

$$V_{ESR} = I_{PK} \times ESR = \frac{V_{IN}}{2Lf_O} \times ESR \text{ (Volts p - p)}$$

Where  $V_{\text{IN}}$  is the coil input voltage, L is its inductance, f is the oscillator frequency, and ESR is the equivalent series resistance of the filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C}$$
 where,  $Q = \frac{t_{DIS} \times I_{peak}}{2}$ 

and, 
$$I_{peak} = \frac{t_{CHG} \times V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN} \times t_{CHG} \times t_{DIS}}{2IC}$$

Where  $t_{CHG}$  and  $t_{DIS}$  are the charge and discharge times for the inductor 1/2  $t_{O}$  can be used for nominal calculations).

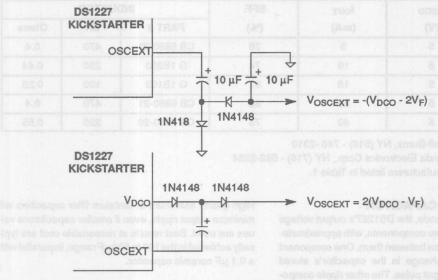
High quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved in the 100 to 500  $\mu$ F range, in parallel with a 0.1  $\mu$ F ceramic capacitor.

#### **OSCEXT FUNCTIONS**

The OSCEXT pin is connected to the internal 40 KHz oscillator (nominal frequency). When Boost mode is enabled (BOOST = 0) and the DC-to-DC converter is running, OSCEXT is active at the same time whenever the error comparator is switched high, i.e., whenever the internal oscillator is enabled to the gate of the VDCI driver. In this configuration it may be used to drive an auxiliary switch mode boost regulator as shown in Figure 8. In this circuit, OSCEXT drives an external NMOS switch with its drain pin connected to an additional inductor and filter capacitor as well as an external catch diode. The amount of supply current which can be realized at the +5V output is determined by the power ratings of the external components. Through proper selection of the these components, increased supply current can be realized than is possible using the Kickstarter's internal V<sub>DCI</sub> driver and catch diode.

When the Pass-Through mode is enabled ( $\overline{BOOST}=1$ ) and at least one of the V<sub>CCO</sub> outputs is switched on, the OSCEXT pin will be continuously driven with the 40 KHz frequency. In this configuration this pin could potentially be used to generated negative or doubled voltages as shown in Figure 9.

#### **VOLTAGE INVERTOR AND DOUBLER CONFIGURATIONS** Figure 9



NOTE: VF = FORWARD 1N418 DIODE VOLTAGE

#### **APPLICATION BRIEF**

The schematic shown in Figure 10 illustrates a typical application of the DS1227 Kickstarter in a microcontroller-based, battery powered system. Together with the Kickstarter, the system incorporates a DS5000FP Soft Microcontroller, a DS1283 Watchdog Timekeeper, and a DS1275 Line Powered RS232 Transceiver. Although the system is not designed to serve a specific application, this chip set could serve the majority of requirements for many types of hand-held instruments.

Using the illustrated configuration provides the following major features:

- Permanently powered operation from a +3V source for many applications
- Data and event logging with time stamp and date
- Reprogrammable through RS232 serial interface
- Buttonless (autonomous) operation for many tasks

#### COMPONENT DESCRIPTION

The DS5000FP is an 8-bit microcontroller which is instruction set-compatible with the industry standard

8051. It provides an embedded interface to 32 Kbytes of nonvolatile static RAM which can be dynamically partitioned for program and data storage, and may be loaded at any time via the on-chip serial port. With proper selection of RAM and the backup lithium source, nonvolatile storage can be maintained for over 10 years in the absence of  $V_{\rm CC}$ . The DS5000FP offers the standard low power operating and standby modes (i.e., Idle, Stop). More importantly, sophisticated crashproof circuitry in conjunction with the lithium energy source allows it to retain its entire operating state for the duration of a power outage without drawing current from its  $V_{\rm CC}$  line.

Timekeeping is provided by the DS1283 Watchdog Timekeeper. Incorporating a self-contained clock and calendar, the DS1283 tracks hundredths of seconds, seconds, minutes, hours, days, date of the month, month, and years. When its chip enable is inactive (no read or write), the DS1283 consumes extremely low current, typically 500 nA. Two alarm functions are provided: a time-of-day Alarm, and a watchdog alarm. The time-of-day Alarm can generate an interrupt pulse up to one week in advance of the current time. The watchdog alarm can produce an interrupt at regular intervals ranging from .01 seconds to 99.99 seconds. Both alarms function when the part is operating in low power standby mode.

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The DS1275 Line Powered RS232 Transceiver allows the instrument to communicate with the RS232 port on a host computer (e.g., COM port on an IBM PC). It operates from a +5V supply and draws no power from the instrument's main energy source to create negative voltages. Instead, it steals power from the incoming RXD line to generate the negative voltages needed during transmission.

#### **INSTRUMENT OPERATION**

A common requirement of instruments is event logging with time stamp and date. The Dallas chip set provides this capability using the DS5000 and DS1283. The DS1283 interfaces directly to the DS5000FP embedded bus, and may be accessed by CE2. In this way, valuable port pins are conserved. Events can be recorded by the microcontroller and logged in RAM with the date and time. In the absence of V<sub>CC</sub>, the data will be retained in RAM by the backup lithium cell. The same energy cell provides backup to the DS1283, so that timekeeping is maintained in the absence of a primary energy source. Therefore, events may be time stamped and dated with confidence that the correct time has been maintained. Backup lithium current is managed by the DS5000FP and is distributed from the V<sub>CCO</sub> line in the absence of Vcc.

#### PERMANENTLY POWERED OPERATION

In order to achieve permanently powered operation, Dallas Semiconductor uses several techniques which conserve the life of a primary energy source. First, the illustrated chip set operates at extremely low power. These components are also capable of very low power data retention. Second, the crashproof circuitry of the DS5000 allows V<sub>CC</sub> to be removed and restored without disruption. This allows the energy management circuits of the Kickstarter to power down the microcontroller during periods when it is unused. Since the DS1227 can monitor external events and wakeup the DS5000 as necessary, the microcontroller and other circuitry may remain in low power data retention mode until needed. The DS5000, RAM, and DS1283 will be backed up via the button cell as show in Figure 1. Finally, the Kickstarter allows software-controlled powering of auxiliary circuits when tasks require them.

Low operating power is a basic requirement of batteryoperated systems. The illustrated Dallas chip set can perform most instrument functions using minimal power. Using a 3.57 MHz crystal, the circuit in Figure 1 will draw approximately 8 mA during microcontroller operation. When the Kickstarter turns off the DS5000, the circuit draws approximately 5  $\mu A$  from the primary energy source. If a similar configuration were created with an ordinary CMOS microcontroller in stop mode, the current could be as high as 55  $\mu A$ . Idle mode operation would consume approximately 3 mA, which would excessively drain a primary power source over extended periods. The Dallas low power chip set provides a tento-one improvement over previously available alternatives.

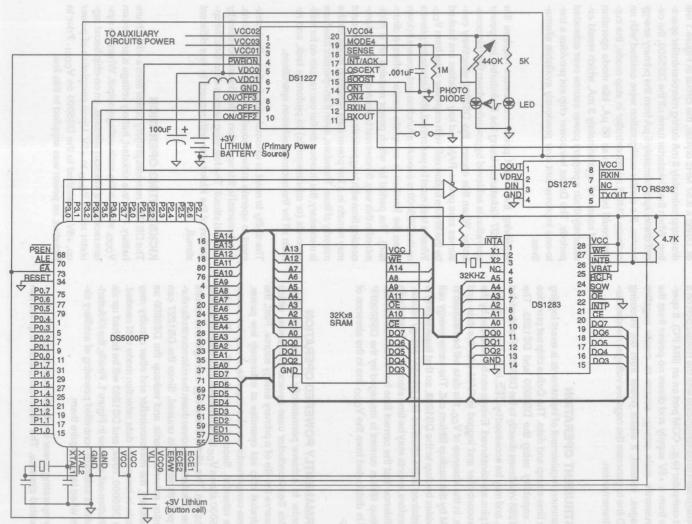
Achieving the lowest power instrument requires the DS1227 Kickstarter. Using the Kickstarter, low power operation is achieved by powering down the microcontroller. When this occurs, the DS5000 effectively consumes zero power. RAM and key registers are backed by the lithium button cell, with no power draw from V<sub>CC</sub>. When a task must be performed, the Kickstarter powers up the DS5000 to execute a function and powers it down when the function is complete (under software direction). The period for which power remains on is minimized in this way. Since most tasks require minimal processing time with long periods of waiting, the instrument may remain in a low power data retention mode for the majority of time. Therefore, even if an operator interface is necessary, the microcontroller can remain on for milliseconds (or microseconds) to perform a task, and remain off for the seconds between operations.

The ability to react to external stimuli allows the instrument to operate autonomously for many applications. Fundamental to this operation is the kickstart caused by external stimuli. The following section describes the operation of the Kickstarter with respect to four different stimuli.

#### KICKSTARTING OPERATION

The DS1227 receives primary power from a +3V lithium battery. Prior to a kickstart, battery voltage is present on V<sub>DCO</sub>, which is the main voltage output. When the system receives a kickstart stimulus, an on-chip boost regulator raises V<sub>DCO</sub> to +5V. Upon completion of power up, +5V is switched to the DS5000 on V<sub>CC01</sub>. Prior to kickstart, no power was supplied to this line.

# TYPICAL APPLICATION OF DS1227 KICKSTARTER Figure 10



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The schematic in Figure 1 demonstrates four kickstart stimuli. They are real time clock alarm, RS232 incoming data, a sensor input, and a user switch. During the low power standby prior to kickstart, V<sub>CCO</sub> from the DS5000 provides battery power to the RAM and real time clock from the button cell. V<sub>DCO</sub> supplies the RS232 transceiver. While operating on battery power, the RTC can still issue alarms. If a time of day alarm is programmed, INTA will be taken low by the RTC when the alarm occurs. Th is is connected to ON1, and issues a Kickstart.

Incoming RS232 activity will allow the transceiver to Kickstart the DS1227. Following the initial interrupt, all additional RS232 data is passed through the RXIN/RXOUT pins of the DS1227 to the DS5000 without further action. In this way, the instrument can collect a table of data and dump it to a PC for analysis when necessary. Since the instrument will kickstart when it detects RS232 communication, it is unnecessary for an operator to take further action. Enough time should be allowed for the DS5000 to complete a power-on reset before sending meaningful data.

Two additional methods of kickstarting are illustrated. One method involves the use of a sampled sensor. Aperiodic pulse (the watchdog alarm) from the DS1283 causes V<sub>CC04</sub> to be applied to the LED. For example, this might occur every 250 ms. It remains on for the time it takes to charge the capacitor on Mode4 to 1/2 VDCO (1.5V). In this example, the on period is approximately 75 µsec. Just prior to removing V<sub>CC04</sub>, the sense line is sampled. If the LED light path to the photodiode is blocked, the sense line will be high and the system will be kickstarted. If the light path is clear, the sense line will be low, and nothing will happen. This facilitates checking for the presence of an ID card in a reader. In the other method a user switch, which is momentarily closed, will start the system. This is tied to ON1 in a wired-OR configuration. All of the above kickstart stimuli cause the boost regulator to raise VDCO and turn on VCC01. In summary, the four kickstart stimuli are:

- Time of Day Alarm INTA goes low and Kickstarts Vcco1.
- 2) RS232 Activity Powers up  $V_{\text{CC01}}$  and routes all RS232 straight through to the DS5000.
- 3) INTB goes low periodically, V<sub>CC04</sub> turns on, and the sense line is sampled. If high, a kickstart occurs. If low, no action.

A user switch momentarily pulls ON1 low and kick starts.

Although the user switch is easily implemented, it may be unnecessary. By allowing the instrument to power up and determine the cause of the Kickstart, it is possible to achieve buttonless operation in many applications. Automatic response allows the instrument to function autonomously and save power by turning off unused circuits.

Once the DS5000 receives power, it must read the INT/ ACK line (tied to INTO). A power-on condition causes this signal to be low. The DS5000 port pin should then acknowledge power up by driving this line high. This recognizes the interrupt and enables the kickstarter for further activity. The DS5000 may now turn on auxiliary loads V<sub>CC02</sub> and V<sub>CC03</sub> using ON/OFF 2 and 3 (tied to any port pins). These auxiliary supplies may supply circuits which are not always necessary (e.g. an A/D converter). Peripheral circuits remain powered down until needed. After an operation is complete, the DS5000 can turn off the auxiliary circuits. When processing of a task is complete, it may turn itself off using OFF1. An application may require that an auxiliary circuit remain on when the microcontroller is off. This might occur with an LCD display or dual slope A/D converter. Since the dual slope A/D takes a relatively long period to convert (40-50 mS), the microcontroller may be powered down while waiting.

Since the INT/ACK line is tied to INT0, additional kickstart stimuli which occur while VCC01 is on will cause the DS5000 to receive an interrupt. This allows the DS5000 to take action for specific conditions.

Precautions against excessive current drain are taken in this application. For example, the data input to the DS1275 RS232 transceiver is tri-stated when VCC01 is off. This is necessary to prevent a high signal from driving the RS232 bus and consuming power while the DS5000 is off. Similar precautions should be taken by the user in designing systems with switched power supplies.

#### **ABSOLUTE MAXIMUM RATINGS\***

Input Voltage on any Pin Relative to Ground
V<sub>DCI</sub> Peak Input Current
Power Dissipation
Plastic DIP (derate 7.41 mW/°C above +50°C)
Small Outline (derate 12.5 mW/°C above +50°C)

Small Outline (derate 12.5 mW/°C above +50°C)

Operating Temperature

Storage Temperature

Lead Soldering Temperature

-937 mW

0° to +70°C

-55°C to +125°C

260°C for 10 sec.

-0.3 to 7.0V

450 mA

- 555 mW

#### **ELECTRICAL CHARACTERISTICS**

 $(t_A = 0^\circ C \text{ to } 70^\circ C)$ 

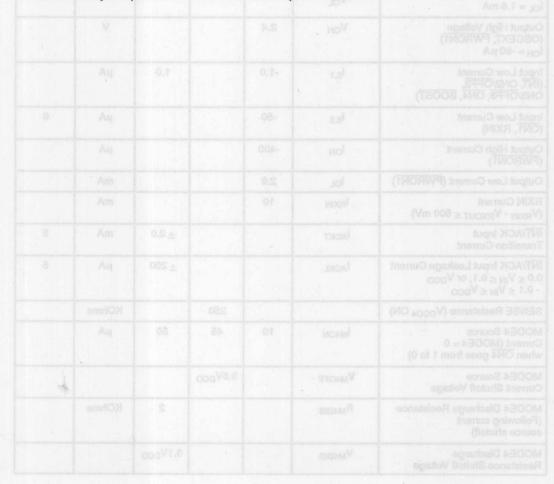
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Startup Voltage	V <sub>DCISU</sub>	1.8	de si mada	tro to vests!	V	1
V <sub>DCO</sub> Voltage Threshold for V <sub>CCO</sub> Turn-ON	V <sub>DCON</sub>	4.38	4.50	4.62	Vertex	seese comunity to take that
V <sub>DCO</sub> Voltage Threshold for V <sub>CCO</sub> Turn-OFF	V <sub>DCOFF</sub>	91069	a Jeaso no-	3.00	V	esti gribn
Operating Supply Current (BOOST=0) (BOOST=1)	lcc	o testa A per A	1.5 0.5	3.0 1.0	mA mA	4 2
Standby Supply	I <sub>SB</sub>	nple,	D. For exa	200	nA	looV acon
V <sub>CCO1</sub> DC Source Current (V <sub>CCO1</sub> = V <sub>DCO</sub> -0.25V)	I <sub>CCO1</sub>	e cody	SNT of Aub	100	mA	2,7
V <sub>CCO2</sub> , V <sub>CCO4</sub> DC Source Current (V <sub>CCO2</sub> , V <sub>CCO4</sub> = V <sub>DCO</sub> - 0.25V)	Icco2 Icco4	el els	sense erit olbotoriq a atawa ark b	50	mA	2,7
V <sub>CCO3</sub> Source Current (V <sub>CCO3</sub> = V <sub>DCO</sub> - 0.25V)	I <sub>CCO3</sub>	tilst er obert	il eanes ed o setalibel	10	mA	2,7
V <sub>CCO1</sub> , V <sub>CCO2</sub> , V <sub>CCO3</sub> , V <sub>CCO4</sub> Voltage	V <sub>OUTB</sub>	4.75	5.00	5.25	V	1, 4
V <sub>CCO1</sub> , V <sub>CCO2</sub> , V <sub>CCO3</sub> , V <sub>CCO4</sub> Voltage	V <sub>OUTP</sub>	V <sub>DCO</sub> -0.25	suao flumb	I restable (	V	2
V <sub>CCO4</sub> Voltage	V <sub>OUT4</sub>	V <sub>DCO</sub> -0.25	3	us ibroite F	V	d yracim
V <sub>CCO1</sub> ON Resistance	R <sub>VCCO1</sub>	alte	EURIZI BINS	2.5	Ohms	U to emil
V <sub>CCO2</sub> , V <sub>CCO4</sub> ON Resistance	R <sub>VCCO2,4</sub>	the state of	abtum ber	5.0	Ohms	M OPOSITI
V <sub>CCO3</sub> ON Resistance	R <sub>VCCO3</sub>		.00	25	Ohms	nde SiSSR
Efficiency		editio	80	ally, Vocas	%	1,8

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Line Regulation +0.5V <sub>CCO</sub> < +V <sub>S</sub> < V <sub>CCO</sub>	V <sub>cco</sub>	ri si nolta:	ngo ebom d	0.4	%	1 Adeplicable
Oscillator Frequency			40	.V0.8≥0	KHz	Valid when
Oscillator Duty Cycle	ol = 2009 l = 200	= roaal	50	stego eboli	%	pénusaold
OSCEXT ON Resistance	Roscext	s of DO-to	50	75	Ohms	i seob ton
V <sub>DCI</sub> Driver ON Resistance (@ I <sub>VDCI</sub> = 100 mA)	R <sub>VDCION</sub>	pacified (b	6	12	Ohms	Inp <b>I</b> t tyani pin from a
V <sub>DCI</sub> Driver OFF Leakage Cur- rent (t <sub>A</sub> = 25° C)	IVDCIL	iveb cu-llus	g lennario-q	30	μА	bna FVO
Catch Diode Forward Voltage	o bello V <sub>F</sub> them.	benichno	i, tine total ex	1.0	day V	When BO
Output Low Voltage, (OSCEXT, PWRON1) I <sub>OL</sub> = 1.6 mA	V <sub>OL</sub>	etia comp	anens. Atemai distr	0.45	yeb at yenek	Actual effic
Output High Voltage (OSCEXT, PWRON1) I <sub>OH</sub> = -80 μA	V <sub>OH</sub>	2.4			٧	
Input Low Current (INT, ON2/OFF2, ON3/OFF3, ON4, BOOST)	I <sub>IL1</sub>	-1.0		1.0	μА	
Input Low Current (ON1, RXIN)	I <sub>IL2</sub>	-50			μА	6
Output High Current (PWRON1)	I <sub>OH</sub>	-400			μА	
Output Low Current (PWRON1)	loL	2.0			mA	
RXIN Current (V <sub>RXIN</sub> - V <sub>RXOUT</sub> ≤ 500 mV)	I <sub>RXIN</sub>	10			mA	
INT/ACK Input Transition Current	I <sub>ACKT</sub>			± 2.0	mA	5
$\overline{\text{INT}}/\text{ACK}$ Input Leakage Current $0.0 \le V_{\text{IN}} \le 0.1$ , or $V_{\text{DCO}}$ - $0.1 \le V_{\text{IN}} \le V_{\text{DCO}}$	I <sub>ACKL</sub>			± 200	μА	5
SENSE Resistance (V <sub>CCO4</sub> ON)			250		KOhms	
MODE4 Source Current (MODE4 = 0 when ON4 goes from 1 to 0)	I <sub>M4ON</sub>	10	45	80	μА	
MODE4 Source Current Shutoff Voltage	V <sub>M4OFF</sub>		0.5V <sub>DCO</sub>			6
MODE4 Discharge Resistance (Following current source shutoff)	R <sub>M4DIS</sub>			2	KOhms	
MODE4 Discharge Resistance Shutoff Voltage	V <sub>M4DIS</sub>			0.1V <sub>DCO</sub>		

#### NOTES:

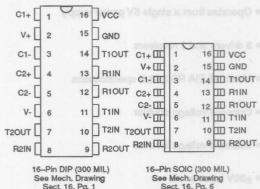
- 1. Applicable only when Boost mode operation is in effect.
- 2. Applicable only when Pass Through mode operation is in effect.
- 3. Valid when 2.5V ≤ V<sub>DCO</sub> ≤ 5.0V.
- 4. Measured with Boost Mode operation in effect; I<sub>CCO1</sub> = I<sub>CCO2</sub> = I<sub>CCO3</sub> = I<sub>CCO4</sub> = 0. This value represents the amount of current drawn by the DS1227 itself during and does not include current supplied on the I<sub>CCO</sub> outputs nor does if boost operator includes inefficiencies of DC-to-DC conversion.
- Input transition current on the INT/ACK pin is specified to indicate the amount of current required to switch the pin from a high to a low or from a low to a high condition. Once the pin has switched states, then the leakage current specification is applicable.
- 6. ON1 and RXIN have internal weak p-channel pull-up devices.
- 7. When BOOST operation is in effect, the total combined current supplied out of  $V_{CCO1}$ ,  $V_{CCO2}$ ,  $V_{CCO3}$ , and  $V_{CCO4}$  is limited by the  $V_{DCI}$  peak current.
- 8. Actual efficiency is dependent on external discrete component characteristics.



#### **FEATURES**

- Operates from a single 5V power supply
- Two drivers and two receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ± 30V input levels
- ± 9V output levels with + 5V supply
- Low-power CMOS
- Pin-compatible with the MAX 232
- Optional 16-pin SOIC surface mount package

#### PIN ASSIGNMENT



Sect. 16, Pg. 1

Sect. 16, Pg. 6

#### PIN DESCRIPTION

C1+, C1 C2+, C2 V+, V-T1IN, T2IN T10UT, T20UT R1IN, R2IN R10UT, R20UT Vcc GND

Capacitor 1 Connections Capacitor 2 Connections ± 10 Volts Transmitter In Transmitter Out Receiver In Receiver Out +5 Volts Ground

#### DESCRIPTION

The DS1228 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single, +5 volt supply. The DS1228 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate -10 volts. The DS1228 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ± 9V RS-232 outputs. The other two level translators are capable of operating with up to ±30 V inputs. The DS1228 is suitable for all RS-232 communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1228 supplies ± 10 volts from the V<sub>CC</sub> input.

See the DS1229 data sheet for electrical specifications and operation.

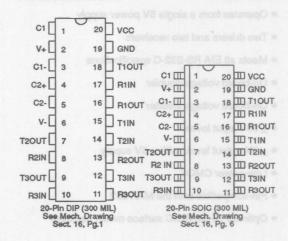


# +5V Powered Triple RS-232 Transmitter/Receiver

#### **FEATURES**

- Operates from a single 5V power supply
- 3 drivers and 3 receivers
- Meets all EIA RS\_232\_C specifications
- Onboard voltage doubler
- Onboard voltage inverter
- ±30V input levels
- ±9V output levels with ±5V supply
- Low-power CMOS
- Optional 20\_Pin SOIC surface mount package

#### **PIN ASSIGNMENT**



#### **PIN DESCRIPTION**

C1+, C1-	Capacitor 1 Connections
C2+, C2-	Capacitor 2 Connections
V+, V-	± 10 Volts
T1IN, T2IN, T3IN	Transmitter In
T1OUT, T2OUT, T3OUT	Transmitter Out
R1IN, R2IN, R3IN	Receiver In
R1OUT, R2OUT, R3OUT	Receiver Out
Vcc	+5 Volts
GND	Ground

#### DESCRIPTION

The DS1229 is a triple RS.232.C receiver/transmitter that meets all EIA specifications while operating from a single +5V supply. The DS1229 has two internal charge pumps which are used to generate ±10V. The DS1229 also contains six level translators, three of which are RS.232 transmitters that convert TTL/CMOS inputs into +9V RS.232 outputs. The other three level translators

are RS\_232 receivers that convert RS\_232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS\_232\_C communications and is particularly valuable where higher voltage power supplies for RS\_232 drivers are not available. The power supply section of the DS1229 supplies ±10V from the V<sub>CC</sub> input.

#### **OPERATION**

The DS1229 consists of three major sections: a triple transmitter, a triple receiver and a dual charge pump which generates ±10V from the 5V supply.

#### **CHARGE PUMP SECTION**

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the  $V_{\rm CC}$  input to +10V. The second charge pump uses external capacitor C2 to invert the +10V to -10V. Capacitors C3 and C4 are used to filter the +10V and -10V power supply. The recommended size of capacitors C1-C4 is 22  $\mu$ F but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the +10V supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1  $\mu$ F where size is critical.

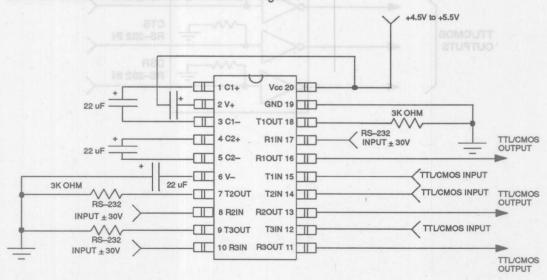
#### TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal +10V supply. The input is TTL/CMOS-compatible. Each input has an internal 750K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from  $\pm$  10V to  $\pm$  10V. Worst-case conditions for RS-232-C of  $\pm$ 5V driving a 3K load are met at maximum allowable ambient temperature and a  $V_{CC}$  level of 5.0V. Typical voltage swings of  $\pm$ 9V occur with outputs of 5K and  $V_{CC}$  equal to 5V. The slew rate at the output is limited to less than 30V/ us and the power-down output impedance will be a minimum of 300 ohms with  $\pm$  2V applied to the outputs and  $V_{CC}$  at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

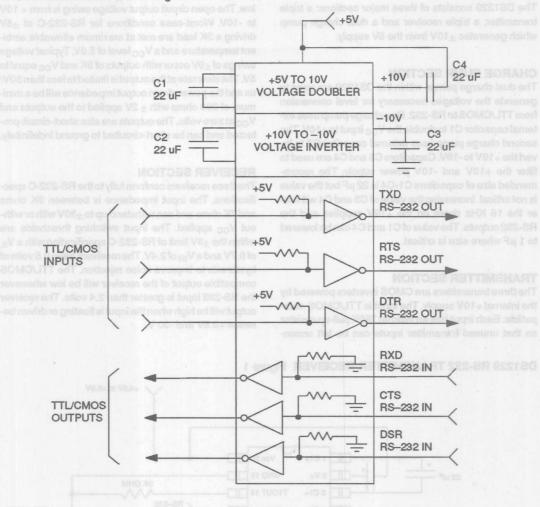
#### RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3K ohms and 7K ohms and can withstand up to  $\pm 30$ V with or without  $V_{CC}$  applied. The input switching thresholds are within the  $\pm 3$ V limit of RS-232-C specification with a  $V_{IL}$  of 0.7V and a  $V_{IH}$  of 2.4V. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8V and -30 V.

#### DS1229 RS-232 TRANSMITTER/RECEIVER Figure 1



#### TYPICAL APPLICATIONS Figure 2



#### **ABSOLUTE MAXIMUM RATINGS\***

V<sub>CC</sub>
V+
VTransmitter Inputs
Receiver Inputs
Transmitter Outputs
Receiver Outputs
Storage Temperature

7.0V +12 volts -12 volts -0.3V to (V<sub>CC</sub> +0.3V) ± 30 volts (V+ + 0.3V) to (V --0.3V) -0.3V to (V<sub>CC</sub> + 0.3V) 55°C to 125°C

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	٧	1
Logic 1 Input	V <sub>IH</sub>	2.2	eyolser Ili	V <sub>CC</sub> +0.3	V And	s to ball
Logic 0 Input	V <sub>IL</sub>	-0.3		+0.8	٧	1
RS-232 Input Voltage	V <sub>RS</sub>	-30		+30	٧	1,2,11

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS-232 Output Voltage	V <sub>ORS</sub>	±4	±9	± 10	V	3,12
Power Supply Current	I <sub>DD</sub>		5	10	mA	4
Transmitter Pull-up Current	I <sub>TP</sub>		5	200	μА	5
RS-232 Input Threshold Low	VTL	0.7	1.2		V	6
RS-232 Input Threshold High	V <sub>TH</sub>		1.7	2.4	V	6
RS-232 Input Hysteresis	V <sub>HY</sub>	0.2	0.5	1.0	V	
Receiver Output Current @ 2.4V	I <sub>ОН</sub>	-1.0			mA	
Receiver Output Current @ 0.4V	l <sub>OL</sub>			3.2	mA	
Output Resistance	Rout	300			ohms	7
RS-232 Output Current @ 0.4 V	Isc			± 25	mA	
Propagation Delay	t <sub>PD</sub>		3		μS	8
Transmitter Output Instanta- neous Slew Rate	tsR			30	V/µS	9
Transmitter Output Transition Slew Rate	t <sub>TSR</sub>		3		V/µS	10

#### NOTES

- 1. All voltages are referenced to ground.
- 2. Applies to Receiver Inputs only.
- 3. T1, T2, and T3 loaded with 3K ohms to ground.
- 4. All outputs are unloaded.
- 5. T1, T2, and T3 Inputs = 0 volts.
- 6.  $V_{CC} = +5$  volts.
- 7.  $V_{OUT} = \pm 2$  volts.
- 8. RS-232 to TTL or TTL to RS-232.
- 9.  $C_L = 10 \text{ pF}$ ,  $R_L = 3\text{K}$ ,  $t_A = 0^{\circ}\text{C}$ . This parameter is sample tested only.
- 10. R<sub>L</sub> = 3K, C<sub>L</sub> = 2500 pF measured from +3 volts to -3 volts or -3 volts to +3 volts.
- 11. This parameter is sample tested only.
- 12. Negative output level of -5V is increased to -4.0 for the DS1229 only. Positive output level remains at +5V. Use of a +10%, -5% power supply will restore the negative level to -5V.

						SETOM.	
	erV.						
				3.6			



# DS1231/S Power Monitor Chip

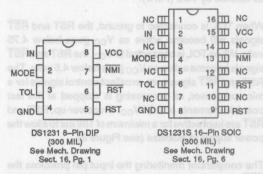
#### **FEATURES**

- · Warns processor of an impending power failure
- · Provides time for an orderly shutdown
- Prevents processor from destroying nonvolatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V<sub>CC</sub> monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

#### DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature-compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor

#### PIN ASSIGNMENT



#### PIN DESCRIPTION

LIM DES	CRIPTION
IN and	of - Input metables level a of allel (g
MODE	- Selects input pin characteristics
TOL	- Selects 5% or 10% V <sub>CC</sub> detect
GND	- Ground
RST	- Reset (Active High)
RST	- Reset (Active Low, open drain)
NMI	- Nonmaskable interrupt
V	- 15 V Supply

- No Connections

shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V<sub>CC</sub> falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the

system from inadvertent data changes.

#### **OPERATION**

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring  $V_{CC}$  (Pin 8). The  $V_{CC}$  comparator outputs the signals RST (Pin 5) and  $\overline{RST}$  (Pin 6) when  $V_{CC}$  falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and  $\overline{RST}$  signals will become active as  $V_{CC}$  goes below 4.75 volts. When TOL is connected to  $V_{CC}$ , the RST and  $\overline{RST}$  signals become active as  $V_{CC}$  goes below 4.5 volts. The RST and  $\overline{RST}$  signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid  $V_{CC}$ . On power-up, RST and  $\overline{RST}$  are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the NMI signal (Pin 7) when the input threshold voltage (V<sub>TP</sub>) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V<sub>CC</sub>, detection occurs at V<sub>TP</sub>-. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V<sub>TP+</sub>. In this mode Pin 1 sources 30 μA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between NMI and RST. On power-up, NMI is released as soon as the input threshold voltage (VTP) is achieved and V<sub>CC</sub> is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

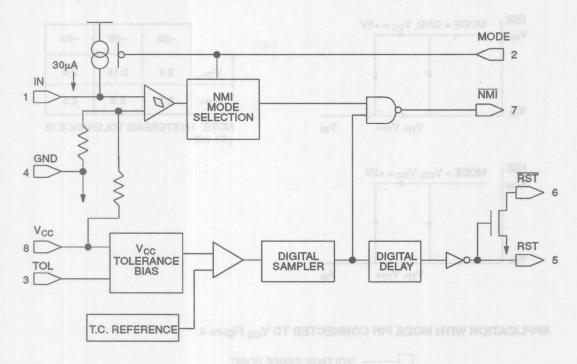
# APPLICATION - MODE PIN CONNECTED TO V<sub>CC</sub>

When the Mode pin is connected to V<sub>CC</sub>, pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

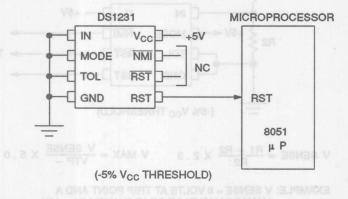
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V<sub>TP</sub>- is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0=.46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate  $\overline{\text{NMI}}$ .

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high enough impedance to keep power consumption low, and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to  $V_{\rm CC}$ .

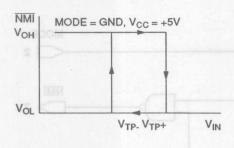
# **POWER MONITOR BLOCK DIAGRAM Figure 1**



# **POWER-UP RESET** Figure 2

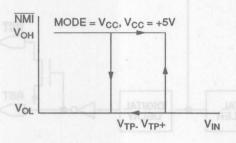


# **INPUT PIN HYSTERESIS** Figure 3

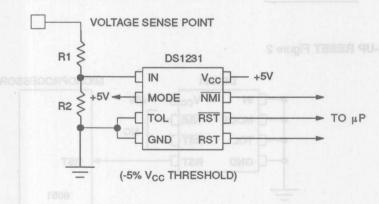


	-20	-35	-50
V <sub>TP-</sub>	2.3	2.15	2.0
V <sub>TP</sub> +	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS +60 mV



# APPLICATION WITH MODE PIN CONNECTED TO VCC Figure 4



$$V \text{ SENSE} = \frac{R1 + R2}{R2} \text{ X 2.3} \qquad V \text{ MAX} = \frac{V \text{ SENSE}}{VTP -} \text{ X 5.0}$$

EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

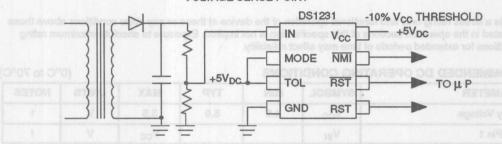
THEN 8 = 
$$\frac{R1 + 10K}{10K}$$
 X 2 . 3 R1 = 25K

## APPLICATION - MODE PIN CONNECTED TO GROUND

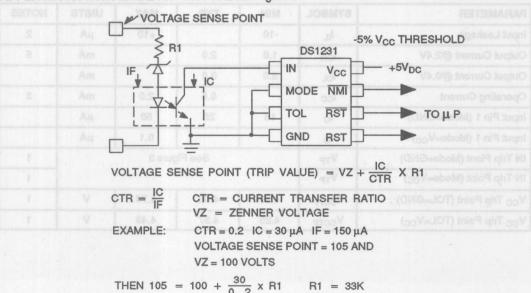
When the Mode pin is connected to ground, pin 1 is a current source of 30 µA with a V<sub>TP</sub>+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 µA of collector current required by pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

# **AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5**

#### **VOLTAGE SENSE POINT**

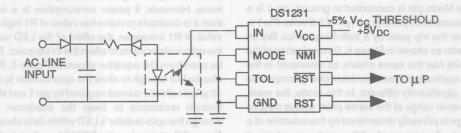


# **APPLICATION WITH MODE PIN GROUNDED Figure 6**



R1 = 33K

# AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground **Operating Temperature** Storage Temperature Soldering Temperature

-0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 sec

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Input Pin 1	V <sub>IN</sub>			Vcc	V	1

# DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V<sub>CC</sub> = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-10		+10	μА	2
Output Current @2.4V	Іон	1.0	2.0	13	mA	5
Output Current @0.4V	loL	2.0	3.0	477,31	mA	
Operating Current	Icc	W	0.5	2.0	mA	3
Input Pin 1 (Mode=GND)	lc	15	25	50	μА	
Input Pin 1 (Mode=V <sub>CC</sub> )	Talc	(B)		0.1	μА	
IN Trip Piont (Mode=GND)	V <sub>TP</sub>	See Figure 3			1	
IN Trip Point (Mode=V <sub>CC</sub> )	V <sub>TP</sub>	VOLTAGE SENSE POINT (TRIP VAL				1
V <sub>CC</sub> Trip Point (TOL=GND)	V <sub>CCTP</sub>	4.50	4.62	4.74	V	1
V <sub>CC</sub> Trip Point (TOL=V <sub>CC</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.49	V	1

#### CAPACITANCE

12		OF	001
AJ	=	20	°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

#### AC ELECTRICAL CHARACTERISTICS

	(0°C to	70°C.	Vcc =	5V +	10%)
--	---------	-------	-------	------	------

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>TP</sub> to NMI Delay	t <sub>IPD</sub>			1.1	μѕ	
V <sub>CC</sub> Slew Rate 4.75-4.25V	t <sub>F</sub>	300			μs	
V <sub>CC</sub> Detect to RST and RST	t <sub>RPD</sub>			100	ns	Teal is
V <sub>CC</sub> Detect to NMI	t <sub>IPU</sub>			200	μѕ	4
V <sub>CC</sub> Detect to RST and RST	t <sub>RPU</sub>	150	500	1000	ms	4
V <sub>CC</sub> Slew Rate 4.25-4.75V	t <sub>R</sub>	0			ns	10-17-

#### NOTES:

- 1. All voltages referenced to ground.
- 2.  $V_{CC} = +5.0$  volts with outputs open.
- 3. Measured with outputs open.
- 4.  $t_R = 5 \, \mu s$ .
- 5. RST is an open drain output.

# **TIMING DIAGRAM-POWER-UP**

MODE=V<sub>CC</sub>
INPUT PIN 1
MODE=GND

t<sub>R</sub>

4.5V

4.75V

V<sub>CC</sub>

V<sub>OH</sub>

10

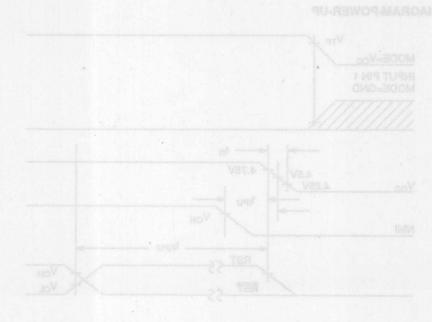
VOH

VOL

RST

**t**RPU

# TIMING DIAGRAM-POWER-DOWN VTP **INPUT PIN 1** MODE=VCC INPUT PIN 1 VTP: MODE=GND t<sub>IPD</sub> NMI VOL Vcc 4.75V 4.5V 4.25V - t<sub>RPD</sub> RST VOH VOL RST



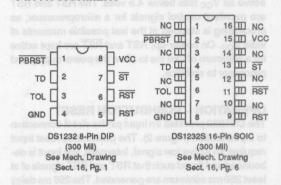


# DS1232 MicroMonitor Chip

#### **FEATURES**

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

#### PIN ASSIGNMENT



#### **PIN DESCRIPTION**

PBRST - Pushbutton Reset Input

TD - Time Delay Set

TOL - Selects 5% or 10% V<sub>CC</sub> Detect

GND - Ground

RST - Reset Output (Active High)

RST - Reset Output (Active Low, Open Drain)

ST - Strobe Input

V<sub>CC</sub> -+5 Volt Power

NC - No Connections

10

#### DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of  $V_{CC}$ . When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When  $V_{CC}$  returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

#### **OPERATION - POWER MONITOR**

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When  $V_{CC}$  falls below a preset level as defined by TOL (Pin 3), the  $V_{CC}$  comparator outputs the signals RST (Pin 5) and  $\overline{RST}$  (Pin 6). When TOL is connected to ground, the RST and  $\overline{RST}$  signals become active as  $V_{CC}$  falls below 4.75 volts. When TOL is connected to  $V_{CC}$ , the RST and  $\overline{RST}$  signals become active as  $V_{CC}$  falls below 4.5 volts. The RST and  $\overline{RST}$  are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid  $V_{CC}$ . On power-up, RST and  $\overline{RST}$  are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

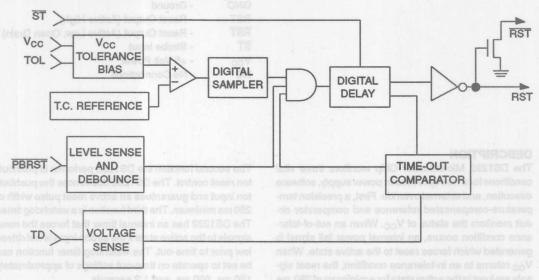
#### **OPERATION - PUSHBUTTON RESET**

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and RST signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

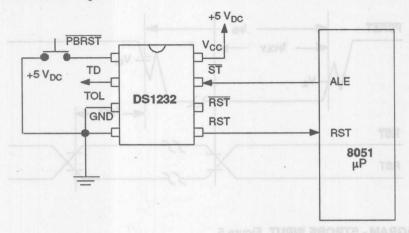
#### **OPERATION - WATCHDOG TIMER**

A watchdog timer function forces RST and RST signals to the active state when the ST input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V<sub>CC</sub>. The watchdog timer starts timing out from the set time period as soon as RST and RST are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and RST signals are driven to the active state for 250 ms minimum. The ST input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

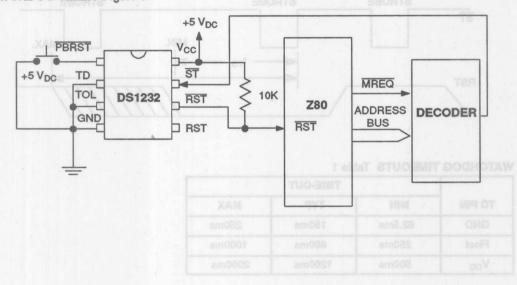
# **MICROMONITOR BLOCK DIAGRAM** Figure 1



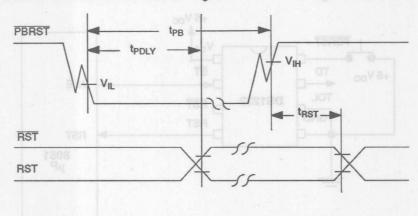
# **PUSHBUTTON RESET** Figure 2



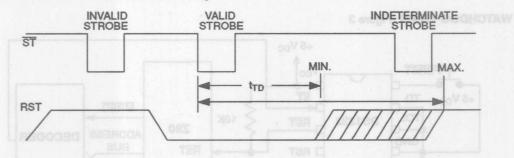
# **WATCHDOG TIMER** Figure 3



# TIMING DIAGRAM - PUSHBUTTON RESET Figure 4



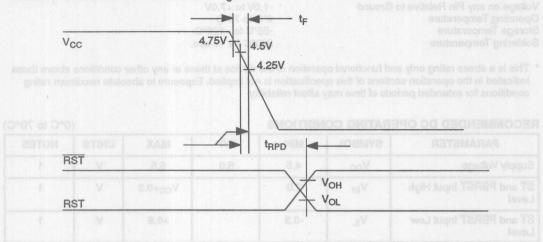
# TIMING DIAGRAM - STROBE INPUT Figure 5



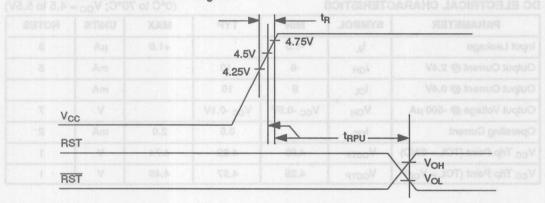
## **WATCHDOG TIMEOUTS** Table 1

TD PIN	TIME-OUT					
	MIN	ТҮР	MAX			
GND	62.5ms	150ms	250ms			
Float	250ms	600ms	1000ms			
Vcc	500ms	1200ms	2000ms			

## **TIMING DIAGRAM - POWER DOWN Figure 6**



#### **TIMING DIAGRAM - POWER UP Figure 7**



# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 sec.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
ST and PBRST Input High Level	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	1
ST and PBRST Input Low Level	V <sub>IL</sub>	-0.3		+0.8	V	1

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CC</sub> = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-1.0	VEA	+1.0	μА	3
Output Current @ 2.4V	I <sub>OH</sub>	-8	-10	1	mA	5
Output Current @ 0.4V	l <sub>OL</sub>	8	10		mA	
Output Voltage @ -500 μA	V <sub>OH</sub>	V <sub>CC</sub> -0.5V	V <sub>CC</sub> -0.1V		V	, 7
Operating Current	Icc		0.5	2.0	mA	2
V <sub>CC</sub> Trip Point (TOL = GND)	V <sub>CCTP</sub>	4.50	4.62	4.74	V	_ 1
V <sub>CC</sub> Trip Point (TOL = V <sub>CC</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.49	V	1

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CIN	5	pF	
Output Capacitance	C <sub>OUT</sub>	7	pF	

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST = V <sub>IL</sub>	t <sub>PB</sub>	20		3	ms	MICON
RESET Active Time	t <sub>RST</sub>	250	610	1000	ms	
ST Pulse Width	t <sub>ST</sub>	20			ns	6
V <sub>CC</sub> Detect to RST and RST	t <sub>RPD</sub>	20 A 1007		100	ns	onoura
V <sub>CC</sub> Slew Rate 4.75V to 4.25V	t <sub>F</sub>	300		of DS1292.	μs	oq-wol requ
V <sub>CC</sub> Detect to RST and RST Transition	t <sub>RPU</sub>	250	610	1000	ms	4
V <sub>CC</sub> Slew Rate 4.25V to 4.75V	t <sub>R</sub>	0	5 after power	osseourquio	μѕ	vilacitemetu
PBRST Stable Low to RST and RST	tPDLY	Пань	d	20	ms	lauq enotino

#### NOTES:

- 1. All voltages referenced to ground.
- 2. Measured with outputs open.
- 3. PBRST is internally pulled up to V<sub>CC</sub> with an internal impedance of 10K typical.
- 4.  $t_R = 5 \, \mu s$ .
- 5. RST is an open drain output.
- 6. Must not exceed t<sub>TD</sub> minimum. See Table 1.
- RST remains within 0.5 of V<sub>CC</sub> on power-down until V<sub>CC</sub> drops below 2.0V. RST remains within 0.5V of GND on power-down until V<sub>CC</sub> drops below 2.0V.

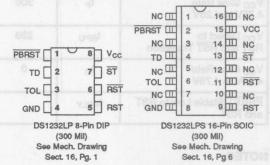


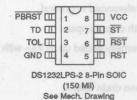
# DS1232LP/LPS Low Power MicroMonitor Chip

#### **FEATURES**

- Super low-power version of DS1232
- 50 μA quiescent current
- Halts and restarts an out-of-control microprocessor
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- 8-pin DIP or 8-pin SOIC package
- Optional 16-pin SOIC package available
- Industrial temperature -40°C to +85°C available

#### **PIN ASSIGNMENT**





Sect. 16, Pg 5

#### PIN DESCRIPTION

PBRST - Pushbutton Reset Input

TD - Time Delay Set

TOL - Selects 5% or 10% V<sub>CC</sub> Detect

GND - Ground

RST - Reset Output (Active High)

RST - Reset Output (Active Low, Open Drain)

ST - Strobe Input V<sub>CC</sub> - +5 Volt Power

#### DESCRIPTION

The DS1232LP/LPS Low Power MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V<sub>CC</sub>. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V<sub>CC</sub> returns to an in-tolerance condition, the reset signals are kept in the active state for a

minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232LP/LPS performs is pushbutton reset control. The DS1232LP/LPS debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232LP/LPS has an internal timer that forces the reset signals to the active state if

the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

**OPERATION - POWER MONITOR** 

The DS1232LP/LPS detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When  $V_{CC}$  falls below a preset level as defined by TOL, the  $V_{CC}$  comparator outputs the signals RST and  $\overline{RST}$ . When TOL is connected to ground, the RST and  $\overline{RST}$  signals become active as  $V_{CC}$  falls below 4.75 volts. When TOL is connected to  $V_{CC}$ , the RST and  $\overline{RST}$  signals become active as  $V_{CC}$  falls below 4.5 volts. The RST and  $\overline{RST}$  are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid  $V_{CC}$ . On power-up, RST and  $\overline{RST}$  are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

#### **OPERATION - PUSHBUTTON RESET**

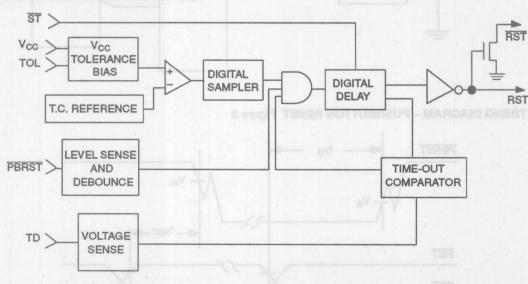
The DS1232LP/LPS provides an input pin for direct connection to a pushbutton (Figure 1). The pushbutton reset input requires an active low signal. Internally, this in-

put is debounced and timed such that RST and RST signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

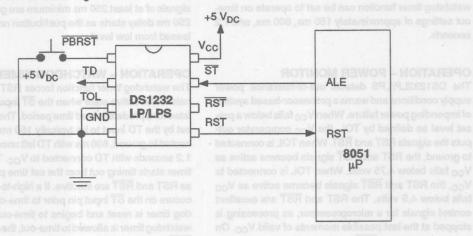
#### **OPERATION – WATCHDOG TIMER**

The watchdog timer function forces RST and RST signals to the active state when the ST input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V<sub>CC</sub>. The watchdog timer starts timing out from the set time period as soon as RST and RST are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and RST signals are driven to the active state for 250 ms minimum. The ST input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 2.

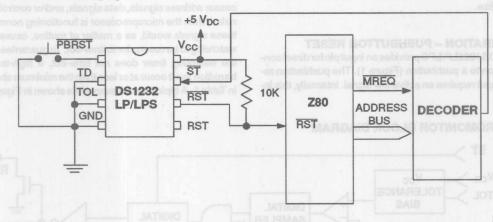
#### MICROMONITOR BLOCK DIAGRAM



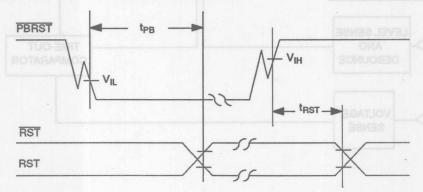
# PUSHBUTTON RESET Figure 1



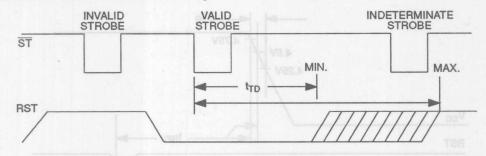
# WATCHDOG TIMER Figure 2



# TIMING DIAGRAM - PUSHBUTTON RESET Figure 3



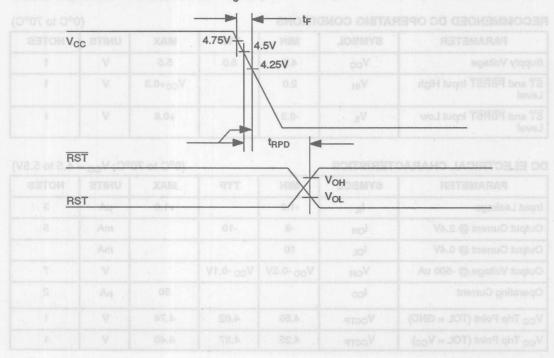
## TIMING DIAGRAM - STROBE INPUT Figure 4



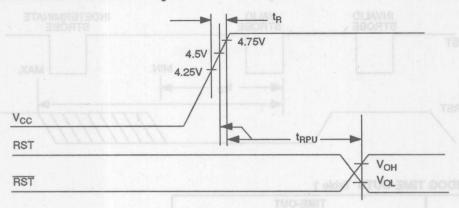
#### **WATCHDOG TIME-OUTS** Table 1

		TIME-OUT	
TD	MIN	TYP	MAX
GND	62.5ms	150ms	250ms
Float	250ms	600ms	1000ms
V <sub>CC</sub>	500ms	1200ms	2000ms

# TIMING DIAGRAM - POWER DOWN Figure 5



# TIMING DIAGRAM - POWER UP Figure 6



# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 sec.

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN va	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
ST and PBRST Input High Level	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	1
ST and PBRST Input Low Level	V <sub>IL</sub>	-0.3	4	+0.8	V	1

#### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>CC</sub> = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	IIL	-1.0		+1.0	μА	3
Output Current @ 2.4V	Юн	-8	-10		mA	5
Output Current @ 0.4V	loL	10			mA	
Output Voltage @ -500 uA	V <sub>OH</sub>	V <sub>CC</sub> -0.5V	V <sub>CC</sub> -0.1V		V	7
Operating Current	Icc			50	μА	2
V <sub>CC</sub> Trip Point (TOL = GND)	V <sub>CCTP</sub>	4.50	4.62	4.74	V	1
V <sub>CC</sub> Trip Point (TOL = V <sub>CC</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.49	V	1

#### CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>	5	pF	Котопанозия
Output Capacitance	C <sub>OUT</sub>	7	pF	

#### **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST = V <sub>IL</sub>	t <sub>PB</sub>	20			ms	erulis
RESET Active Time	t <sub>RST</sub>	250	610	1000	ms	luq anolinol
ST Pulse Width	tst	40	rlo£wa n	stiudifeug sec	ns	6
V <sub>CC</sub> Detect to RST and RST	t <sub>RPD</sub>	n	of anuder	100	ns	m anistnial
V <sub>CC</sub> Slew Rate 4.75V to 4.25V	t <sub>F</sub>	150	beasel swod V2 se	no Budrigua eniconcionalm	μs	consistor
V <sub>CC</sub> Detect to RST and RST Inactive	t <sub>RPU</sub>	250	610	1000	ms	4
V <sub>CC</sub> Slew Rate 4.25V to 4.75V	t <sub>R</sub>	0	ster egatov	betseneqmo	ns	et notploer

#### NOTES:

- 1. All voltages referenced to ground.
- 2. Measured with outputs open.
- 3. PBRST is internally pulled up to V<sub>CC</sub> with an internal impedance of 40K typical.
- 4.  $t_R = 5 \mu s$ .
- 5. RST is an open drain output.
- 6. Must not exceed to minimum. See Table 1.
- RST remains within 0.5 of V<sub>CC</sub> on power-down until V<sub>CC</sub> drops below 2.0V, RST remains within 0.5V of GND on power-down until V<sub>CC</sub> drops below 2.0V.

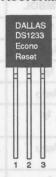


DS1233 5V EconoReset

#### **FEATURES**

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V<sub>CC</sub> returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K ohm pull-up resistor

#### **PIN ASSIGNMENT**









SOT-223 Package See Mech. Drawing Sect. 16, Pg. 19

#### PIN DESCRIPTION

PIN 1 GROUND

PIN 2 RESET

PIN3 VC

#### DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V<sub>CC</sub>). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V<sub>CC</sub>

returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

#### **OPERATION - POWER MONITOR**

The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V<sub>CC</sub> is detected as out-of-tolerance, as defined by the tolerance of the part selected, the RST signal is asserted. On power-up, RST is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before RST is released.

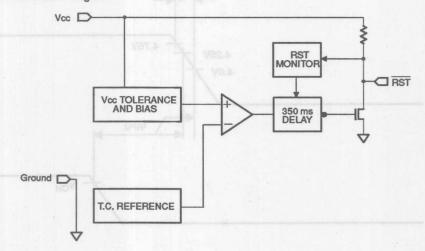
#### **OPERATION - PUSHBUTTON RESET**

The DS1233 provides for a pushbutton switch to be connected to the  $\overline{RST}$  output pin. When the DS1233 is not

in a reset cycle, it continuously monitors the RST signal for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the RST line low. After the internal timer has expired, the DS1233 will continue to monitor the RST line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the RST line low and hold it low for 350 ms.

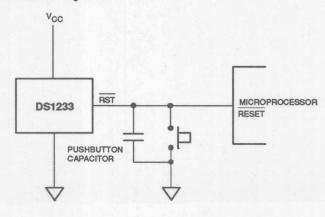
**NOTE:** For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01  $\mu$ F must be connected between  $\overline{RST}$  and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1K $\Omega$  minimum.

#### **BLOCK DIAGRAM** Figure 1

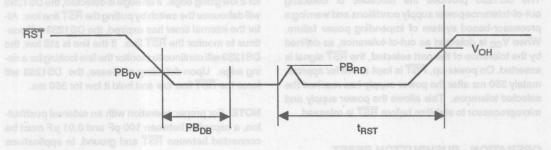


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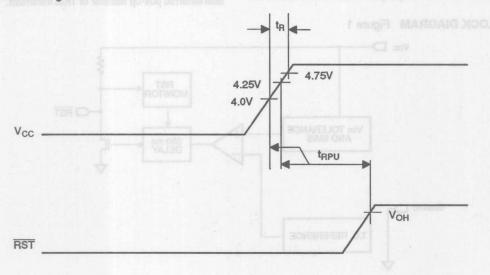
# **APPLICATION EXAMPLE** Figure 2

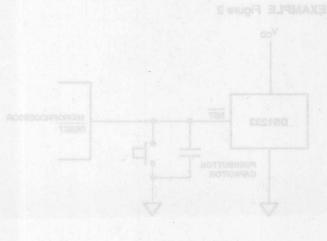


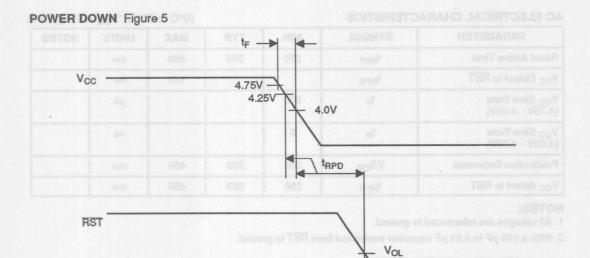
#### PUSHBUTTON RESET Figure 3



# POWER UP Figure 4







#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	1.2	5.0	5.5	Volts	1

# DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{DD} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V <sub>OL</sub>			0.4	Volts	
Output Current @ 2.4V	Іон		350		μА	
Output Current @ 0.4V	l <sub>OL</sub>	+10			mA	
Operating Current	FINANTAL.			50	μА	
V <sub>CC</sub> Trip Point 10%	V <sub>CCTP1</sub>	4.25	4.375	4.49	Volts	1.
V <sub>CC</sub> Trip Point 15%	V <sub>CCTP2</sub>	4.0	4.125	4.24	Volts	1
Output Capacitance	C <sub>OUT</sub>			10	pF	
Pushbutton Detect 10%	PB <sub>DV</sub>	1.8		3.3	Volts	1.
Pushbutton Detect 15%	PB <sub>DV</sub>	1.8		3.3	Volts	1
Pushbutton Release	PB <sub>RD</sub>		0.3	0.8	Volts	1,2
Internal Pull-Up Resistor	R <sub>P</sub>	3.75	5	6.25	KOhm	

#### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C;  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t <sub>RST</sub>	250	350	450	ms	
V <sub>CC</sub> Detect to RST	t <sub>RPD</sub>	1	4.75	100	ns	bV-
V <sub>CC</sub> Slew Rate (4.75V - 4.00V)	t <sub>F</sub>	300	4.2		μѕ	
V <sub>CC</sub> Slew Rate (4.00V - 4.75V)	t <sub>R</sub>	0			ns	
Pushbutton Debounce	PB <sub>DB</sub>	250	350	450	ms	
V <sub>CC</sub> detect to RST	t <sub>RPU</sub>	250	350	450	ms	100

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. With a 100 pF to 0.01  $\mu$ F capacitor connected from  $\overline{RST}$  to ground.

		товиля	
			Output Current @ 0.4V
			Pushbutton Dated 15%



# DS1233A 3.3V EconoReset

#### **FEATURES**

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V<sub>CC</sub> returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 3.3V power supply monitoring
- · Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K ohm pull-up resistor

#### **PIN ASSIGNMENT**









SOT-223 Package See Mech. Drawing Sect. 16, Pg. 19

#### PIN DESCRIPTION

PIN 1

GROUND

PIN 2

RESET

PIN3 Vcc

10

#### DESCRIPTION

The DS1233A EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V<sub>CC</sub>). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V<sub>CC</sub> returns to an in-tolerance condition, the reset

signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233A is pushbutton reset control. The DS1233A debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

#### **OPERATION - POWER MONITOR**

The DS1233A provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When  $V_{CC}$  is detected as out-of-tolerance, as defined by the tolerance of the part selected, the  $\overline{RST}$  signal is asserted. On power-up,  $\overline{RST}$  is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before  $\overline{RST}$  is released.

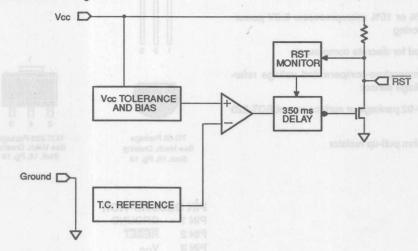
#### **OPERATION - PUSHBUTTON RESET**

The DS1233A provides for a pushbutton switch to be connected to the RST output pin. When the DS1233A is not in a reset cycle, it continuously monitors the RST

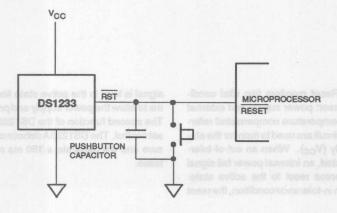
signal for a low going edge. If an edge is detected, the DS1233A will debounce the switch by pulling the RST line low. After the internal timer has expired, the DS1233A will continue to monitor the RST line. If the line is still low, the DS1233A will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233A will force the RST line low and hold it low for 350 ms.

**NOTE:** For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01  $\mu$ F must be connected between  $\overline{RST}$  and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1K $\Omega$  minimum.

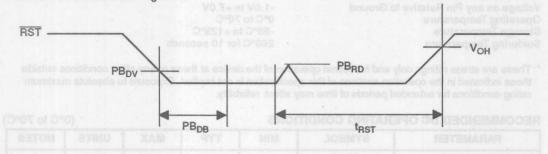
#### **BLOCK DIAGRAM** Figure 1



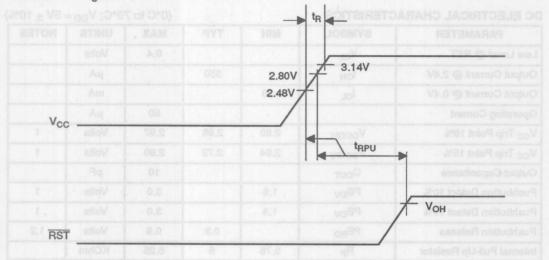
# **APPLICATION EXAMPLE** Figure 2



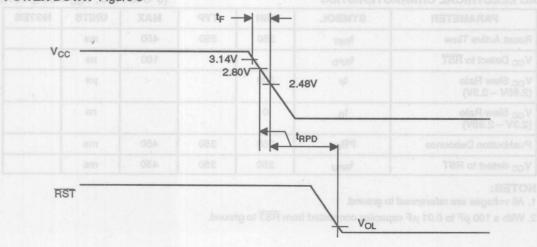
## **PUSHBUTTON RESET** Figure 3



# **POWER UP** Figure 4



# POWER DOWN Figure 5



020692 3/4

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

\* These are stress ratings only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	1.2	3.3	5.0	Volts	1

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{DD} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V <sub>OL</sub>			0.4	Volts	
Output Current @ 2.4V	ГОН	V68.3	350		μА	
Output Current @ 0.4V	loL	+10			mA	
Operating Current				50	μА	W
V <sub>CC</sub> Trip Point 10%	V <sub>CCTP1</sub>	2.80	2.88	2.97	Volts	1
V <sub>CC</sub> Trip Point 15%	V <sub>CCTP2</sub>	2.64	2.72	2.80	Volts	1
Output Capacitance	C <sub>OUT</sub>			10	pF	
Pushbutton Detect 10%	PB <sub>DV</sub>	1.8		3.0	Volts	1
Pushbutton Detect 15%	PB <sub>DV</sub>	1.8		3.0	Volts	. 1
Pushbutton Release	PB <sub>RD</sub>		0.3	0.8	Volts	1,2
Internal Pull-Up Resistor	R <sub>P</sub>	3.75	5	6.25	KOhm	

#### AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \text{ to } 70^{\circ}C; V_{CC} = 5V \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t <sub>RST</sub>	250	350	450	ms	
V <sub>CC</sub> Detect to RST	t <sub>RPD</sub>	1 F	8.14N	100	ns	100
V <sub>CC</sub> Slew Rate (2.85V – 2.3V)	t <sub>F</sub> Val	300			μs	,
V <sub>CC</sub> Slew Rate (2.3V – 2.85V)	t <sub>R</sub>	0			ns	
Pushbutton Debounce	PB <sub>DB</sub>	250	350	450	ms	
V <sub>CC</sub> detect to RST	t <sub>RPU</sub>	250	350	450	ms	

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. With a 100 pF to 0.01 μF capacitor connected from RST to ground.



# DS1236 MicroManager Chip

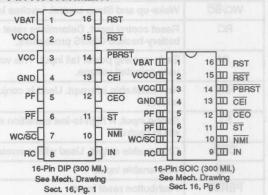
#### **FEATURES**

- Holds microprocessor in check during power transients
- · Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

#### DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a

#### **PIN ASSIGNMENT**



#### **PIN DESCRIPTION**

VBAT	+3 Volt Battery Input	
Vcco	Switched SRAM Supply Output	
Vcc	+5 Volt Power Supply Input	
GND	Ground	
PF	Power Fail (Active High)	
PF	Power Fail (Active Low)	
WC/SC	Wake-Up Control (Sleep)	
RC	Reset Control	
IN	Early Warning Input	
NMI	Non-Maskable Interrupt	
ST	Strobe Input	
CEO	Chip Enable Output	
CEI	Chip Enable Input	
PBRST	pushbutton Reset Input	
RST	Reset Output (Active Low)	
RST	Reset Output (Active High)	

non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

#### PIN DESCRIPTION

PIN NAME	DESCRIPTION			
V <sub>BAT</sub>	+3V battery input provides nonvolatile operation of control functions.			
V <sub>cco</sub>	V <sub>CC</sub> output for nonvolatile SRAM applications.			
Vcc	+5V primary power input.			
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.			
PF	Power fail indicator, active low.			
WC/SC	Wake-up and Sleep control. Invokes low-power mode.			
RC	Reset control input. Determines reset output . Normally low for NMOS processors and hig battery-backed CMOS processors.			
IN an	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.			
NMI	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.			
ST	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.			
CEO	Chip enable output. Used with nonvolatile SRAM applications.			
CEI	Chip enable input.			
PBRST	Pushbutton reset input.			
RST	Active low reset output.			
RST	Active high reset output.			

#### PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V<sub>CC</sub>. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt (NMI) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V<sub>CCO</sub>.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of  $V_{CC}$ . This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until  $V_{CC}$  reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

#### POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V<sub>CC</sub>) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and RST outputs are driven to the active state. The V<sub>CC</sub> trip point (V<sub>CCTP</sub>) is set for 10% operation so that the RST and RST outputs will become active as V<sub>CC</sub> falls below 4.5 volts (4.37 typical). The V<sub>CCTP</sub> for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and RST signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V<sub>CC</sub>. On power-up, the RST and RST signals are held active for a minimum of 25 ms (100 ms typical) after V<sub>CCTP</sub> is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more infor-

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#### WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and RST signals to the active state when the strobe input (ST) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and RST are inactive. If a high-to-low transition occurs at the ST input prior to time-out, the watchdog timer is reset and begins to time out again. The ST input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on ST must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and RST outputs are driven to the active state for 25 ms minimum. The ST input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below  $V_{TP}$ . With IN grounded, an  $\overline{\text{NMI}}$  output will occur only at power-up, or when the  $\overline{\text{ST}}$  pin is strobed. As shown in the Figure 3, a falling edge on  $\overline{\text{ST}}$  will generate an  $\overline{\text{NMI}}$  when IN is below  $V_{TP}$ . This allows the processor to verify that power is between  $V_{TP}$  and  $V_{CCTP}$  as an  $\overline{\text{NMI}}$  will be returned immediately after the  $\overline{\text{ST}}$  strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the  $\overline{\text{NMI}}$  signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the  $\overline{\text{ST}}$  input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as  $V_{CC}$  falls to  $V_{CCTP}$ .

#### **PUSHBUTTON RESET**

An input pin is provided on the DS1236 for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V<sub>CC</sub> is greater than V<sub>BAT</sub>. The PBRST pin is also debounced and timed such that the RST and RST outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The PBRST input is disabled whenever the IN pin voltage

level is less than  $V_{TP}$  and the reset control (RC) is tied high (CMOS mode). The  $\overline{PBRST}$  input is also disabled whenever  $V_{CC}$  is below  $V_{BAT}$ . Timing of the  $\overline{PBRST}$ -generated RST is illustrated in Figure 5.

#### **NON-MASKABLE INTERRUPT**

The DS1236 generates a non-maskable interrupt NMI for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V<sub>TP</sub> is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to VIN. Therefore, the maximum allowable voltage at the supply being monitored (V<sub>MAX</sub>) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between NMI and RST or RST.

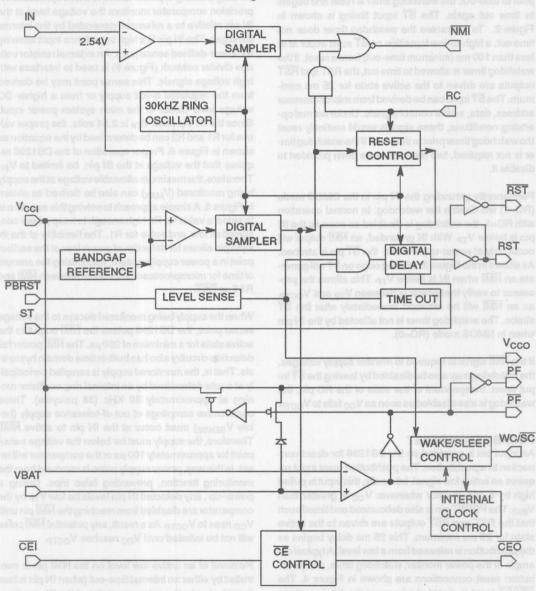
When the supply being monitored decays to the voltage sense point, the DS1236 pulses the NMI output to the active state for a minimum of 200 µs. The NMI power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V<sub>SENSE</sub>) must occur at the IN pin to active NMI. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up, any detected IN pin levels be low VTP by the comparator are disabled from reaching the NMI pin until V<sub>CC</sub> rises to V<sub>CCTP</sub>. As a result, any potential NMI pulse will not be initiated until V<sub>CC</sub> reaches V<sub>CCTP</sub>.

Removal of an active low level on the  $\overline{\text{NMI}}$  pin is controlled by either an internal time-out (when IN pin is less than  $V_{TP}$ ) or by the subsequent rise of the IN pin above

 $V_{TP}$ . The initiation and removal of the  $\overline{NMI}$  signal during power-up results in an  $\overline{NMI}$  pulse of from 0 μs minimum to 500 μs maximum, depending on the relative voltage relationship between  $V_{CC}$  and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 μs

minimum to 500  $\mu$ s maximum. In contrast, if the IN pin is tied to  $V_{CCO}$  during power-up,  $\overline{NMI}$  will not produce a pulse on power-up. Note that a fast slewing power supply may cause the  $\overline{NMI}$  to be virtually non-existent on power-up. This is of no consequence, however, since a RST will be active.

# **DS1236 FUNCTIONAL BLOCK DIAGRAM** Figure 1



If the IN pin is connected to  $V_{CCO}$ , the  $\overline{NMI}$  output will pulse low as  $V_{CC}$  decays to  $V_{CCTP}$  in the NMOS mode (RC=0). In the CMOS mode (RC= $V_{CCO}$ ) the power-down of  $V_{CC}$  out-of-tolerance at  $V_{CCTP}$  will not produce a pulse on the  $\overline{NMI}$  pin. Given that any  $\overline{NMI}$  pulse has been completed by the time  $V_{CC}$  decays to  $V_{CCTP}$ , the  $\overline{NMI}$  pin will remain high. The  $\overline{NMI}$  voltage will follow  $V_{CC}$  down until  $V_{CC}$  decays to  $V_{BAT}$ . Once  $V_{CC}$  decays to  $V_{BAT}$ , the  $\overline{NMI}$  pin will either remain at  $V_{OHL}$  or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

#### **MEMORY BACKUP**

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V<sub>CC</sub>) or from an external battery (V<sub>BAT</sub>), whichever is greater. This switched supply (VCCO) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output (CEO) to within 0.3 volts of VCC or to within 0.7 volts of VBAT. This write protection mechanism occurs as V<sub>CC</sub> falls below V<sub>CCTP</sub> as specified. If CEI is low at the time power fail detection occurs, CEO is held in its present state until CEI is returned high, or the period toE expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If CEO is in an inactive state at the time of V<sub>CC</sub> fail detection, CEO will be unconditionally disabled within t<sub>CF</sub> During nominal supply conditions CEO will follow CEI with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal opera-

tion will begin when  $V_{CC}$  is cycled and reapplied to a level above  $V_{BAT}\!.$ 

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3 volt clock to TP1.

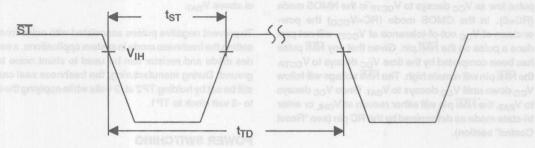
#### **POWER SWITCHING**

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V<sub>CCO</sub> with a reasonable voltage drop. For these applications, the PF and PF outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V<sub>CC</sub> to battery on power-down, and from battery to V<sub>CC</sub> on power- up. The DS1336 is designed to use the PF output to switch between VBAT and V<sub>CC</sub>. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and PF is set to the external battery voltage VBAT, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

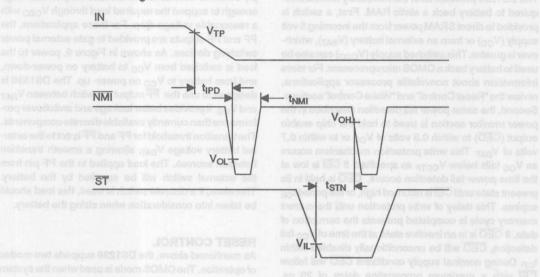
#### RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, RST, and NMI outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

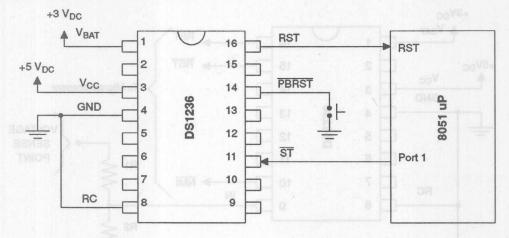
# ST/INPUT TIMING Figure 2



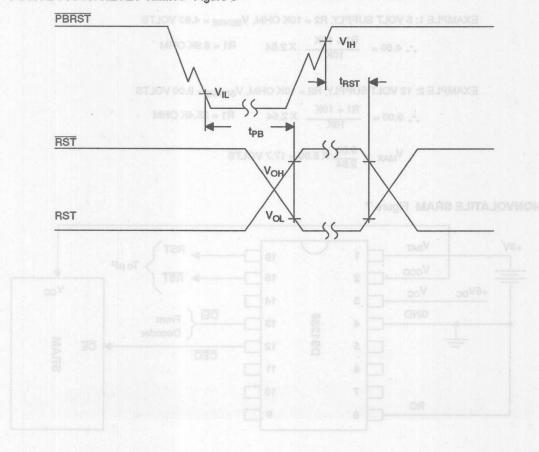
## NMI/FROM ST/INPUT Figure 3



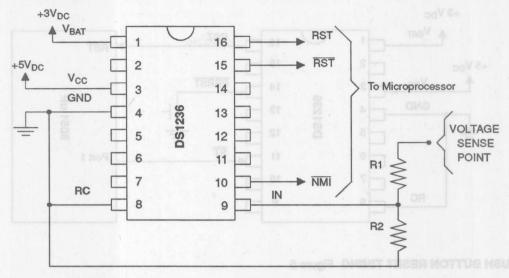
# **POWER MONITOR, WATCHDOG Figure 4**



# **PUSH BUTTON RESET TIMING** Figure 5



## NON-MASKABLE INTERRUPT Figure 6



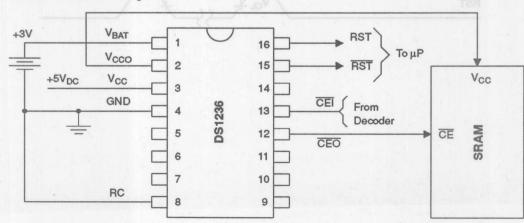
EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V<sub>SENSE</sub> = 4.80 VOLTS

$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54$$
 R1 = 8.9K OHM

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V<sub>SENSE</sub> = 9.00 VOLTS

•• 9.00 = 
$$\frac{R1 + 10K}{10K}$$
 X 2.54 R1 = 25.4K OHM  
 $V_{MAX} = \frac{9.00}{2.54}$  X 5.00 = 17.7 VOLTS

# NONVOLATILE SRAM Figure 7



10

When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the backup battery supply, or grounded when system V<sub>CC</sub> decays below V<sub>BAT</sub>. In the NMOS processor system, the principal emphasis is placed on giving early warnings with NMI, then providing a continuously active RST and RST signal during power-down while isolating the backup battery from the processor during a loss of V<sub>CC</sub>.

During power-down, NMI will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on NMI will follow V<sub>CC</sub> until V<sub>CC</sub> supply decays to V<sub>BAT</sub>, at which point NMI will enter tri-state (see timing diagram). Also, upon V<sub>CC</sub> out-of-tolerance at V<sub>CCTP</sub>, the RST and RST outputs are driven active and RST will follow V<sub>CC</sub> as the supply decays. On power-up, RST follows VCC up, RST is held low, and both remain active for t<sub>RST</sub> after valid V<sub>CC</sub>. During a power-up from a V<sub>CC</sub> voltage below V<sub>BAT</sub>, any detected IN pin levels below V<sub>TP</sub> are disabled from reaching the NMI pin until V<sub>CC</sub> rises to V<sub>CCTP</sub>. As a result, any potential NMI pulse will not be initiated until V<sub>CC</sub> reaches V<sub>CCTP</sub>. Removal of an active low level on the NMI pin is controlled by either an internal time-out (when the IN pin is less than V<sub>TP</sub>), or by the subsequent rise of the IN pin above V<sub>TP</sub>. The initiation and removal of the NMI signal results in an NMI pulse of 0 μs minimum to 500 μs maximum during power-up, depending on the relative voltage relationship between V<sub>CC</sub> and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V<sub>CCO</sub>, NMI will not produce a pulse on power-up.

Connecting the RC pin to a high (V<sub>CCO</sub>) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low-power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the con-

tents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no NMI and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed NMI for early power failure warning. Waiting to initiate a Stop mode until after the NMI pin has returned high will guarantee the processor that no other active NMI or RST/RST will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above VTP, which activates the watchdog, or 2) V<sub>CC</sub> cycles below then above V<sub>BAT</sub>, which also results in an active RST and RST. If Vcc. does not fall below V<sub>CCTP</sub>, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above VTP.

With the RC pin tied to V<sub>CCO</sub>, RST and RST are not forced active as V<sub>CC</sub> collapses to V<sub>CCTP</sub>. The RST is held at a high level via the external battery as V<sub>CC</sub> falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from NMI at an earlier voltage level. The NMI output pin will pulse low for t<sub>NMI</sub> following a low voltage detect at the IN pin of VTP. Following tNMI, however, NMI will also be held at a high level (VBAT) by the battery as VCC decays below VBAT. On power-up, RST and RST are held inactive until V<sub>CC</sub> reaches V<sub>RAT</sub>, then RST and RST are driven active for t<sub>RST</sub>. If the IN pin falls below V<sub>TP</sub> during an active reset, the reset outputs will be forced inactive by the NMI output. In addition, as long as the IN pin is less than V<sub>TP</sub>, stimulation of the ST pin will result in additional NMI pulses. In this way, the ST pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

#### **TIMING DIAGRAMS**

This section provides a description of the timing diagrams shown in Figure 10, Figure 11, Figure 12, and Figure 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for

power-down in CMOS mode. As  $V_{CC}$  falls, the IN pin voltage drops below  $V_{TP}$ . As a result, the processor is notified of an impending power failure via an active  $\overline{\text{NMI}}$ , which allows it to enter a sleep mode. As the power falls further,  $V_{CC}$  crosses  $V_{CCTP}$ , the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The  $\overline{\text{RST}}$  voltage will follow  $V_{CC}$  down, but will fall no further than  $V_{BAT}$ . At this time,  $\overline{\text{CEO}}$  is brought high to write protect the RAM. When the  $V_{CC}$  reaches  $V_{BAT}$ , a power fail is issued via the PF and  $\overline{\text{PF}}$  pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an  $\overline{\text{NMI}}$  is issued. This gives the processor time to save critical data in nonvolatile SRAM. When  $V_{CC}$  reaches  $V_{CCTP}$ , an active RST and  $\overline{\text{RST}}$  are given. The RST voltage will follow  $V_{CC}$  as it falls.  $\overline{\text{CEO}}$ , PF, and  $\overline{\text{PF}}$  will operate in a similar manner to CMOS mode. Notice that the  $\overline{\text{NMI}}$  will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the NMOS mode. As  $V_{CC}$  slews above  $V_{BAT}$ , the PF and  $\overline{PF}$  pins are deactivated. An active reset occurs as well as an  $\overline{NMI}$ . Although the  $\overline{NMI}$  may be short due to slew rates, reset will be maintained for the standard  $t_{RST}$  time-out period. At a later time, if the IN pin falls below  $V_{TP}$ , a new  $\overline{NMI}$  will occur. If the processor does not issue a  $\overline{ST}$ , a watchdog reset will also occur. The second  $\overline{NMI}$  and RST are provided to illustrate these possibilities.

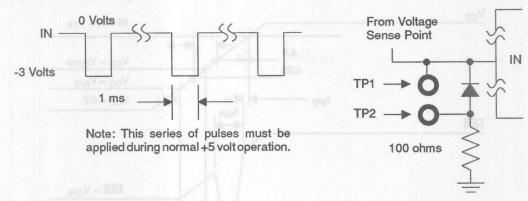
Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above  $V_{TP}$ . Depending on the processor type, the  $\overline{\text{NMI}}$  may terminate the Stop mode in the processor.

#### WAKE CONTROL/SLEEP CONTROL

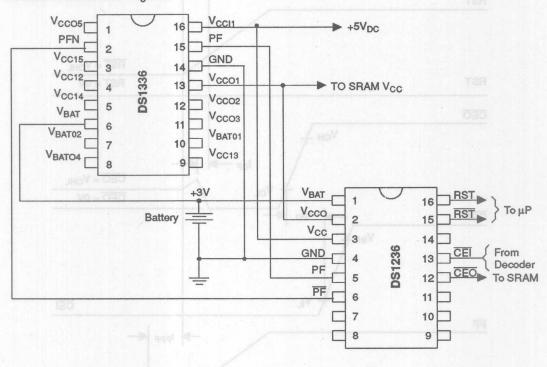
The Wake/Sleep Control input (WC/SC) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high-to-low transition on the PBRST input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and RST active. The DS1236 can also be started up by forcing the WC/SC pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V<sub>CC</sub> rises above V<sub>BAT</sub>. These possibilities are illustrated in Figure 15.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the NMI, RST, and RST outputs disabled as well as the ST and IN inputs. However, a loss of power during a sleep mode will result in an active RST and RST when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and RST pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the PBRST input is not affected by the IN pin threshold at VTP when the RC pin is tied high (CMOS mode). Subsequent power-up of the V<sub>CC</sub> supply with the RC pin tied high will activate the RST and RST outputs as the main supply rises above VBAT. A high-to-low transition on the WC/SC pin must follow a high-to-low transition on the ST pin by two to invoke a Sleep mode for the DS1236.

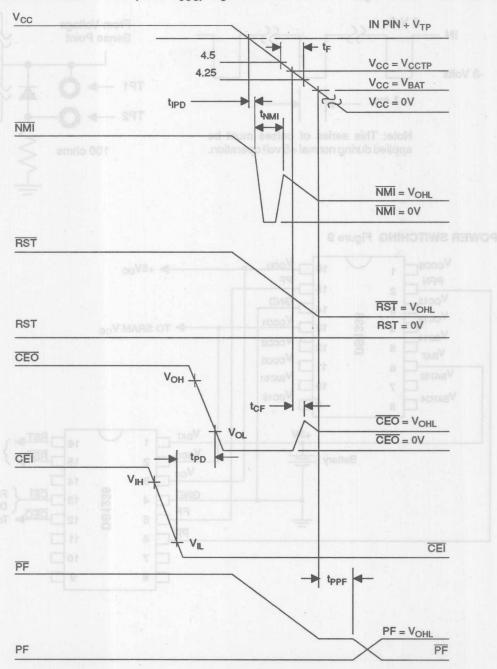
# FRESHNESS SEAL Figure 8



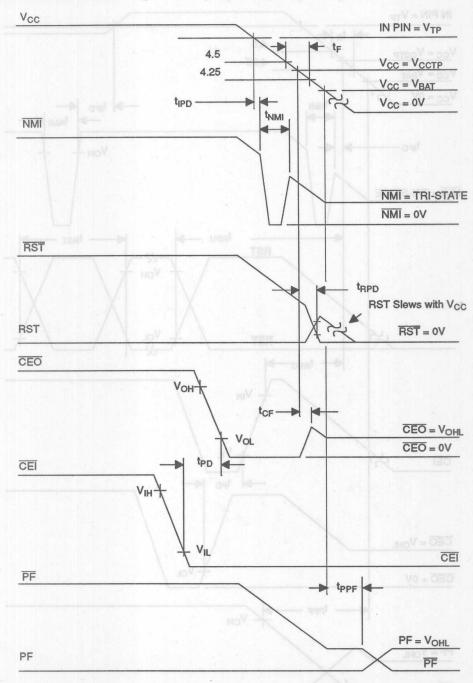
# **POWER SWITCHING** Figure 9



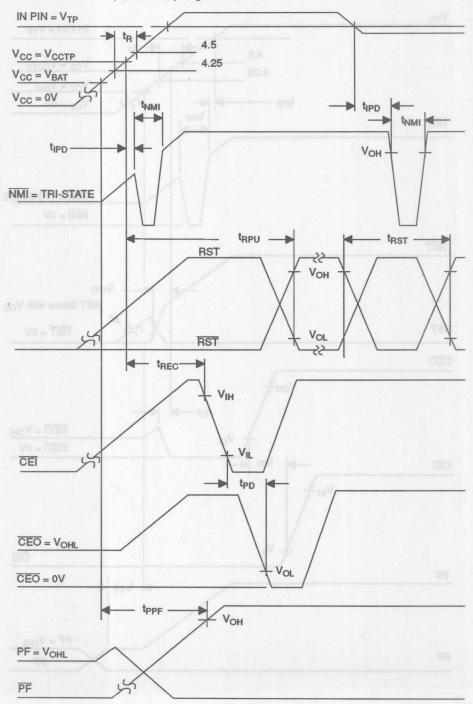
# CMOS MODE POWER-DOWN (RC = V<sub>CCO</sub>) Figure 10



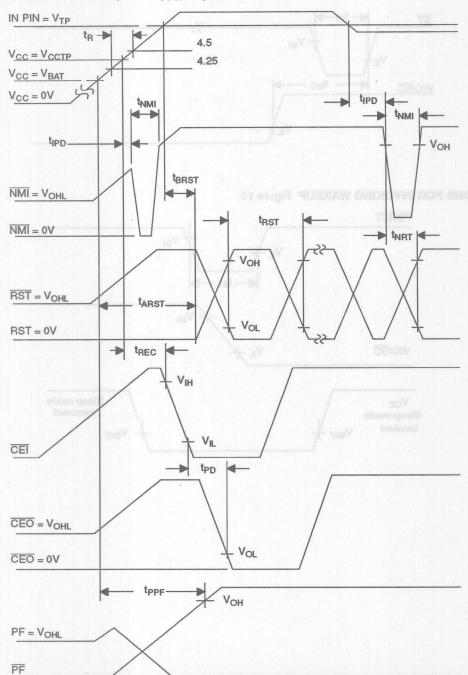
# NMOS MODE POWER-DOWN (RC = GND) Figure 11 1 (MAD = OR) 484-83WO4 300M 300M



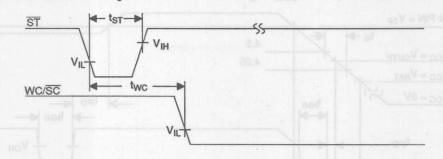
# NMOS MODE POWER-UP (RC = GND) Figure 12



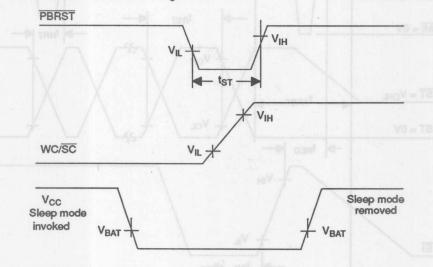
# CMOS MODE POWER-UP (RC = Vcco) Figure 13



## WAKE/SLEEP CONTROL Figure 14



# **OPTIONS FOR INVOKING WAKEUP** Figure 15



## **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature on the Leads -0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	тип 1 г
Supply Voltage (5% Option)	V <sub>CC</sub>	4.75	5.0	5.5	V	ESEPT Acti
Input High Level	VIH	2.0	tionel	V <sub>CC</sub> +0.3	Vittoli	/ salu¶ TV
Input Low Level	V <sub>IL</sub>	-0.3	ret	+0.8	V dib	W salts 7
IN Input Pin	VIN	-0.3	1919	V <sub>CC</sub> +0.3	V	O TERE
Battery Input	V <sub>BAT</sub>	2.7	all	4.0	of a Valeto	R wat or

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	lcc		Dille	4	mA	2
Sleep Supply Current in Sleep mode	Icc	a: ] [	Usel	20	μА	oo Valid to
Battery Current	I <sub>BAT</sub>		16/14	0.1	μА	2
Supply Output Current (V <sub>CCO</sub> =V <sub>CC</sub> - 0.3V)	I <sub>CC01</sub>		saw oan <sup>d</sup>	100	mA	3
Supply Output Current in Data Retention (V <sub>CC</sub> < V <sub>BAT</sub> )	I <sub>CC02</sub>		p)	1	mA	4 A well ac
Supply Output Voltage	Vcco		V <sub>CC</sub> -0.3	1 1	V V	idanii qirl
Battery Backup Voltage	Vcco	oor I	V <sub>BAT</sub> -0.7		ValoV emi	1,6
CEO and PF Output	V <sub>OHL</sub>	1.5	V <sub>BAT</sub> -0.7		V	1,6
PBRST Pull Up Resist	R <sub>PBRST</sub>	10K	व्यवर्ग		Ohms	BAT Debe
Input Leakage Current	ILI	-1.0	unet	+1.0	μА	18
Output Leakage	lLO	-1.0	raud	+1.0	μА	18
Output Current @0.4V	loL		tena)	4.0	mA	12
Output Current @2.4V	ГОН	-1.0	renef		mA	13
Power Sup. Trip Point	V <sub>CCTP</sub>	4.25	4.37	4.50	V	1

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Trip (5% Option)	V <sub>CCTP</sub>	4.50	4.62	4.75	sperVure .	erating Tea
IN Input Pin Current	ICCIN	-1.0		+1.0	μА	19) Burier
IN Input Trip Point	V <sub>TP</sub>	2.5	2.54	2.6	V	te s al sid

## AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> Fail Detect to RST, RST	t <sub>RPD</sub>	40	100	175	μS	PAR
V <sub>TP</sub> to NMI	t <sub>IPD</sub>	40	100	175	μS	nation Alddin
RESET Active Time	t <sub>RST</sub>	25	100	150	mS	upply Volta
NMI Pulse Width	t <sub>NMI</sub>	200	300	500	μS	14
ST Pulse Width	t <sub>ST</sub>	20	дV		nS	put Low Le
PBRST @ V <sub>IL</sub>	t <sub>PB</sub>	30	. wV		mS	nist augni i
V <sub>CC</sub> Slew Rate 4.75 to 4.25	t <sub>F</sub>	300	VBAT		μS	attery Input
Chip Enable Propagation Delay	t <sub>PD</sub>		SAITE	20	nS	W 200 10 -
V <sub>CC</sub> Fail to Chip Enable High	tcF	7	12	44	μS	17
V <sub>CC</sub> Valid to RST, RST (RC=1)	t <sub>FPU</sub>		lco	100	nS	υρρλу Ουπι
V <sub>CC</sub> Valid to RST & RST	t <sub>RPU</sub>	25	100	150	mS	5
V <sub>CC</sub> Slew to 4.24 to V <sub>BAT</sub>	t <sub>FB1</sub>	10	tund.		μS	7
V <sub>CC</sub> Slew 4.25 to 4.75 V <sub>BAT</sub>	t <sub>FB2</sub>	100	- Innered		μS	8
Chip Enable Output Recovery Time	t <sub>REC</sub>	.1			μS	9 9
V <sub>CC</sub> Slew 4.25 to 4.75	t <sub>R</sub>	0		(12	μS	dnoteR sta
Chip Enable Pulse Width	t <sub>CE</sub>		Voco	5	S	10
Watchdog Time Delay	t <sub>TD</sub>	100	400	600	mS	diely Back
ST to WC/SC	twc	0.1	жо∀	50	μS	EG and Pi
V <sub>BAT</sub> Detect to PF, PF	tppF	KI	Првазт	2	μS	7
ST to NMI	t <sub>STN</sub>	U.	13	30	nS	11
NMI to RST & RST	t <sub>NRT</sub>	4-1	- aul	30	nS 👓	riand to give
V <sub>BAT</sub> Detect to RST & RST	tARST		Jol	200	μS	15
V <sub>CC</sub> Valid to RST, RST	t <sub>BRST</sub>	30	100	150	μS	16

CAPACITANCE  $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	MODEM:
Output Capacitance	C <sub>OUT</sub>			7	pF	

#### NOTES:

- 1. All voltages referenced to ground. A 0.1 μF capacitor is recommended between V<sub>CC</sub> and GND.
- 2. Measured with V<sub>CCO</sub>, CEO, PF, ST, PBRST, RST, RST, and NMI pin open. I<sub>BAT</sub> specified at 25°C.
- 3. I<sub>CCO1</sub> is the maximum average load which the DS1236 can supply at V<sub>CC</sub>-0.3V through the V<sub>CCO</sub> pin during normal 5-volt operation.
- I<sub>CCO2</sub> is the maximum average load which the DS1236 can supply through the V<sub>CCO</sub> pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
- 5. With  $t_B = 5 \mu s$ .
- 6. V<sub>CCO</sub> is approximately V<sub>BAT</sub>-0.5V at 1 μA load.
- 7. Sleep mode is not invoked.
- 8. Sleep mode is invoked.
- 9. t<sub>REC</sub> is the minimum time required before CEI/CEO memory access is allowed.
- 10. t<sub>CF</sub> maximum must be met to ensure data integrity on power loss.
- 11. IN input is less than V<sub>TP</sub> but V<sub>CC</sub> greater than V<sub>CCTP</sub>.
- 12. All outputs except RST which is 25 µA maximum.
- 13. All outputs except RST which is 25 µA minimum.
- 14. Pulse width of NMI requires that the IN pin remain below V<sub>TP</sub>. If the IN pin returns to a level above V<sub>TP</sub> for a period longer than t<sub>IPD</sub> and before the t<sub>NMI</sub> period has elapsed, the NMI pin will immediately return to a high.
- 15. IN pin greater than V<sub>TP</sub> when V<sub>CC</sub> supply rises to V<sub>BAT</sub>. Example: IN tied to GND.
- 16. IN pin less than V<sub>TP</sub> when V<sub>CC</sub> supply rises to V<sub>BAT</sub>.
- 17. CEI low.
- 18. The WC/SC pin contains an internal latch which drives back on to the pin. This latch requires ±200 μamps to switch states. The ST pin will sink ±50 uamps in normal operation and ±1 μamp in the sleep mode.



# DS1238 MicroManager

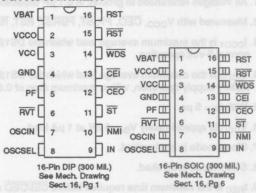
#### **FEATURES**

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- · Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- · Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238-5
- Provides orderly shutdown in microprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

#### DESCRIPTION

The DS1238 MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238 also provides early warning detection of a user-defined threshold by driving a non-maskable inter-

#### **PIN ASSIGNMENT**



#### PIN DESCRIPTION

V <sub>BAT</sub>	+3 Volt Battery input	
Vcco	Switched SRAM Supply Output	
Vcc	+5 Volt power supply input	
GND	Ground	
PF	Power Fail	
RVT	Reset Voltage Threshold	
OSCIN	Oscillator In	
OSCSEL	Oscillator Select	
IN	Early Warning input	
NMI	Non Maskable Interrupt	
ST	Strobe input	
CEO	Chip Enable output	
CEI	Chip Enable input	
WDS	Watchdog status	
RST	Reset output (active low)	
RST	Reset output (active high)	

rupt. External reset control is provided by a pushbutton reset debounce circuit connected to the  $\overline{RST}$  pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via  $\overline{WDS}$  and  $\overline{RVT}$ , respectively. A block diagram of the DS1238 is shown in Figure 1.

# 10

#### PIN DESCRIPTION

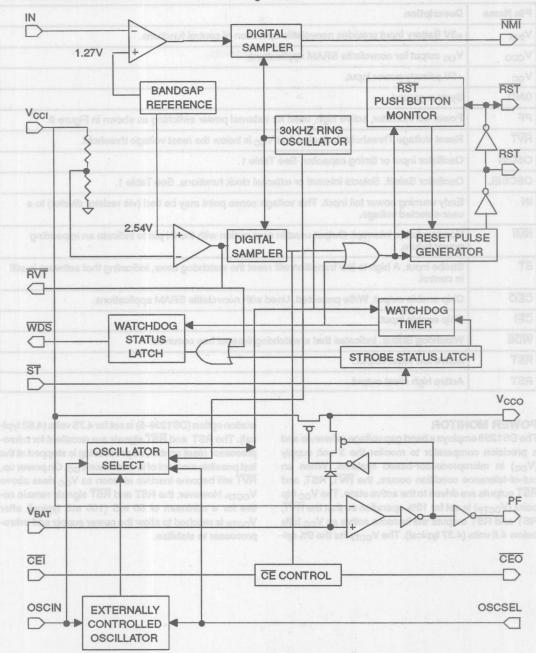
Pin Name	Description
V <sub>BAT</sub>	+3V Battery Input provides nonvolatile operation of control functions.
Vcco	V <sub>CC</sub> output for nonvolatile SRAM applications.
Vcc	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
RVT	Reset Voltage Threshold. Indicates that V <sub>CC</sub> is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN A	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
NMI	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
ST	Strobe input. A high to low transition will reset the watchdog timer, indicating that software is still in control.
CEO	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
CEI	Chip enable input.
WDS	Watchdog Status. Indicates that a watchdog timeout has occurred.
RST	Active low reset output.
RST	Active high reset output.

#### **POWER MONITOR**

The DS1238 employs a band gap voltage reference and a precision comparator to monitor the 5 volt supply (V<sub>CC</sub>) in microprocessor-based systems. When an out-of-tolerance condition occurs, the  $\overline{\text{RVT}}$ , RST, and  $\overline{\text{RST}}$  outputs are driven to the active state. The V<sub>CC</sub> trip point (V<sub>CCTP</sub>) is set for 10% operation so that the  $\overline{\text{RVT}}$ , RST and  $\overline{\text{RST}}$  outputs will become active as V<sub>CC</sub> falls below 4.5 volts (4.37 typical). The V<sub>CCTP</sub> for the 5% op-

eration option (DS1238-5) is set for 4.75 volts (4.62 typical). The RST and  $\overline{RST}$  signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance  $V_{CC}$ . On power up,  $\overline{RVT}$  will become inactive as soon as  $V_{CC}$  rises above  $V_{CCTP}$ . However, the RST and  $\overline{RST}$  signals remain active for a minimum of 50 mS (100 mS typical) after  $V_{CCTP}$  is reached to allow the power supply and microprocessor to stabilize.

## **DS1238 FUNCTIONAL BLOCK DIAGRAM** Figure 1



# 10

#### WATCHDOG TIMER

The DS1238 provides a watchdog timer function which forces the WDS, RST, and RST signals to the active state when the strobe input (ST) is not stimulated for a predetermined time period. This time period is described below in Table 1. The Watchdog timeout period begins as soon as RST and RST are inactive. If a high-to-low transition occurs at the ST input prior to timeout, the watchdog timer is reset and begins to time out again. The ST input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on ST must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the WDS, RST, and RST outputs are driven to the active state. WDS is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The WDS pin will remain low until one of three operations occurs. The first is to strobe the ST pin with a falling edge, which will both set the WDS as well as the watchdog timer count. The second is to leave the ST pin open, which disables the Watchdog, Lastly the WDS pin is set whenever Vcc falls below V<sub>CCTP</sub> and activates the RVT signal. The ST input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the Watchdog timer prior to time out. The Watchdog is disabled by leaving the ST input open, or as soon as V<sub>CC</sub> falls to V<sub>CCTP</sub>.

#### NON-MASKABLE INTERRUPT

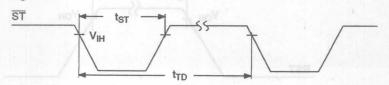
The DS1238 generates a non-maskable interrupt (NMI) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power

input. Since the IN trip point  $V_{TP}$  is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238 requires that the voltage at the IN pin be limited to  $V_{IH}$ . Therefore, the maximum allowable voltage at the supply being monitored ( $V_{MAX}$ ) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between  $\overline{NMI}$  and RST or  $\overline{RST}$ .

When the supply being monitored decays to the voltage sense point, the DS1238 will force the NMI output to an active state. Noise is removed from the NMI power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V<sub>SENSE</sub>) must occur at the IN pin to active NMI. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power up, any IN pin levels below V<sub>TP</sub> detected by the comparator are disabled from reaching the NMI pin until V<sub>CC</sub> rises to V<sub>CCTP</sub>. As a result, any potential active NMI will not be initiated until V<sub>CC</sub> reaches V<sub>CCTP</sub>.

Removal of an active low level on the  $\overline{\text{NMI}}$  pin is controlled by the subsequent rise of the IN pin above V<sub>TP</sub>. The initiation and removal of the  $\overline{\text{NMI}}$  signal during power up depends on the relative voltage relationship between V<sub>CC</sub> and the IN pin voltage. Note that a fast slewing power supply may cause the  $\overline{\text{NMI}}$  to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The  $\overline{\text{NMI}}$  voltage will follow V<sub>CC</sub> down until V<sub>CC</sub> decays to V<sub>BAT</sub>. Once V<sub>CC</sub> decays to V $\overline{\text{BAT}}$ , the  $\overline{\text{NMI}}$  pin will enter a tri-state mode.

**ST INPUT TIMING** Figure 2

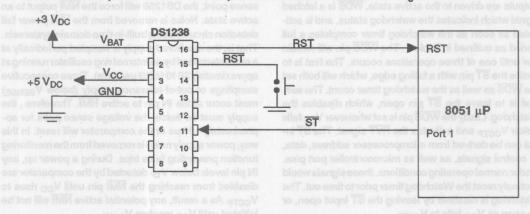


### **OSCILLATOR CONTROLS** Table 1

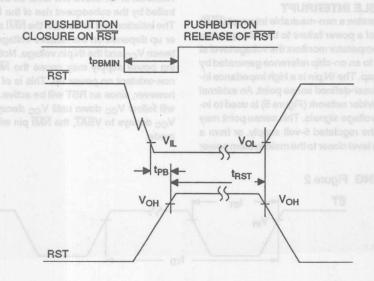
lsupe erit yd be	n metabled nsa	lor R1 and R2	Watchdog Time	out Period (typ)	e DS 1238 provides
	OSCIN	OSCSEL	First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	≅ 550 ms X Cpf	$\cong \frac{2.2 \text{ sec}}{47 \text{ pf}} \text{ X Cpf}$	$\cong \frac{69 \text{ ms}}{47 \text{ pf}} \text{ X Cpf}$
Internal	Low	Hi/Open	2.7 sec	170 mS	85 mS
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 mS

Note that the OSCIN and OSCSEL pins are tri-stated when V<sub>CC</sub> is below V<sub>BAT</sub>.

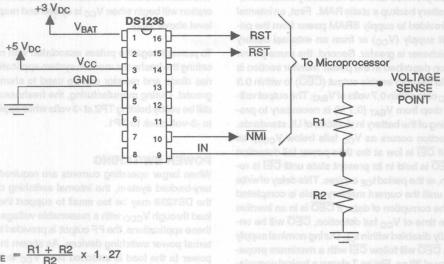
## POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



## **PUSHBUTTON RESET TIMING** Figure 4



# NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

MAXVOLTAGE =  $\frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$ 

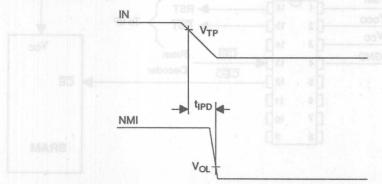
Example 1: 5 Volt Supply, R2 = 10K Ohms,  $V_{SENSE} = 4.8 \text{ Volts}$   $4.8 = \frac{R1 + 10K}{10K} \times 1.27 \ge R1$ = 27.8K Ohm

Example 2: 12 Volt Supply, R2 = 10K Ohms, 
$$V_{SENSE} = 9.0 \text{ Volts}$$

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \ge R1 = 60.9K$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$





#### **MEMORY BACKUP**

The DS1238 provides all of the necessary functions required to battery backup a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V<sub>CC</sub>) or from an external battery (VBAT), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output (CEO) to within 0.3 volts of V<sub>CC</sub> or to within 0.7 volts of V<sub>BAT</sub>. The output voltage diode drop from VBAT (0.7 V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V<sub>CC</sub> falls below V<sub>CCTP</sub> as specified. If CEI is low at the time power fail detection occurs, CEO is held in its present state until CEI is returned high, or the period top expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If CEO is in an inactive state at the time of V<sub>CC</sub> fail detection, CEO will be unconditionally disabled within top. During nominal supply conditions CEO will follow CEI with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1238 provides an internal freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will result in the tri-state of outputs  $V_{CCO}$ , RST,  $\overline{RST}$ , and  $\overline{CEO}$ . The PF pin is not disabled by the freshness mode and will continue to source

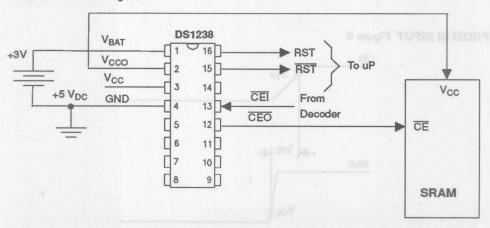
power from the  $V_{BAT}$  pin whenever  $V_{CC}$  is below  $V_{BAT}$ . The freshness seal will be disconnected and normal operation will begin when  $V_{CC}$  is cycled and reapplied to a level above  $V_{BAT}$ .

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3-volt clock to TP1.

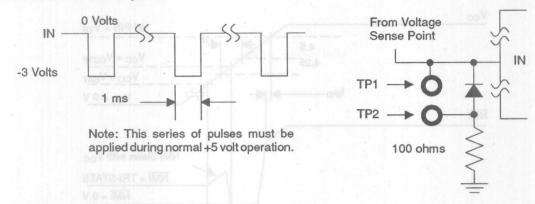
#### **POWER SWITCHING**

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238 may be too small to support the required load through V<sub>CCO</sub> with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V<sub>CC</sub> to battery on power down, and from battery to V<sub>CC</sub> on power up. The DS1336 is designed to use the PF output to switch between VBAT and VCC. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V<sub>BAT</sub>, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

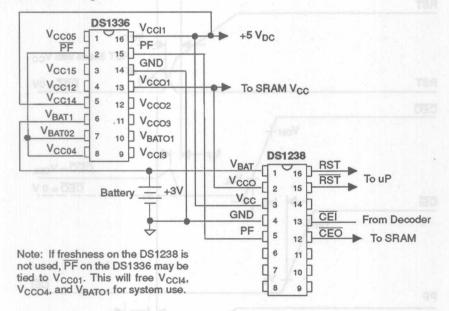
## **NONVOLATILE SRAM** Figure 7



## FRESHNESS SEAL Figure 8



## **POWER SWITCHING** Figure 9



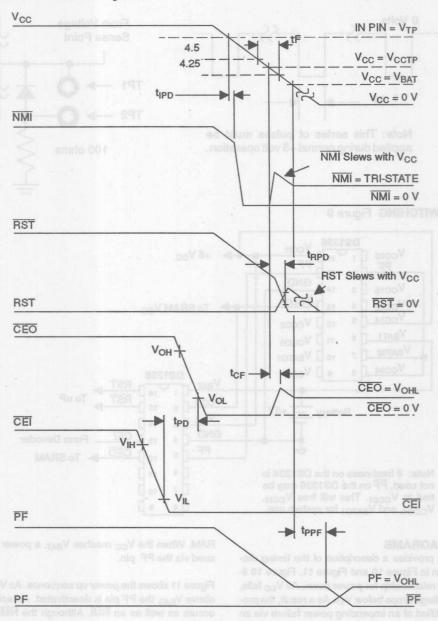
## TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 10 and Figure 11. Figure 10 illustrates the relationship for power down. As  $V_{\rm CC}$  falls, the IN pin voltage drops below  $V_{\rm TP}$ . As a result, the processor is notified of an impending power failure via an active  $\overline{\rm NMI}$ . This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further,  $V_{\rm CC}$  crosses  $V_{\rm CCTP}$ , the power monitor trip point. When  $V_{\rm CC}$  reaches  $V_{\rm CCTP}$ , and active RST and  $\overline{\rm RST}$  are given. At this time,  $\overline{\rm CEO}$  is brought high to write protect the

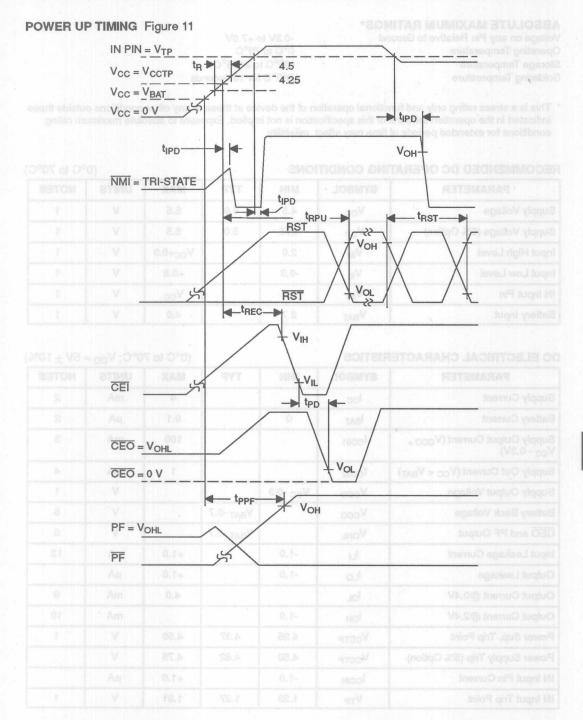
RAM. When the  $V_{CC}$  reaches  $V_{BAT}$ , a power fail is issued via the PF pin.

Figure 11 shows the power up sequence. As  $V_{CC}$  slews above  $V_{BAT}$ , the PF pin is deactivated. An active reset occurs as well as an  $\overline{\text{NMI}}$ . Although the  $\overline{\text{NMI}}$  may be short due to slew rates, reset will be maintained for the standard  $t_{RPU}$  timeout period . At a later time, if the IN pin falls below  $V_{TP}$ , a new  $\overline{\text{NMI}}$  will occur. If the processor does not issue an  $\overline{\text{ST}}$ , a watchdog reset will also occur. The second  $\overline{\text{NMI}}$  and RST are provided to illustrate these possibilities.

## **POWER DOWN TIMING** Figure 10







## **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 seconds

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	Vcc	4.75	5.0	5.5	٧	1
Input High Level	V <sub>IH</sub>	2.0	N	V <sub>CC</sub> +0.3	٧	1
Input Low Level	V <sub>IL</sub>	-0.3	X	+0.8	٧	1
IN Input Pin	VIN	0		Vcc	٧	1
Battery Input	V <sub>BAT</sub>	2.7	图19一岁	4.0	٧	1

## DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{DD} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc	10 4-		4	mA	2
Battery Current	I <sub>BAT</sub>	0		0.1	μА	2
Supply Output Current (V <sub>CCO</sub> = V <sub>CC</sub> - 0.3V)	I <sub>CC01</sub>			100	mA	3
Supply Out Current (V <sub>CC</sub> < V <sub>BAT</sub> )	I <sub>CC02</sub>			1 V	mA	4
Supply Output Voltage	V <sub>cco</sub>	V <sub>CC</sub> -0.3	month and		V	1
Battery Back Voltage	V <sub>cco</sub>	NOV TY	V <sub>BAT</sub> -0.7		V	6
CEO and PF Output	V <sub>OHL</sub>		V <sub>BAT</sub> -0.7	JPK	V	6
Input Leakage Current	I <sub>LI</sub>	-1.0	180	+1.0	μА	12
Output Leakage	ILO	-1.0		+1.0	μА	
Output Current @0.4V	l <sub>OL</sub>			4.0	mA	9
Output Current @2.4V	Іон	-1.0			mA	10
Power Sup. Trip Point	V <sub>CCTP</sub>	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V <sub>CCTP</sub>	4.50	4.62	4.75	V	
IN Input Pin Current	ICCIN	-1.0		+1.0	μА	
IN Input Trip Point	V <sub>TP</sub>	1.23	1.27	1.31	V	1

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# AC ELECTRICAL CHARACTERISTIC

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> Fall Detect to RST, RST	t <sub>RPD</sub>	40	100	175	μS	bewseek
V <sub>TP</sub> to NMI	t <sub>IPD</sub>	40	100	175	μS	ccos is life
RESET Active OSCSEL=high	t <sub>RST</sub>	50	85	150	mS	tt al energy
ST Pulse Width	t <sub>ST</sub>	20	primum drog	n, with a m	nS	sattery sup
PBRST @ V <sub>IL</sub>	t <sub>PB</sub>	30			mS	e pl (til)
V <sub>CC</sub> Slew Rate 4.75 to 4.25	t <sub>F</sub>	300	baol Au Ta	Va.O-TAB	μS	15 El 000 \
Chip Enable Prop Delay	t <sub>PD</sub>	nomem OS	Also aroleo	20	nS	eris al pan
V <sub>CC</sub> Fail to Chip Enable High	t <sub>CF</sub>	7	12	144	μS	11
V <sub>CC</sub> Valid to RST (RC = 1)	t <sub>FPU</sub>		以高四 利其	100	nS	EUGIZIO SA
V <sub>CC</sub> Valid to RST	t <sub>RPU</sub>	50	100	150	mS	5
V <sub>CC</sub> Slew to 4.25 to V <sub>BAT</sub>	t <sub>FB1</sub>	10	mes operation	in ni Au Ot	μS	THEOSC TIS SI
Chip Enable Output Recovery Time	t <sub>REC</sub>	.1			μS	7
V <sub>CC</sub> Slew 4.25 to 4.75	t <sub>R</sub>	0			μS	
Chip Enable Pulse Width	t <sub>CE</sub>			5	μS	8
Watchdog Time Delay int clock Long period	t <sub>TD</sub>		2.7		S	
Short period			170		mS	
Watchdog Time Delay, ext clock, After reset	t <sub>TD</sub>		20480		clocks	
Normal			5120		clocks	
V <sub>BAT</sub> Detect to PF	t <sub>PPF</sub>			2	μS	
OSC IN Frequency	fosc	0		250	KHz	

CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

## NOTES:

- 1. All voltages referenced to ground.
- 2. Measured with V<sub>CCO</sub>, CEO, PF, ST, RST, RST, and NMI pin open.
- I<sub>CCO1</sub> is the maximum average load which the DS1238 can supply at V<sub>CC</sub>-.3V through the V<sub>CCO</sub> pin during normal 5-volt operation.
- I<sub>CCO2</sub> is the maximum average load which the DS1238 can supply through the V<sub>CCO</sub> pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
- 5. With  $t_R = 5 \mu s$ .
- 6. V<sub>CCO</sub> is approximately V<sub>RAT</sub> 0.5V at 1 μA load.
- 7. t<sub>REC</sub> is the minimum time required before CEI/CEO memory access is allowed.
- 8. t<sub>CF</sub> maximum must be met to insure data integrity on power loss.
- 9. All outputs except RST which is 50 µA max.
- 10. All outputs except RST which is 50 μA min.
- 11. The  $\overline{ST}$  pin will sink  $\pm$  50  $\mu$ A in normal operation. The OSCIN pin will sink  $\pm$  5  $\mu$ A in normal operation. The OSCSEL pin will sink  $\pm$  10  $\mu$ A in normal operation.



# **DALLAS**SEMICONDUCTOR

# DS1239 MicroManager Chip

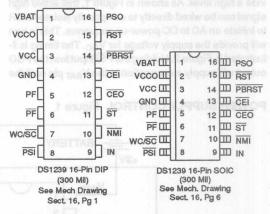
#### **FEATURES**

- Provides necessary control for start up and shutdown of power supply from keyboard
- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1239-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operate hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

#### **DESCRIPTION**

The DS1239 MicroManager provides all the necessary functions for power supply control and monitoring, reset control, and memory backup in microprocessor-based systems. Using the DS1239, an AC power switch is no longer required for microprocessor-based systems. A keyboard control system for power supply start up and shutdown is provided through the use of the Power Supply Control Input and Output. In other respects, the DS1239 is functionally identical to a DS1236 in the

## **PIN ASSIGNMENT**



#### PIN DESCRIPTION

VBAT	+3 Volt Battery Input
Vcco	Switched SRAM Supply Output
Vcc	+5 Volt Power Supply Input
GND	Ground
PF	Power Fail (Active High)
PF	Power Fail (Active Low)
WC/SC	Wake-Up Control (Sleep)
PSI	Power Supply Control Input
IN	Early Warning Input
NMI	Non-Maskable Interrupt
ST	Strobe Input
CEO	Chip Enable Output
CEI	Chip Enable Input
PBRST	Push Button Reset Input
RST	Reset Output (Active low)
PSO	Power Supply Control Outputs

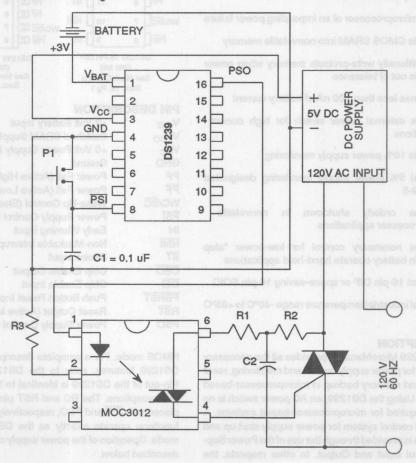
NMOS mode. For a complete description of the other DS1239 features, refer to the DS1236 data sheet. Pin-out of the DS1239 is identical to the DS1236 with two exceptions. The RC and RST pins have been replaced with  $\overline{PSI}$  and PSO, respectively. Other pins and functions operate exactly as the DS1236 in NMOS mode. Operation of the power supply control function is described below.

#### POWER SUPPLY CONTROL

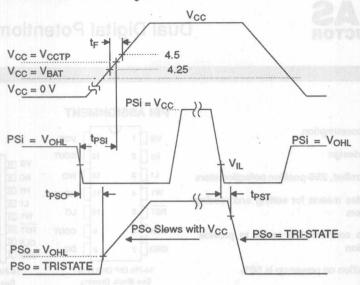
The DS1239 facilitates the power-up and power down sequencing of a main power supply from a keyboard or pushbutton. The Power Supply Control Input (PSI) and Power Supply Control Output (PSO) are used for this purpose. Prior to establishing a voltage on V<sub>CC</sub> (+5V), the PSI is internally held at a high level at all times with the V<sub>BAT</sub> supply. When PSI is forced low via a key pad or other source, the PSO is connected to the V<sub>BAT</sub> to provide a high level. As shown in Figure 1, this active high signal can be wired directly to an optically isolated SCR to initiate an AC to DC power-up sequence. This in turn will provide the supply voltage for V<sub>CC</sub>. The timing is illustrated in Figure 2. Holding the PSI input low, the PSO output will supply a connection to the V<sub>BAT</sub> pin until the

 $V_{CC}$  reaches  $V_{BAT}$ , or a maximum of 200 mS. If the supply voltage on  $V_{CC}$  rises above the  $V_{BAT}$  level before the  $t_{PSI}$  time-out, the PSO pin will remain high and track the  $V_{CC}$  input. If  $V_{CC}$  does not rise above  $V_{BAT}$  before either  $t_{PSI}$  or  $\overline{PSI}$  is allowed to return to a high level, the PSO output will return to tristate. Once the PSO output and  $V_{CC}$  are set at a high level, a subsequent falling edge on  $\overline{PSI}$  will tristate PSO to initiate a shut down condition. The 10 microamp current supplied by the  $\overline{PSI}$  pin allows the use of a 0.1  $\mu F$  capacitor as a simple pushbutton debounce circuit. The battery size for this application must be selected to provide the SCR on-current for the power supply response time and is consequently application-specific.

# **POWER SUPPLY CONTROL** Figure 1



# **POWER SUPPLY CONTROL TIMING** Figure 2



#### NOTES:

1. Minimum turn-on response time for AC-to-DC power supply.

2. PSO pulse width for V<sub>CC</sub> held below V<sub>BAT</sub>.

3. PSO will typically source 1.5 mA at 1.5V with  $V_{CC} = 0V$ ,  $V_{BAT} = 3V$ .

## **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature on the Leads -0.3V to +7.0V 0°C to 70°C -55°C to +125°C 260°C for 10 sec.

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

These specifications reflect the power supply control feature of the DS1239. For complete electrical specifications, refer to the DS1236 data sheet.

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>CC</sub> = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PSI Output Current	I <sub>PSI</sub>	i lo abri	3	bibbes byli	μА	a. Betwee
PSO Output Current	I <sub>PSO</sub>	10	and ordinate	and the sec	mA	3

#### AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C,  $V_{CC} = 4.5V$  to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PSI to Valid V <sub>CC</sub>	tpsi			200	ms	1
PSI to PSO Tri-state	t <sub>PST</sub>	a testi	four bats	20	ns	it ,neillibb
PSI to Valid PSO	t <sub>PSO</sub>	on Eve	NV alluse	100	ns	idnideq et
PSO Pulse Width	t <sub>PSP</sub>	1000000	200	500	ms	2



# Dual Digital Potentiometer Chip

## **FEATURES**

- Ultra-low power consumption
- Quiet, pumpless design
- Two digitally controlled, 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power-up is 50%
- Resistive elements are temperature-compensated to ± 0.3 LSB relative linearity
- Operating temperature range of 0° C to 70° C
- 16-Pin SOIC for surface-mount applications
- Resistance values:

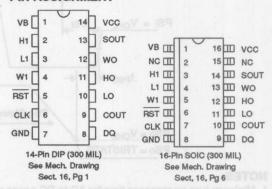
Device	Resolution	<u>-3dB</u>
DS1267-10: 10K	39 ohms	*1 MHz
DS1267-50: 50K	195 ohms	*200KHz
DS1267-100: 100	K 390 ohms	*100KHz
* into voltage follow	wer	

#### DESCRIPTION

The DS1267 is a dual solid-state potentiometer that is set to value by digitally selected resistive elements. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistance array is set by an 8-bit register that controls which tap point is connected to the wiper output. Each 8-bit register can be read or written by sending or receiving data bits over a three-wire serial port.

In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the

### **PIN ASSIGNMENT**



## PIN DESCRIPTION

LIM DESC	MIPHON
L0, L1	Low end of resistor
H0, H1	High end of resistor
W1, W2	Wiper end of resistor
VB	Substrate bias
SOUT	Wiper for stacked configuration
RST	Serial port reset input
DQ	Serial port data input
CLK	Serial port clock input
COUT	Cascade serial port output
Vcc	+5 volt input
GND	Ground
NC	No connection

DS1267 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same.

#### **OPERATION**

The DS1267 contains two potentiometers, each of which has its wiper set by a value contained in an 8-bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end. An 8-bit wiper register controls a 256-to-1 multiplexer that selects which tap point is connected to the wiper output.

10

In addition, the potentiometers can be stacked by connecting them in series such that the high end of Potentiometer 0 is connected to the low end of Potentiometer 1. When stacking potentiometers, the Stack Select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (S<sub>OUT</sub>). A 0 written to the stack multiplexer will connect Wiper 0 to the S<sub>OUT</sub> pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, Wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is present at the S<sub>OUT</sub> pin.

Information is written and read from the Wiper 0 and Wiper 1 register and the Stack Select bit via the 17-bit I/O Shift register. The I/O Shift register is always serially loaded by a 3-wire serial port consisting of RST, DQ, and clock. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17-bit shift register only when the RST input is at a high level. While at a high level, the RST function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until RST is taken to low a level, which terminates data transfer. While RST input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O Shift register while RST is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the Stack Select bit. The 17th bit to be entered, therefore, will be the least significant of the Wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, not sending 17 bits may produce indeterminate potentiometer settings.

As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (C<sub>OUT</sub>). By connecting the C<sub>OUT</sub> pin to the DQ pin of a second DS1267, multiple devices can be daisy-chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1267s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the C<sub>OUT</sub> pin of the last device connected in a daisy chain (one or more) must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between C<sub>OUT</sub> and DQ when writing to the device (see Figure 3).

When reading data, the DQ line is left floating by the reading device. When  $\overline{RST}$  is driven high, bit 17 is present on the  $C_{OUT}$  pin, which is fed back to the input DQ pin through the resistor. This data bit can now be read by the reading device. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on  $C_{OUT}$  and DQ. After 17 bits (17X devices for daisy chain), the data has shifted completely around and back to its original position. When  $\overline{RST}$  is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the Wiper 0 and Wiper 1 register and the Stack Select bit is loaded from the I/O shift register.

When power is applied to the DS1267, the device always has the wiper settings at half position and the Stack Select bit is at zero.

## **DS1267 LINEARITY MEASUREMENTS**

An important specification for the DS1267 is linearity; that is, for a given digital input, how close is the analog output relative to that which is expected.

The test circuit used to measure the linearity of the DS1267 is shown in Figure 5. The part is set up in a worst case situation for linearity, which is the stacked configuration. This gives 512 possible settings for the composite potentiometer. Note that to get an accurate output voltage, it is necessary to assure that the output current is 0 in order to negate the effects of wiper impedances RW1 and RW0, which are typically 400 ohms. For any given setting N for the pot, the expected voltage out put at S<sub>OUT</sub> is:

$$V_0 = -5 + (10 \times [N/512])$$
 [in volts]

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/512 or 0.01953 volts. The equation for the absolute linearity of the DS1267 is:

$$\frac{V_O \text{ (actual)} - V_O \text{ (expected)}}{LSB} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1267 is  $\pm$  0.75 LSB typical.

Figure 6 is a plot of absolute linearity AL and relative linearity (rel) versus wiper setting for a typical DS1267 at 25°C.

## **ANALOG CHARACTERISTICS**

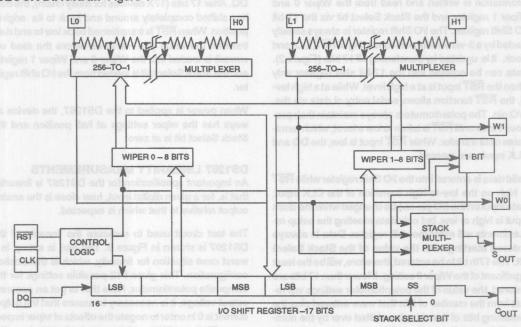
End-to-End Resistance Tolerance =  $\pm$  20% Noise = < -120dB/ Hz Ref: 1V (Thermal) Absolute Linearity =  $\pm$  0.75 LSB typical Relative Linearity = ± 0.3 LSB typical

Temperature Coefficient = ± 800 PPM/°C typical

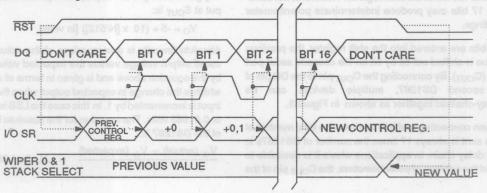
## NOTES:

- Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
- Relative linearity is used to determine the change in voltage between successive tap positions.
- Typical values are for t<sub>A</sub> = 25°C and nominal supply voltage.

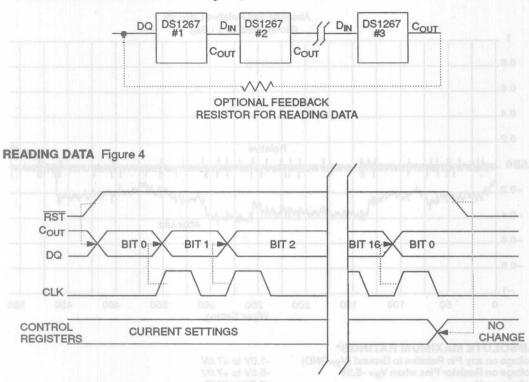
# **BLOCK DIAGRAM** Figure 1



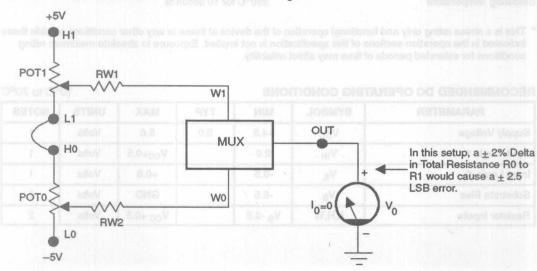
## **WRITING DATA** Figure 2



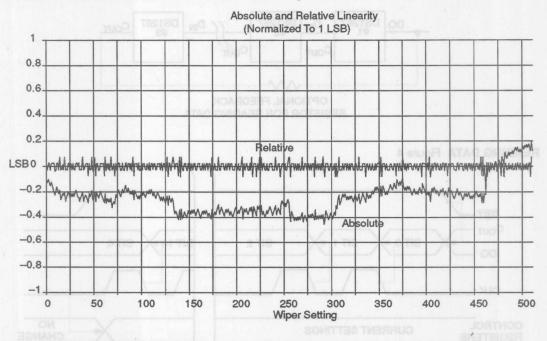
## CASCADING MULTIPLE DEVICES Figure 3



# **LINEARITY MEASUREMENT CONFIGURATION** Figure 5



# DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



## **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground (V<sub>B</sub>=GND) Voltage on Resistor Pins when V<sub>B</sub>= -5.5V

Voltage on V<sub>B</sub>

Operating Temperature Storage Temperature

Soldering Temperature

-1.0V to +7.0V -5.5V to +7.0V

-5.5V to GND

-0°C to 70°C -55°C to +125°C

260°C for 10 seconds

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	+4.5	5.0	5.0	Volts	1
Input Logic 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5	Volts	1
Input Logic 0	V <sub>IL</sub>	-0.5		+0.8	Volts	1
Substrate Bias	V <sub>B</sub>	-5.5	ow	GND	Volts	Sorte
Resistor Inputs	L,H,W	V <sub>B</sub> -0.5	3120	V <sub>CC</sub> +0.5	Volts	2

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

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## DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I <sub>CC</sub>		22	650	μА	6
Input Leakage	lu lu	-1		+1	μА	
Wiper Resistance	R <sub>W</sub>		400	1000	Ohms	
Wiper Current	I <sub>W</sub>	- n	1		mA	
Output Leakage	ILO	-1	-	+1	μА	
Logic 1 Output @ 2.4 Volts	loh	-1.0		-	mA	4
Logic 0 Output @ 0.4 Volts	l <sub>OL</sub>			4	mA	4
Standby Current	I <sub>STBY</sub>		22		μА	

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>	5/4	N/L	7	pF	

## AC ELECTRICAL CHARACTERISTICS

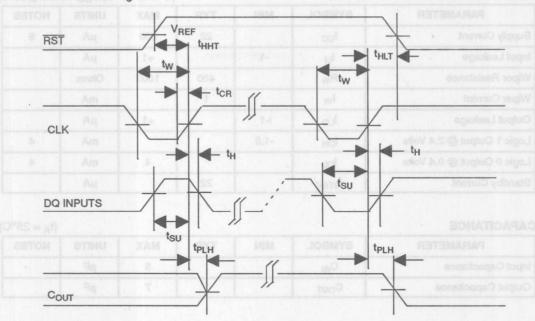
 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

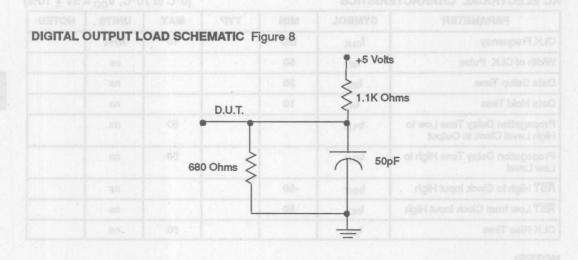
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f <sub>CLK</sub>	DC	1 DITAME	10	MHz	LATER
Width of CLK Pulse	t <sub>W</sub>	50			ns	
Data Setup Time	tsu	30			ns	
Data Hold Time	t <sub>H</sub>	10	Tue		ns	
Propagation Delay Time Low to High Level Clock to Output	t <sub>PLH</sub>			50	ns	
Propagation Delay Time High to Low Level	oa <sup>t</sup> PLH		≤ amdO (	50	ns	
RST High to Clock Input High	tннт	50	f .		ns	
RST Low from Clock Input High	t <sub>HLT</sub>	50	J		ns	
CLK Rise Time	t <sub>CR</sub>			50	ns	

### NOTES:

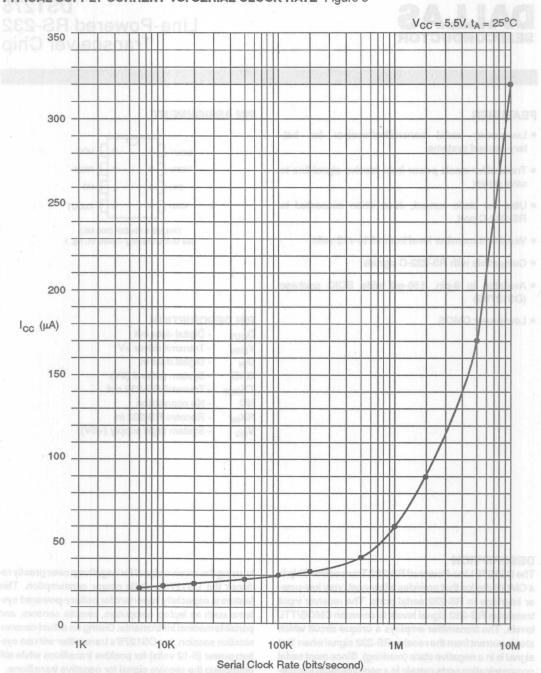
- 1. All voltages are referenced to ground.
- 2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction.
- 3. Measured with a load as shown in Figure 8.
- 4. V<sub>REF</sub> = 1.5 volts.
- 5. See Figure 9.

## TIMING DIAGRAM Figure 7





# TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 9



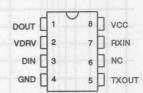


DS1275 Line-Powered RS-232 Transceiver Chip

#### **FEATURES**

- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-C port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-C signals
- Available in 8-pin, 150-mil wide SOIC package (DS1275S)
- Low-power CMOS

#### PIN ASSIGNMENT



DS1275 8-Pin DIP (300 Mil.) See Mech. Drawing - Sect. 16, Pg. 1

# PIN DESCRIPTION

D<sub>OUT</sub> - Digital data out
V<sub>DRV</sub> - Transmit driver +V
D<sub>IN</sub> - Digital data in
GND - System ground (0V)
TX<sub>OUT</sub> - Transmit RS-232 out

NC - No connection RX<sub>IN</sub> - Receive RS-232 in

V<sub>CC</sub> - System logic supply (+5V)

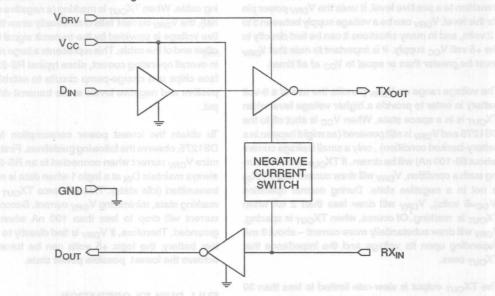
#### DESCRIPTION

The DS1275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statical-

ly, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

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# **DS1275 BLOCK DIAGRAM** Figure 1



#### **OPERATION**

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended. power will statically flow into that port, draining the battery capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RXIN) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TX<sub>OUT</sub>) when data is sent. However, since synchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

#### RECEIVER SECTION

The RX $_{IN}$  pin is the receive input for an RS-232 signal whose levels can range from  $\pm$  3 to  $\pm$  15 volts. A nega-

tive data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RX<sub>IN</sub> is D<sub>OUT</sub> which swings from +V<sub>CC</sub> to ground. Therefore, a mark on RX<sub>IN</sub> produces a logic 1 at D<sub>OUT</sub>; a space produces a logic 0.

The input threshold of RX<sub>IN</sub> is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause D<sub>OUT</sub> to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause D<sub>OUT</sub> to switch again. An open on RX<sub>IN</sub> is interpreted as a mark, producing a logic 1 at D<sub>OUT</sub>.

## TRANSMITTER SECTION

 $D_{IN}$  is the CMOS/TTL-compatible input for digital data from the user system. A logic 1 at  $D_{IN}$  produces a mark (negative data signal) at  $TX_{OUT}$  while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the  $RX_{IN}$  line for swinging to negative levels. The  $RX_{IN}$  line must be in a marking or idle state to take advantage of this design; if  $RX_{IN}$  is in a spacing state,

 $TX_{OUT}$  will only swing to ground. When  $TX_{OUT}$  needs to transition to a positive level, it uses the  $V_{DRV}$  power pin for this level.  $V_{DRV}$  can be a voltage supply between 5 to 12 volts, and in many situations it can be tied directly to the +5 volt  $V_{CC}$  supply. It is important to note that  $V_{DRV}$  must be greater than or equal to  $V_{CC}$  at all times.

The voltage range on  $V_{DRV}$  permits the use of a 9-volt battery in order to provide a higher voltage level when  $TX_{OUT}$  is in a space state. When  $V_{CC}$  is shut off to the DS1275 and  $V_{DRV}$  is still powered (as might happen in a battery-backed condition), only a small leakage current (about 50-100 nA) will be drawn. If  $TX_{OUT}$  is loaded during such a condition,  $V_{DRV}$  will draw current only if  $RX_{IN}$  is not in a negative state. During normal operation ( $V_{CC}$ =5 volts),  $V_{DRV}$  will draw less than 2 uA when  $TX_{OUT}$  is marking. Of course, when  $TX_{OUT}$  is spacing,  $V_{DRV}$  will draw substantially more current — about 3 mA depending upon its voltage and the impedance that  $TX_{OUT}$  sees.

The TX<sub>OUT</sub> output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TX<sub>OUT</sub> should be inadvertently shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

#### **RS-232 COMPATIBILITY**

The intent of the DS1275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least ± 5 volts minimum when terminated by a 3K ohm load and V<sub>DRV</sub>=+5 volts. Typically a voltage of 4 volts will be present at TX<sub>OUT</sub> when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

#### **APPLICATIONS INFORMATION**

The DS1275 is designed as a low-cost, RS-232-C interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS1275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TX<sub>OUT</sub> output, the DS1275 only draws significant V<sub>DRV</sub> current when TX<sub>OUT</sub> transitions positively (spacing). This current flows primarily into the RS-232

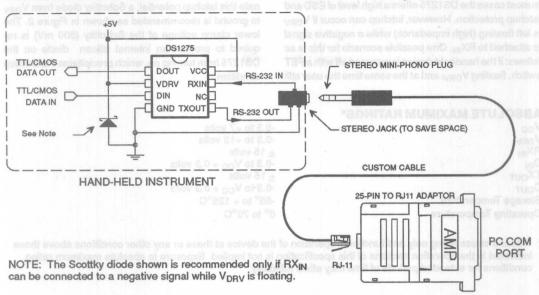
receiver's 3-7K ohm load at the other end of the attaching cable. When TX<sub>OUT</sub> is marking (a negative data signal), the V<sub>DRV</sub> current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

To obtain the lowest power consumption from the DS1275, observe the following guidelines. First, to minimize  $V_{DRV}$  current when connected to an RS-232 port, always maintain  $D_{IN}$  at a logic 1 when data is not being transmitted (idle state). This will force  $TX_{OUT}$  into the marking state, minimizing  $V_{DRV}$  current. Second,  $V_{DRV}$  current will drop to less than 100 nA when  $V_{CC}$  is grounded. Therefore, if  $V_{DRV}$  is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

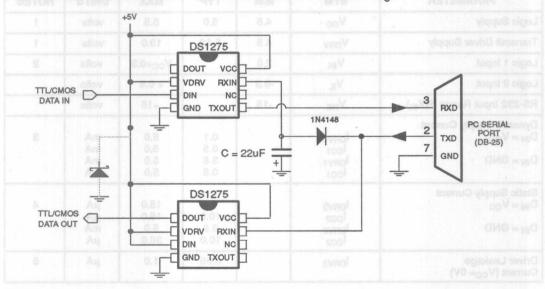
# **FULL-DUPLEX OPERATION**

The DS1275 is intended primarily for half-duplex operation; that is, RXIN should remain idle in the marking state when transmitting data out TX<sub>OUT</sub> and visa versa. However, the part can be operated full-duplex with most RS-232-C serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-C receiver device. The 5-volt swing occurs when TX<sub>OUT</sub> attempts to swing negative while RX<sub>IN</sub> is at a positive voltage, which turns on an internal weak pull-down to ground for the TX<sub>OUT</sub> driver's negative reference. So, transmit mark signals at TX<sub>OUT</sub> may have voltage jumps from some negative value (corresponding to RXIN marking) to approximately ground. One possible problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full-duplex circuit shown in Figure 3 can be used as an alternative. The 22 µF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TX<sub>OUT</sub> still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7K ohms). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TX<sub>OUT</sub> signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TX<sub>OUT</sub> to swing both positive and negative in full-duplex operation with this device.

# HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



# FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



#### NOTE:

The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS1275's TX<sub>OUT</sub> uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TX<sub>OUT</sub> is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TX<sub>OUT</sub>. However, when TXD is marking, the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

#### LATCHUP PROTECTION

In most cases the DS1275 offers a high level of ESD and latchup protection. However, latchup can occur if  $V_{DRV}$  is left floating (high impedance) while a negative signal is attached to  $RX_{IN}$ . One possible scenario for this is as follows: if the handheld device is powered off with a FET switch, floating  $V_{DRV}$ , and at the same time the user still

has the the RS-232-C port connected. In order to eliminate this latchup potential, a Schottky diode from  $V_{DRV}$  to ground is recommended as shown in Figure 2. The lower clamp voltage of the Schottky (300 mV) is required to prevent an internal silicon diode on the DS1275 from turning on, which precipitates the latchup condition.

#### **ABSOLUTE MAXIMUM RATINGS\***

Vcc VDRV RXIN DIN TXOUT DOUT Storage Temperature Operating Temperature -0.3 to +7 volts -0.3 to +13 volts ± 15 volts -0.3 to V<sub>CC</sub> + 0.3 volts ± 15 volts -0.3 to V<sub>CC</sub> + 0.3 volts -55° to + 125°C 0° to 70°C

## RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V <sub>CC</sub>	4.5	5.0	5.5	volts	1
Transmit Driver Supply	V <sub>DRV</sub>	4.5	5-12	13.0	volts	1
Logic 1 Input	VIH	2.0	DOV TUD	V <sub>CC</sub> +0.3	volts	2
Logic 0 Input	VIL	-0.3	SIXA VRO	+ 0.8	volts	MENUTT
RS-232 Input Range (RX <sub>IN</sub> )	V <sub>RS</sub>	-15	TUDKT ON	+15	volts	AIAO
Dynamic Supply Current D <sub>IN</sub> = V <sub>CC</sub> D <sub>IN</sub> = GND	I <sub>DRV1</sub> I <sub>CC1</sub> I <sub>DRV1</sub> I <sub>CC1</sub>	Russ	0.1 0.5 3.8 0.5	5.0 5.0 5.0 5.0	mA mA mA	3
Static Supply Current D <sub>IN</sub> = V <sub>CC</sub> D <sub>IN</sub> = GND	I <sub>DRV2</sub> I <sub>CC2</sub> I <sub>DRV2</sub> I <sub>CC2</sub>		1.5 10.0 3.8 10.0	15.0 15.0 5.0 30.0	μΑ μΑ mA μΑ	4 DATAQ
Driver Leakage Current (V <sub>CC</sub> = 0V)	I <sub>DRV3</sub>		0.05	1.0	μА	5

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

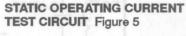
(0° to	70°C	Voc=	VDDV =	5V +	10%)
10 10	100.	A ( .(	A 1 1 1 1 1	OAT	10/01

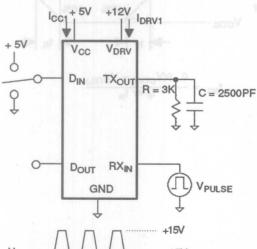
PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
TX <sub>OUT</sub> Level High	V <sub>OTXH</sub>	3.5	4.0	4.5	volts	6
TX <sub>OUT</sub> Level Low	V <sub>OTXL</sub>	-8.5	-9.0	7	volts	7
TX <sub>OUT</sub> Short Circuit Current	I <sub>SC</sub>		+60	+85	mA	
TX <sub>OUT</sub> Output Slew Rate	t <sub>SR</sub>			30	V/µs	
Propagation Delay	t <sub>PD</sub>		5	100	μѕ	8
RX <sub>IN</sub> Input Threshold Low	V <sub>TL</sub>	0.8	1.2	1.6	volts	
RX <sub>IN</sub> Input Threshold High	V <sub>TH</sub>	1.6	2.0	2.4	volts	
RX <sub>IN</sub> Threshold Hysteresis	V <sub>HYS</sub>	0.5	0.8		volts	9
D <sub>OUT</sub> Output Current @ 2.4 V	Гон	-1.0	81-ot 8- C	-L.xa	mA	
D <sub>OUT</sub> Output Current @ 0.4 V	I <sub>OL</sub>			3.2	mA	Y

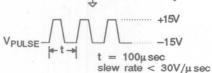
#### NOTES:

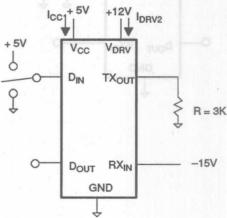
- V<sub>DRV</sub> must be greater than or equal to V<sub>CC</sub>.
- $V_{CC} = V_{DRV} = 5V \pm 10\%$ .
- See test circuit in Figure 4.
- See test circuit in Figure 5.
- See test circuit in Figure 6.
- DIN = VIL and TX<sub>OUT</sub> loaded by 3K ohms to ground.
- $D_{IN} = V_{IH}$ ,  $RX_{IN} = -10$  volts and  $TX_{OUT}$  loaded by 3K ohms to ground.
- D<sub>IN</sub> to TX<sub>OUT</sub> see Figure 7.
- VHYS = VTH VTL.

# **DYNAMIC OPERATING CURRENT TEST CIRCUIT** Figure 4

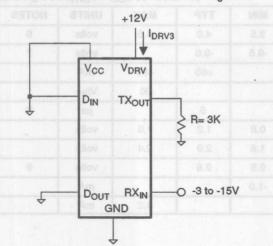




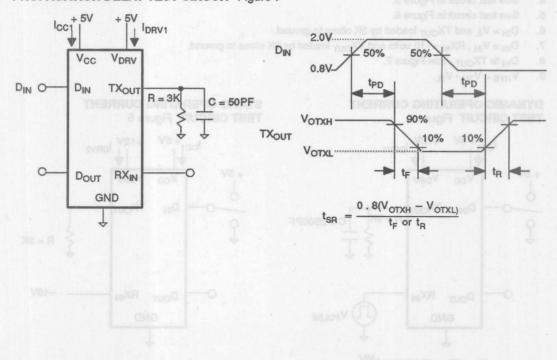




# **DRIVER LEAKAGE TEST CIRCUIT** Figure 6



# **PROPAGATION DELAY TEST CIRCUIT** Figure 7



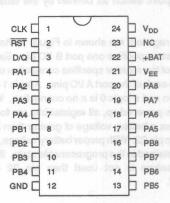


# 8-Channel Crosspoint Switch

#### **FEATURES**

- Any port A input/output can be programmed for connection to any port B input/output
- Registers which define port connections are programmable via a 3—wire serial port
- All port input/output pins will accept both analog and digital signals
- Optional +5 volts and ±5 volts operation
- Switch registers can be made nonvolatile with external connection of a 3-volt lithium battery
- Applications include:
- digital/analog switching and multiplexing
- data scrambling for secure transmission

#### **PIN ASSIGNMENT**



24-Pin DIP (600 mil) See Mech. Drawing Sect. 16, Pg 4

# PIN DESCRIPTION

+BAT - Battery Input
NC - No Connection

V<sub>EE</sub> - Optional -5 Volts Supply Input

PA1 - PA8 - Port A Input/Output

GND - Ground

PB1 - PB8 - Port B Input/Output

D/Q - Serial Port Data Input/Output

 CLK
 Serial Port Clock

 RST
 Serial Port Reset

 V<sub>DD</sub>
 5 Volts Power Supply

#### **DESCRIPTION**

The DS1277 8-Channel Crosspoint Switch Chip is a programmable, low-power CMOS switching device which has the capacity to interconnect eight digital or analog signals in any combination. Interconnection is controlled by eight data registers of eight bits each which are read and written via a 3-wire serial port. The

eight registers define the 64 possible combinations of the internal crosspoint switch. The DS1277 can be operated from a single +5 volts supply or optional ±5 volts operation can be selected to allow inputs and outputs to swing above and below ground.

#### **OPERATION - GENERAL**

With the -5 volts input grounded and +5 volts applied to pin 24, input/output pins of ports A and B will accept voltage levels between 0 and 5 volts. When V<sub>EE</sub> is connected to -5 volts with +5 volts applied to pin 24, the input/output pins of ports A and B will accept voltage levels between -5 and +5 volts. Regardless of the voltage selections, applied voltages on port pins will be reproduced on pins which are interconnected by the internal crosspoint switch as defined by the data register settings.

The data registers are shown in Figure 1. As defined, each register specifies one port B I/O pin. Each of the eight bits of the register specifies connection or no connection to each of the port A I/O pins. A logic 1 causes a connection and a logic 0 is a no connection. When the DS1277 is powered up, all register bits are forced to a zero unless a battery voltage of greater than 2 volts is present on pin 22. With proper battery voltage, all registers are retained in the programmable state. If the nonvolatile feature is not used then pin 22 must be grounded.

#### **OPERATION - SERIAL PORT**

The eight data registers of the DS1277 are written and read via a 3-wire serial port consisting of RST, CLK, and D/Q. To initiate data transfer with the DS1277, RST is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines either a read or a write. If a match does not exist communication will be ignored. If the command register is properly loaded then communication is allowed to continue and the next 64 cycles to the DS1277 will either update the data registers or read the data register content when the data registers are being updated.

Switch settings are not affected until RST is driven low at the end of the 64-bit data transfer.

#### COMMAND WORD

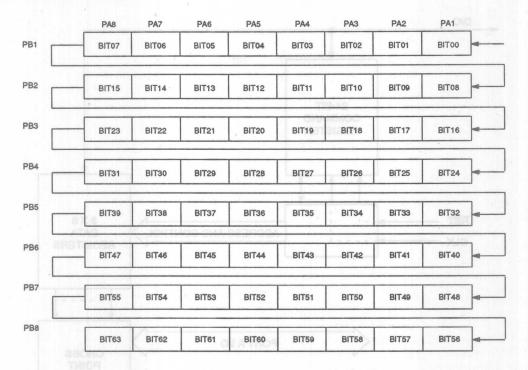
Each data transfer begins with a 3-byte command word as shown in Figure 3. The first byte of the command word specifies whether the 64-bit data registers will be written or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted. The 8-bit pattern for read is 01000110. The pattern for write is 10111001. The second and third bytes of the command word must match the exact pattern 00000000, 11110000 or data transfer is aborted.

#### **RESET AND CLOCK CONTROLS**

All data transfers are initiated by driving the RST input high. RST must remain high for the entire 24-bit command word and the 64-bit data stream. The RST input terminates communication and updates the switch settings only after all 64 bits of the data registers have been written when reset is driven low. Reading of registers can be terminated at any time by driving RST low.

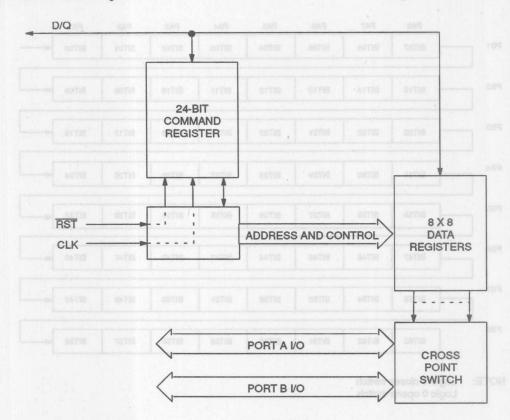
A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate and D/Q goes to a high impedance state if the RST input is low. Transfer of register data to switches occurs as RST is driven low only if 64 bits of data have been written. RST has no other effect on the register content. Data transfer is illustrated in Figures 4, 5 and 6.

# **DATA REGISTERS** Figure 1

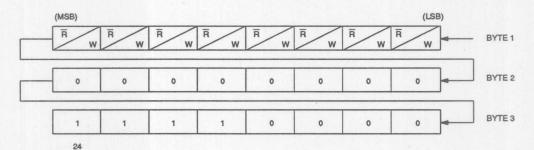


NOTE: Logic 1 closes switch Logic 0 opens switch

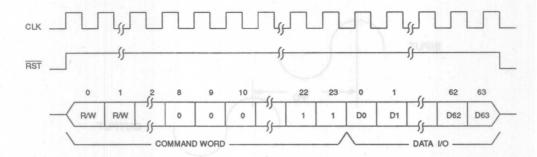
# **BLOCK DIAGRAM** Figure 2



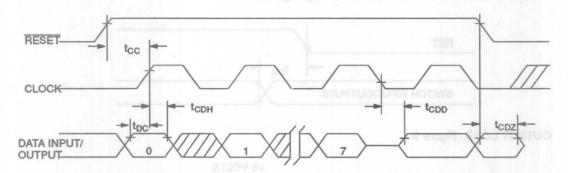
# **COMMAND REGISTER** Figure 3



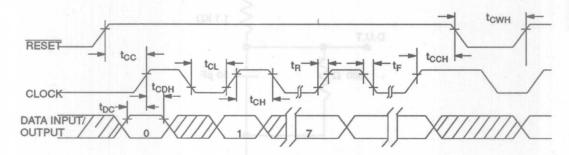
# COMMAND WORD/DATA TRANSFER Figure 4 10 40 TABLE AND ASSOCIATION AS



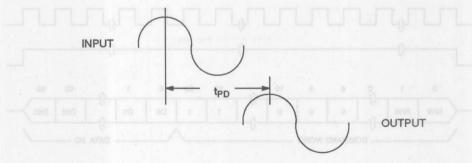
# **READ DATA TRANSFER** Figure 5



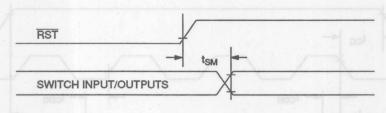
# WRITE DATA TRANSFER Figure 6



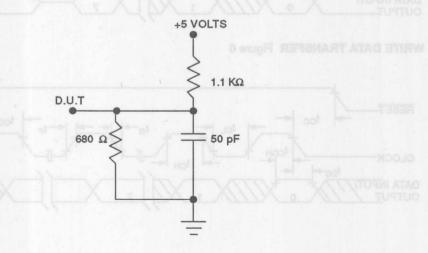
# TIMING DIAGRAM: SWITCH PROPAGATION DELAY Figure 7



# TIMING DIAGRAM: SWITCH CONNECT tpD Figure 8



# OUTPUT LOAD Figure 9



# 10

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground

-5.5V to +7.0V

Operating Temperature

Storage Temperature

Soldering Temperature

-5°C to 125°C

260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage		V <sub>DD</sub>	4.5	5.0	5.5	V	NUO di TRI
- Supply Voltage		VEE	0 08	-5.0	-5.5	V	TER di xuo
Serial Port Logic 0	7.5	V <sub>IL</sub>	-0.3	2002	0.8	V	SST B I/O
Serial Port Logic 1	50	V <sub>IH</sub>	2.0	asi	V <sub>DD</sub> +0.3	V	rput to Out
A @ B Port Input	08	V <sub>IN</sub>	0	Mod	V <sub>DD</sub>	V	-Supply=GND
A @ B Port Input		V <sub>IN</sub>	-V <sub>EE</sub>	HWDI	V <sub>DD</sub>	V	-Supply=-5.0V
+Battery Input		V <sub>BAT</sub>	2.5		3.7	V	1

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V<sub>FF</sub> = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
D/Q Output Current @ 2.4V	loh	ego 14 ig ren	GND: all of	volts, Vas	mA	2
D/Q Output Current @ 0.4V	loL	in beloenred	to sonstelse	+4	mA	2
Input Leakage	uaddling a	ngo (1 : 1/A -	GNO, RST.	es/+1 <sup>floy</sup>	μА	3
Output Leakage	loh	esti pumba	en en 01 bris	V8.0+1.1V1	μА	3
X Switch On Impedance	X <sub>ON</sub>		250	500	ohms	4
+ Supply Current Active	I <sub>DD1</sub>			10	mA	
+ Supply Current Quiescent	I <sub>DD2</sub>		7		mA	5
- Supply Current	I <sub>EE</sub>			1	mA	
X Switch Off Impedance	X <sub>OFF</sub>	1 Meg			ohms	
Battery Current @ 3V	I <sub>BAT</sub>			100	nA	1

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	
Feedthrough Capacitance	C <sub>IN</sub> -C <sub>OUT</sub>			10	pF	

# AC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{CC} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t <sub>DC</sub>	50			ns	6
CLK to Data Hold	t <sub>CDH</sub>	50			ns	6
CLK to Data Delay	t <sub>CDD</sub>	rebailt long	itaraqo tano	200	ns	2, 6, 7
CLK Low Time	t <sub>CL</sub>	250	menye ann ne may affen	o andeces i If to abolted	ns	6
CLK High Time	t <sub>CH</sub>	250			ns	6
CLK Frequency	SCLK	DC	TIOMOD &	2.0	MHz	6
CLK Rise and Fall	t <sub>RTF</sub>	MUN	LOUMY	500	ns	6
RST to CLK Setup	tcc	1 8 4	geV		μѕ	6
CLK to RST Hold	tcch	50	J 30V		ns	6
RST to I/O High Z	t <sub>CDZ</sub>	6,0-	Val.	75	ns	6
Input to Output Delay	t <sub>PD</sub>	0.\$	- InV	50	ns	I hoff lahe
RST Low to Switch Transition	t <sub>SM</sub>	0	te V	50	ns	mod S @
RST Inactive Time	tcwH	138V-	lu.A.		μѕ	G B Port

## NOTES

- 1. All voltages are referenced to ground (VSS).
- 2. Measured with a load as shown in Figure 9.
- 3.  $V_{DD} = +5$  volts,  $V_{EE} = -5$  volts,  $V_{SS} = GND$ : all other pins open.
- 4. X switch impedance is the terminal resistance of connected switch inputs to outputs.
- 5.  $V_{DD} = +5$  volts,  $V_{EE} = -5$  volts,  $V_{SS} = GND$ ,  $\overline{RST} = V_{IL}$ : all other pins open.
- 6. Measured at  $V_{IH} = 2.0$  or  $V_{IL} = 0.8V$  and 10 ns maximum rise ( $t_P$ ) and fall times ( $t_F$ ).
- 7. Measured at  $V_{OH} = 2.4$  volts and  $V_{OL} = 0.4$  volts.

# **FEATURES**

- Replaces 8 or 16 hard-to-get-at manual switches
- · Options printed circuit board via software
- Modular expansion by cascading packages
- · Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention for DS1290 and DS1292

#### **PIN ASSIGNMENT**

GND2	1	24	GND3		1	248		
₹ 🛚	2	23	VCC	Ŧ	2	238	VCC	
DI [	3	22	OA	DI	■3	228	OA	
00	4	21	ОВ	OQ	₿ 4	21 🗟	ОВ	
00 [	5	20	oc	00	■ 5	20	oc	
ON [	6	19	OD	ON	■ 6	19🛭	OD	
ом [	7	18	OE	OM	₿7	18	OE	
OL [	8	17	OF,	OL	8	178	OF	
ок 🛚	9	16	OG	ОК	9	16🛭	OG	
o [	10	15	ОН	OJ	10	15	ОН	
01	11	14	CLEAR	OI	₿ 11	148	CLEAR	
GND [	12	13	CLOCK	GND	■ 12	138	CLOCK	

DS1293 24-Pin DIP (300 Mil) See Mech. Drawing Sect. 16, Pg 1

DS1292 24-Pin Encapsulated Package (450 Mil) See Mech. Drawing - Sect. 16, Pg. 8

		30				
GND2	1	16 GND3		■ 1	16🛭	
Ŧ	2	15 VCC	Ŧ	1 2	15 🛭	vcc
DI	3	14 OA	DI	■3	148	OA
ом [	4	13 OB	OM	84	13 🛮	ОВ
og [	5	12 00	OG	■ 5	12	oc
OF [	6	11 OD	OF	86	11 📓	OD
OE	7	10 CLEAR	OE	₽7	10	CLEAR
GND	8	9 CLOCK	GND	■8	9 🛭	CLOCK
	_			_		

DS1291 16-Pin DIP (300 Mil) See Mech. Drawing Sect. 16, Pg 1 DS1290 16-Pin Encapsulated Package (450 MII) See Mech. Drawing - Sect. 16, Pg 8

# DESCRIPTION

The DS129x Eliminator replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

## PIN DESCRIPTION

CRIPTION
Transfer
Data Input
Switch Outputs
Clock Input
All Outputs Set Lo

V<sub>CC</sub> +5 Volts GND Ground

GND2 Missing on DS1292. Must be

grounded on DS1293.

GND3 Missing on DS1292. Must be

grounded on DS1293.

#### **OPERATION**

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see "Block Diagram" in Figure 1). The DS1290/DS1291 Eliminator is an 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input (T) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 00 through 0B remain in the state that was set prior to T being driven to a high level. Output 0A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the T input low (Figure 2). When the T input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 00 through 0A. When the T input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while T is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The CLEAR input will always set all outputs to low level regardless of the level of the CLOCK or T input.

#### **DATA RETENTION MODE**

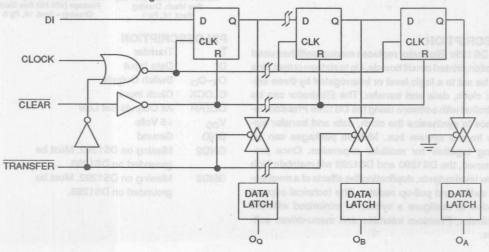
The DS129x Eliminator provides full functional capability when  $V_{CC}$  is greater than 4.5 volts and will ignore all inputs when  $V_{CC}$  reaches 4.25 volts typical. In this manner, the settings of each register remain intact during

power transients. As  $V_{CC}$  falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when  $V_{CC}$  rises above approximately 3 volts, the power switching circuit connects external  $V_{CC}$  to the shift register and disconnects the lithium energy source. Normal operation can resume after  $V_{CC}$  exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of  $V_{CC}$  if set to logic 1 and will remain at ground level if set to Logic 0.

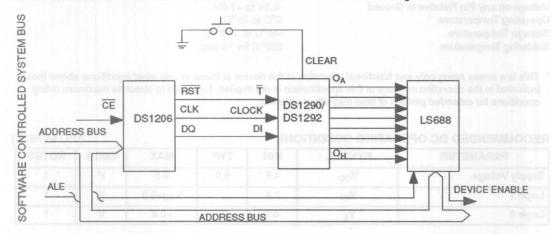
# TYPICAL APPLICATION - ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

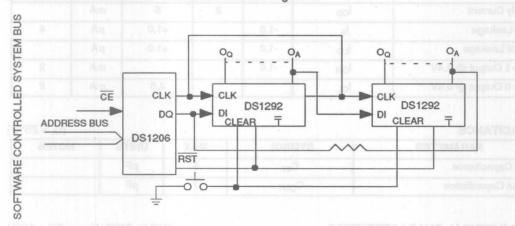
#### **BLOCK DIAGRAM - DS129x Figure 1**



# PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



# **MODULAR EXPANSION OF THE ELIMINATOR** Figure 3



# ABSOLUTE MAXIMUM RATINGS\*

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature

-0.3V to +7.0V 0°C to 70°C -40°C to +70°°C 260°C for 10 sec.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V	1
Logic 0	V <sub>IL</sub>	-0.3	esarqoa	+0.8	V	1

# DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C}; V_{\text{CC}} = 4.5\text{V to } 5.5\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc		3	5	mA	
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μА	4
Output Leakage	ILO	-1.0	60	+1.0	μА	
Logic 1 Output @ 2.4V	loH	-1.0			mA	2
Logic 0 Output @ 0.4V	l <sub>OL</sub>		and the last	4.0	mA	2

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PAIAGITANGE			morphis V	(tA - 20
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CIN	5	pF	
Output Capacitance	C <sub>OUT</sub>	- 070	pF	Waller of

# **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 10\%)$ 

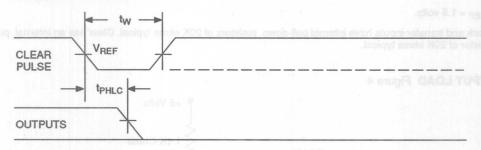
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	fcLock		100000	10	MHz	N 34
Width of Clock Pulse	twcLock	50			ns	3
Width of Clear Pulse	twcLEAR	50			ns	3
Data Setup Time	tsu	30			ns	3
Data Hold Time	t <sub>H</sub>	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	tPHLC			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t <sub>PLH</sub>			50	ns	3

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

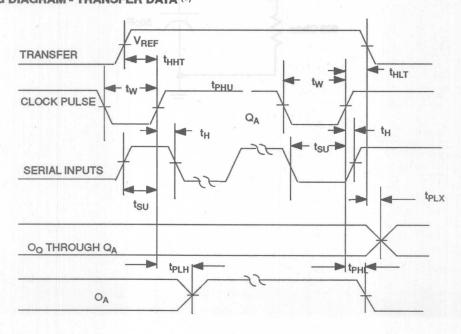
# AC ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay Time High to Low Level Clock to Output	t <sub>PHL</sub>	27.	4.25 VO	50	ns	3
Recovering on Power-Up	t <sub>REC</sub>	10	1038 -		ms	
Propagation Delay Time High to Low Level Transfer to O Out	t <sub>PLX</sub>	TW	Na.	50	ns	3
Transfer High to Clock Input High	tннт	50	777	777	ns	3
Transfer Low from Clock Input High	tHLT	50			ns	3

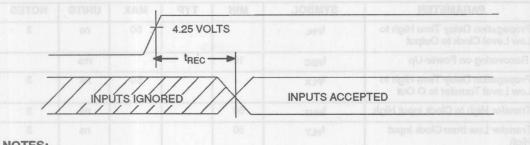
# TIMING DIAGRAM - CLEAR CONTROL (3)



# TIMING DIAGRAM - TRANSFER DATA (3)



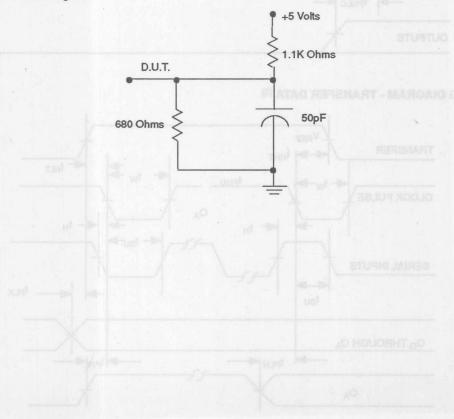
# TIMING DIAGRAM - POWER-UP (3)



## NOTES:

- 1. All voltages are referenced to ground.
- 2. Measured with a load as shown in Figure 4.
- 3.  $V_{REF} = 1.5$  volts.
- 4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

# **OUTPUT LOAD** Figure 4



# DS1632 PC Power Fail and Reset Controller

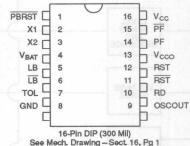
#### **FEATURES**

- · Power fail detector for personal computers and workstations
- Connects directly to popular personal computer chip sets
- On chip 32.768 KHz oscillator for real time clock
- Provides battery backup power to clock chip
- Pushbutton reset input
- Accurate 5% or 10% +5 volt power supply monitoring
- · Complementary outputs for reset, power fail, and low battery
- Provides for reset pulse width of either 100 ms or
- Eliminates the need for discrete components
- Low-power CMOS circuitry
- 16-pin DIP or SOIC surface mount package
- 0°C to 70°C operation

# DESCRIPTION

The DS1632 PC Power Fail and Reset Controller is designed to do various functions involving battery backup and other functions typically accomplished with discrete components. The DS1632 provides a 32.768 KHz battery backed up crystal oscillator and switched V<sub>CC</sub>/V<sub>BAT</sub> power via V<sub>CCO</sub> for the real-time clock function located in accompanying chip sets. In addition, the DS1632 provides for reset on both power up and via pushbutton

#### **PIN ASSIGNMENT**



	-	-	_		
PBRST CIL	1	0	16	П	Vcc
X1 🗆	2		15	Ш	PF
Х2 Ш	3		14	田	PF
V <sub>BAT</sub> III	4		13		Vcco
LB CIL	5		12		RST
LB CIL	6		11		RST
TOL CIL	7		10		RD
GND III	8		9		OSCOUT
	1				

16-Pin SOIC (300 Mil) See Mech. Drawing - Sect. 16, Pg. 6

#### PIN DESCRIPTION

**PBRST** Pushbutton Reset Input

Crystal Inputs X1, X2 **Battery Input** VBAT LB, LB Low Battery Outputs

RST, RST **Reset Outputs Reset Duration** RD

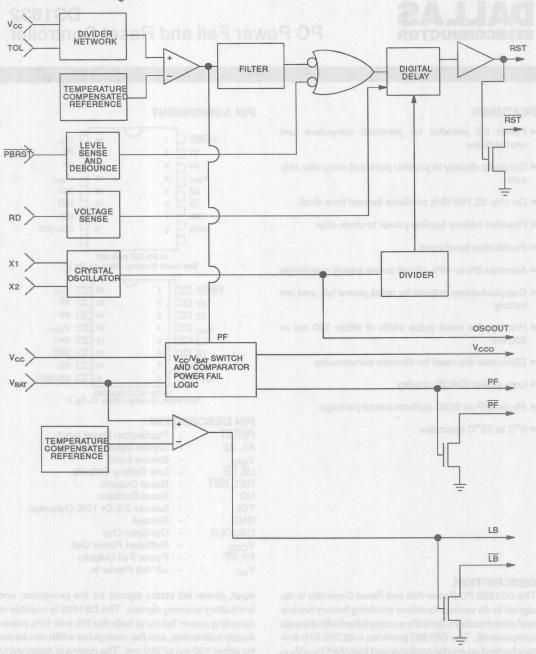
TOL Selects 5% Or 10% Detection

Ground GND Oscillator Out OSCOUT V<sub>CCO</sub> PF, PF Switched Power Out Power Fail Outputs

+5 Volt Power In Vcc

input, power fail status signals for the processor, and low battery warning signals. The DS1632 is capable of detecting power failure at both the 5% and 10% power supply tolerances, and the reset pulse width can be set for either 100 ms or 200 ms. The device is designed to connect directly to popular laptop and notebook chip sets which eliminates the need for discrete components and reduces cost. (See Figure 1.)

# **BLOCK DIAGRAM** Figure 1



# 10

# OPERATION - CRYSTAL OSCILLATOR SECTION

The DS1632 crystal oscillator is designed to be hooked directly to a 32.768 KHz crystal. By using the Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, the oscillator will be accurate enough to run a real time clock to within  $\pm 2$  minutes per month. If another crystal is to be selected, it should have a specified load capacitance (C<sub>L</sub>) of 6 pF. The crystal oscillator will run as long as either V<sub>CC</sub> or V<sub>BAT</sub> is present, providing that V<sub>BAT</sub> is greater than 2.3V. The oscillator output provides a rail to rail swing with regards to V<sub>CC</sub> or V<sub>BAT</sub>, whichever is greater. The crystal oscillator is also used internally as a time base.

# OPERATION – POWER FAIL, BATTERY BACKUP

The DS1632 provides a switch to direct power from the battery (V<sub>BAT</sub>) or the incoming supply (V<sub>CC</sub>) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The V<sub>CC</sub> input is constantly monitored by a precision comparator for an out of tolerance condition. When such a condition occurs, the power fail signals are driven to their active state immediately. The reset signals are also driven active, but this action is delayed by a time determined by the level of the input on the reset duration pin (RD). If RD is tied to ground then reset signals will become active after 10 ms. If RD is tied to V<sub>CC</sub>, then reset signals will become active after 20 ms. Once active, both the reset signals and the power fail signals will remain active as long as a (V<sub>CC</sub>) out of tolerance condition persists. If an out of tolerance condition is not long enough to activate the reset signals, then only the power fail signals would be affected. When power returns to within nominal limits the power fail signals will return immediately to the inactive state. However, the reset signals remain in the active state for a time which is dependent on the state of the RD pin. If RD is tied to ground, the reset signals will remain active for 100 ms. If RD is tied to VCC, then the reset signals will remain active for 200 ms after power is within nominal limits. The delay action on the reset signals allows time for the power supply and microprocessor clock oscillators to stabilize. The tolerance pin (TOL) selects the point at which power fail detection occurs. With the tolerance pin grounded, power fail detection occurs in the range of 4.75V to 4.5V. If the tolerance pin is connected to V<sub>CC</sub>, then power fail detection occurs in the range of

4.5V to 4.25V. During most power supply conditions the V<sub>CC</sub> input will supply power to all functions within the chip and also to the V<sub>CCO</sub> pin. The battery pin (V<sub>BAT</sub>) only supplies power when V<sub>CC</sub> is less than V<sub>BAT</sub>. When Vcc is below the level of VBAT only the Vcco and the OSC OUT pin remain powered by VBAT. All other outputs will be driven to ground when in a logic low state and will be driven to V<sub>CC</sub> when in a logic high state. This is done to preserve battery capacity by avoiding battery drain resulting from loads on these outputs. The output ground level will be maintained for all levels of Vcc. even V<sub>CC</sub> = GND. However, the output V<sub>CC</sub> level will be maintained only for V<sub>CC</sub> > 2.0V. Internal battery power consumption is less than 2 µA while VBAT is supplying power. The external load on OSC OUT and Voco must be added to internal consumption to determine the total load on the battery.

# **OPERATION - PUSHBUTTON RESET**

The DS1632 provides an input pin for direct connection to a pushbutton. The pushbutton reset input PBRST requires an active low level input. While TTL levels are sufficient to properly activate this input, it has been primarily designed for contact closure. Internally, this input is debounced and timed such that RST and RST signals of 100 ms or 200 ms minimum are generated. If RD is tied to ground, then a reset pulse of 100 ms is generated. If RD is tied to V<sub>CC</sub> then a reset pulse of 200 ms is generated. The delay time is started as the pushbutton reset input is released from low level.

#### **OPERATION - LOW BATTERY WARNING**

The DS1632 provides outputs which warn of a low battery condition. Whenever  $V_{CC}$  is within nominal limits, the  $V_{BAT}$  input is continuously monitored. If the  $V_{BAT}$  input is below 2.5V, the low battery outputs are driven to their active states, and will remain in the active state as long as  $V_{CC}$  is within nominal limits or until the battery input is restored to an in limit status. On power up, if the  $V_{BAT}$  input is below 2.5V, the low battery outputs are not guaranteed active until power fail is deactivated, but guaranteed active prior to reset inactive. When  $V_{CC}$  is below the  $V_{CC}$  fail trip point both LB and  $\overline{LB}$  will be driven to ground.

For application information, please reference Application Note #64, published separately.

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to +7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.0	5.5	٧	e tirpe base
PBRST Input High Level	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	٧	1,3
PBRST Input Low Level	V <sub>IL</sub>	-0.3	7735	+0.8	V	1,3
Battery Supply Voltage	V <sub>BAT</sub>	2.3	3.0	3.5	V	180 m

# DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = 4.5 \text{ to }5.5\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 2.4V	ГОН	ogliuse1 (	rediately. The	ımi etate ev	mA	5, 7
Output Current @ 0.4V	loL	0014	p tugni erir idi	by the lave	mA	7
Output Voltage @ -500 μA	V <sub>OH</sub>	V <sub>CC</sub> -0.5V	V <sub>CC</sub> -0.1V	belt at GR I	(CFV gno	6
Operating Current	lcc	sneneo X	0.5	2.0	mA	2
V <sub>CC</sub> Trip Point (TOL=GND)	V <sub>CCTP</sub>	4.50	4.62	4.75	V	bs 8010 .
V <sub>CC</sub> Trip Point (TOL=V <sub>CC</sub> )	V <sub>CCTP</sub>	4.25	4.37	4.50	V	1
Battery Fail Trip Point	V <sub>BATTP</sub>	2.30	2.45	2.55	of the A un Ba	ol ton 1 no
Supply Voltage Output	V <sub>cco</sub>	V <sub>CC</sub> -0.2	ewoo ertt atin	it toomon r	V	on power in
Supply Current Output	I <sub>CCO1</sub>	EBA BUIL	inactive state	100	mA	4

# DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C; V_{CC} = < V_{BAT})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I <sub>BAT</sub>	INTERIOR	ewolla alsng	2	μА	ant Lathmal
Battery Backup Current	I <sub>CCO2</sub>	waled	atfalpeles (.	500	μА	ala o 4 o ta

# CAPACITANCE

	(ta	= 25°C)

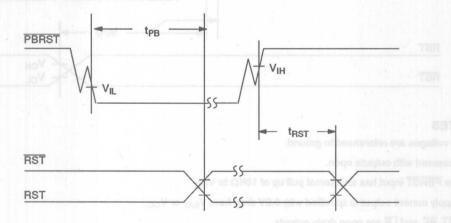
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>	Valu	1 ware	7	pF	0.

# AC ELECTRICAL CHARACTERISTICS

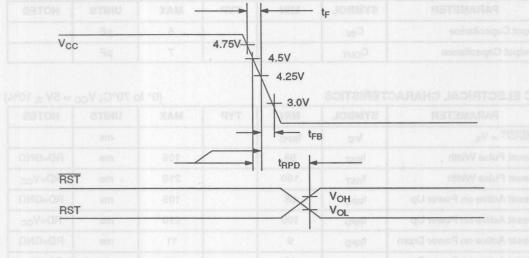
$(0^{\circ} \text{ to } 70^{\circ}\text{C}; V_{CC} = 5\text{V} \pm$
---

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST = V <sub>IL</sub>	t <sub>PB</sub>	t <sub>RPD</sub>	-		ms	
Reset Pulse Width	t <sub>RST</sub>	95		105	ms	RD=GND
Reset Pulse Width	t <sub>RST</sub>	190		210	ms	RD=V <sub>CC</sub>
Reset Active on Power Up	t <sub>RPU</sub>	95		105	ms	RD=GND
Reset Active on Power Up	t <sub>RPU</sub>	190		210	ms	RD=V <sub>CC</sub>
Reset Active on Power Down	t <sub>RPD</sub>	9		11	ms	RD=GND
Reset Active on Power Down	t <sub>RPD</sub>	18		22	ms	RD=V <sub>CC</sub>
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub>	300			μѕ	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub>	10			μѕ	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub>	10	Mar A		μs	

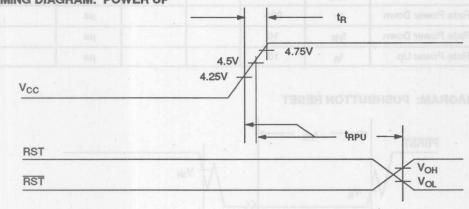
# TIMING DIAGRAM: PUSHBUTTON RESET



### TIMING DIAGRAM: POWER DOWN



# TIMING DIAGRAM: POWER UP



#### **NOTES**

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. The PBRST input has an internal pull up of 10KΩ to VCC.
- 4. Supply current output is specified with 0.2V drop from VBAT or VCC.
- 5. RST, PF, and LB are open drain outputs.
- 6. RST and PF remain within 0.5 volts of  $V_{CC}$  on power down until  $V_{CC}$  drops below 2.0V.
- 7. Sink and source currents apply to all outputs except OSC OUT which has a drive capability of sourcing 500  $\mu$ A at  $V_{OH} = V_{CCO}$  0.5V and sinking 1 mA at  $V_{OL} = 0.5$  V.

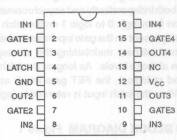


# DS1640/DS1640C Personal Computer Power FET

#### **FEATURES**

- Contains four P channel power FET switches that can each supply over 300 mA @ 0.2 volts drop
- · Controlled directly from CMOS or TTL level signals
- Fast switching time of less than 10 µs at rated supply current
- 16-pin DIP or 16-pin SOIC surface mount package
- Positive logic signal turns each FET on and ground or low level signal turns each FET off
- Off condition allows less than 50 nA of current flow
- · Low control gate capacitance of less than 5 pF
- · FET gates can either follow inputs or be latched
- Designed for use with power supplies ranging from +3 to +5 volts

#### **PIN ASSIGNMENT**



16-Pin DIP (300 Mil) See Mech. Drawing - Sect. 16, Pg. 1



16-Pin SOIC (300 Mil) See Mech. Drawing - Sect. 16, Pg. 6

#### PIN DESCRIPTION

V<sub>CC</sub> - +3 to+5 Volt Input

GND - Ground
IN1-IN4 - FET Sources
OUT1-OUT4 - FET Drains

GATE1-GATE4 - FET Control Gates
NC - No Connection

LATCH - Gate Inputs Latch Control

# DESCRIPTION

The DS1640 contains four P channel power MOS FET's designed as switches to conserve power in personal computer systems. When connected to power management control units, power consuming devices like disk drives or display panel backlights can be routinely shut down to conserve battery or main power supply en-

ergy. The P channel power MOS FET's are individually controlled and are capable of handling 300 mA each continuously with less than 0.2 volts drop from input to output. The device requires a +3 \* +5 volt power supply input which is used to power internal logic and to operate a gate bias generator.

to the FET a myerted and pass

aroundanion of farming With +3 → +5 volts applied between the V<sub>CC</sub> pin and ground, any one of four inputs can be connected or disconnected from its respective output based on the bias applied to the control gate (see Figure 1). A set of four internal latches is controlled by the latch input. The logic levels passed to the FET gates are controlled by the gate inputs and latch pin status. When the latch pin is logic 0, the gate input levels are inverted and passed directly to the control gates, enabling the switches to be switched both independently and asynchronously. With a transition from logic 0 to logic 1 on the latch pin, the input levels present on the gate inputs are locked by the four internal latches, maintaining the corresponding

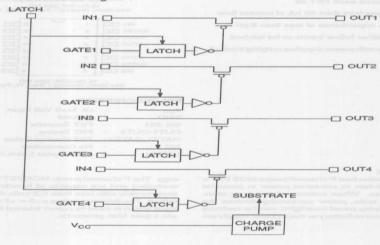
FET gates at those levels. As long as the latch input is

maintained at logic 1, the FET gate levels are main-

tained. When the latch input is returned to logic 0, the

gate inputs again are inverted and passed to the FET control gates without being latched. A TTL or CMOS logic 1 turns a switch completely on and TTL or CMOS logic 0 turns a switch completely off. The four switches can be operated independently or two or more can be connected in parallel for added current carrying capability. The four switches contained within the DS1640 are not designed to be operated in a linear manner. When V<sub>CC</sub> is not applied to the DS1640 or if V<sub>CC</sub> is not within nominal limits, the output levels and current carrying capability of the four switches are not guaranteed. When all four gate inputs are off (logic 0) the device enters a low Vcc current standby mode because the onboard charge pump is turned off. The gate and latch inputs are CMOS-compatible throughout the entire Voc range and are TTL-compatible when V<sub>CC</sub> falls between 4.5 and 5.5V.

#### DS1640 BLOCK DIAGRAM Figure 1



10

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.3V to +7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

# DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	hemnorivne	5.5	ens V ara	1,2
Logic 0 Input 3.0 V ≤ V <sub>CC</sub> ≤ 4.5 V	V <sub>IL2</sub>	-0.3	Joubons	+0.5	00 k V 30k	the DS14
Logic 0 Input 4.5 V ≤ V <sub>CC</sub> ≤ 5.0 V	V <sub>IL1</sub>	-0.3		+0.8	٧	1
Logic 1 Input 3.0 V ≤ V <sub>CC</sub> ≤ 5.0 V	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5	٧	1,7
Source Voltage	V <sub>SOURCE</sub>			V <sub>CC</sub> +0.5	V	1,7

#### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = +5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I <sub>CC1</sub>		0.3	1	mA	3
Supply Current	I <sub>CC2</sub>		0.1	1	μА	4
Switch Off Leakage	I <sub>SL</sub>			100	nA	
Switch On Resistance	Ron		0.3	.67	Ω	
Switch Current @ V <sub>F</sub> = 200 mV	Is			300	mA	5
Input Leakage	I <sub>IL</sub>	-1		+1	μА	6
Gate Input Capacitance	C <sub>G</sub>			5	pF	7

#### **AC ELECTRICAL CHARACTERISTICS**

 $(0^{\circ}\text{C to }70^{\circ}\text{C}; V_{CC} = +5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Switching Time (OFF → ON)	t <sub>STON</sub>			10	μs	
Switching Time (ON → OFF)	tSTOFF			10	μs	
Minimum Time to Engage Latch	t <sub>LM</sub>			50	ns	Partie !

<sup>\*</sup> This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### NOTES

- 1. All voltages are referenced to ground.
- 2. When V<sub>CC</sub> is below minimum limits output levels are not guaranteed.
- 3. I<sub>CC1</sub> is the supply current with one or more switches on.
- 4. I<sub>CC2</sub> is when all switches are off and all inputs are within 0.5V of a supply rail.
- 5. Each switch is capable of carrying 300 mA maximum at 200 mV forward drop.
- 6. Input leakage applies to the four gate inputs and the latch input only.
- 7. Applies to each of four gate inputs and the latch input.

V	nsumer grade	p. 3444		.ogic 0 Input 4.5 V ≤ V <sub>CC</sub> ≤ 5.0 V



# DS1652B Key Code Memory

## **FEATURES**

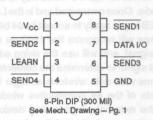
- The key forms the basis of a secure access system
- The DS1652B is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64 bit code prevents unauthorized copying of keys
- Each key capable of generating 4-code conditions.
- Keys are programmed from an external device only under controlled user access/secure conditions
- · Low cost, economical
- Key codes may be changed as many times as necessary
- 3V operation, 5V for programming
- −25°C to +85°C operating range
- All stored 64 bit codes in the key are non-volatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification.

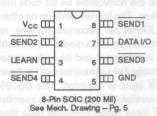
# DESCRIPTION

The DS1652B key operates as part of a system to limit access of any secure system or area to keyholders. The DS1652B key contain a 64 bit memory which acts as the security code, controlling access. Once set, the code is nonvolatile.

To gain access to a locked system, the key's code must be transmitted to the lock via some user transmission

#### **PIN ASSIGNMENT**





## **PIN DESCRIPTION**

LEARN

 Vcc
 - +3V to +7V Input

 GND
 - Ground

 DATA I/O
 - Serial Data Input/Output

 SEND1
 - Send Input 1

 SEND2
 - Send Input 2

 SEND3
 - Send Input 3

 SEND4
 - Send Input 4

- Learn Input

media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a lock system must compare the requesting key's 64 bit code to the lock's systems programmed code. If the key code matches the lock system code, the lock system must generate a match signal, which can be used to allow access to the secure system.

## **OPERATION DS1652B KEY**

The operation of the DS1652B key is shown in Figure 1. The key is programmed with code from an external source with the key in Learn mode.

For the DS1652B key to be programmed, the LEARN pin must be driven active high, with V<sub>CC</sub> on the DS1652B at 5V. The DS1652B key's data input/output pin must be physically connected to the external programming device for the DS1652B key to successfully accept a code. Once connected and in the Learn mode, the DS1652B key is ready to accept its 64 bit code. The DS1652B key will recognize the 1600 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the external programming device, become latched into the nonvolatile 64 bit code memory of the DS1652B key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652B to its operation mode. The DS1652B key will transmit a reset signal and its code memory out of its data input/output pin a maximum of ten times as long as the SENDX input is asserted. The DS1652B key will transmit a version of the code that is specifically tailored to SENDX input being triggered (see diagram, Page 10-141).

#### SERIAL PULSE PROTOCOL

The DS1652B transmits and receives data serially, according to the protocol listed in the timing diagram.

The transmission and reception of data begins with the rising edge of the 1600  $\mu$ s reset signal. The DS1652B then begins looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1652B will time the duration of the active pulse in each window. Once the pulse is inter-

preted as a 1 or a 0, the data bit is written to the 64 bit code memory. This iterative process continues through all 64 bits until they are written. For the DS1652B, after 64 bits are written, the key may be returned to its operation mode for use.

# **OPERATION, LOCK AND KEY**

The DS1652B key provides a security code matching system which can be used as the code control logic of any security system.

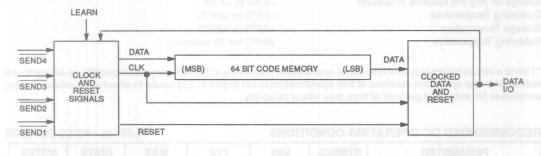
The DS1652B key is programmed from an external programming device and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of a DS1652B key based system is limiting the manner by which a key may be programmed with the code to open the lock. The only way in which a DS1652B key will accept code is to connect its data input/output pin directly to the external programming device. Therefore the only method of transferal is by physically connecting the device holding the DS1652B key with the device holding the programmer. A quick and efficient method of implementing this interface is illustrated on Page 10–137

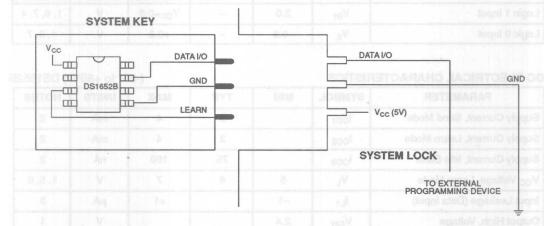
By designing the system key with three external leads, one tied to  $V_{\rm CC}(5V)$ , one tied to ground, and one tied to the input pin, the system key may accept a new code from a system lock only through these three connections

As many keys as needed may be programmed. As required for security purposes, or in case of the loss of a key a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.

# DS1652B KEY BLOCK DIAGRAM Figure 1



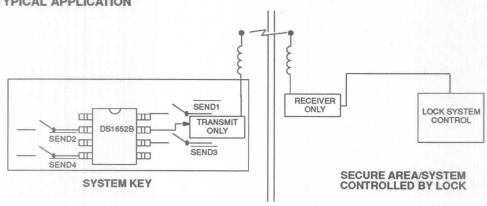
## INTERIOR OF LOCK SECURED AREA



## TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/ output pin of the DS1652B key to the system lock. For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1652B's serial pulse protocol may be used to link the key to the users lock system.

# TYPICAL APPLICATION



# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to +7.0V -25°C to +85°C -55°C to 125°C 260°C for 10 seconds

#### RECOMMENDED DC OPERATING CONDITIONS

(-25° to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.5	5.0	7.0	NOV.	ROBET
Logic 1 Input	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3	V	1, 6, 7, 4
Logic 0 Input	V <sub>IL</sub>	-0.3	J -	+0.8	V	1, 6, 7

#### DC ELECTRICAL CHARACTERISTICS

(-25° to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I <sub>CC1</sub>		3	4	mA	2
Supply Current, Learn Mode	I <sub>CC2</sub>		3	4	mA	2
Supply Current, Idle State	I <sub>CC3</sub>		75	100	nA	2
V <sub>CC</sub> Voltage, Learn Mode	VL	5	6	7	V	1, 5, 6
Input Leakage (Data Input)	I <sub>L1</sub>	-1		+1	μА	3
Output High, Voltage	V <sub>OH</sub>	2.4			V	1
Output High, Current	Іон	4	al bear shoulder	190 Innovatorel	mA	no act to
Output Low, Voltage	Vol	0.4	duta inb	rell of settime	mi TiVns s	u of alme
Output Low, Current	loL	1	_ Jour mere	s ean or Year	mA	to my aux

<sup>\*</sup>This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

# AC ELECTRICAL CHARACTERISTICS DS1652B KEY DATA TRANSMISSION PARAMETERS

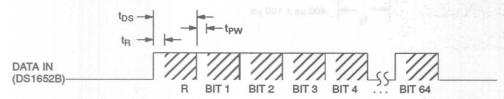
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t <sub>R</sub>	1200	1600	2000	μs	2000
Logic 1 Active	t <sub>1</sub>	600	800	1000	μs	ACM
Logic 0 Active	t <sub>0</sub>	300	400	500	μs	
Data Sample Window	t <sub>DS</sub>	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t <sub>PW</sub>	300	NIN	2000	μѕ	FUO ATAI
Active Signal Pulse Width SEND1, SEND2, SEND3, and SEND4	ts	10		20	ms	(2)
Delay Between LEARN Pin Transition and Operation Mode Change	, t <sub>T</sub>			10	ms	GIC TEN
Delay Between Minimum SENDX Assertion and Data Out Transmitted	t <sub>SD</sub>			100	μѕ	
Number of Words Transmitted for 1 SENDX Input Recognized		10				

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

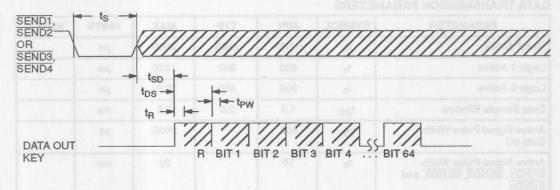
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		The state of	5	pF	
Output Capacitance	C <sub>OUT</sub>			7.	pF	

## **LEARN MODE DS1652B KEY**

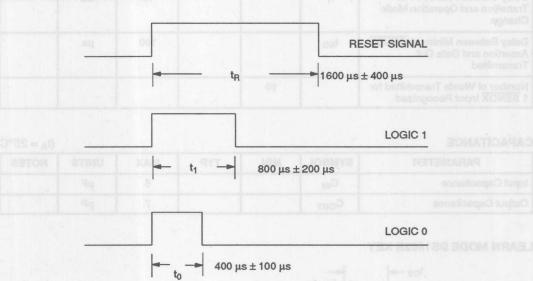




# **OPERATION DS1652B KEY**



# **LOGIC TIMING DIAGRAMS**



INPUT TRIGGERED				64 CODE	TRANSM	ITTED AS	- A A		
SEND1 (DATA)*	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND2 (DATA)	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND3 (ODD)	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND4 (EVEN)	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>

<sup>\*</sup>The bit pattern transmitted by the SEND1 trigger it the unaltered contents of the DS1652B code memory. SEND2, SEND3, and SEND4 transmit modified versions of this code a listed above.

### NOTES

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. Input leakage applies to DS1652B data input only.
- 4. Absolute maximum rating is 7.0V on any pin.
- Input voltage on the V<sub>CC</sub> pin is required to be in the Learn mode, for the DS1652B to properly accept new code data.
- 6. The DS1652B LEARN pin is internally pulled down with approximately a  $10K\Omega$  resistor.
- The DS1652B SEND1, SEND2, SEND3, and SEND4 inputs are internally pulled up with approximately 10KΩ resistors.



# DS1651 3-Code Lock, DS1652 Key Match Memory System

#### **FEATURES**

- The two chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64 bit code or internally generated random 64 bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 3-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- · Low cost, economical
- Lock codes may be changed as many times as necessary
- 3V operation, 5V for programming
- -25°C to +75°C operating range
- All stored 64 bit codes in the lock and key are non-volatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

### **PIN ASSIGNMENT**

Vcc III	1	8		SEND1
SEND2	2	7	田	DATA I/C
LEARN III	3	6	Ш	SEND3
SEND4	4	5		GND

DS1652 8-Pin DIP ( 300 MII) and DS1652S 8-Pin SOIC (200 MII) See Mech. Drawings – Sect. 16, Pgs. 1 & 5

V <sub>cc</sub> I		1	8		DATA I/O
SEND3 MATCH		2	7	Ш	SEND1 MATCH
MODE2	Ш	3	6		SEND2 MATCH
MODE1		4	5	Ш	GND

DS1651 8-Pin DIP (300 Mil) and DS1651S 8-Pin SOIC (200 Mil) See Mech. Drawings – Sect. 16, Pgs. 1 & 5

### **DS1652 PIN DESCRIPTION**

GND - Ground

 DATA I/O
 Serial Data Input/Output

 SEND1
 Send Input 1

 SEND2
 Send Input 2

 SEBD3
 Send Input 3

 SEND4
 Send Input 4

# LEARN - Learn Input

DS1651 PIN DESCRIPTION

MODE2 - Function Control Pin

MODE1 - Function Control Pin

Vcc - 43V to +7V Input

GND - Ground

DATA I/O
SEND1 MATCH
SEND2 MATCH
SEND3 MATCH
Code Match Signal for SEND2
SEND3 MATCH
Code Match Signal for SEND2
Code Match Signal for SEND3

### DESCRIPTION

The DS1651 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1651 Lock and DS1652 Key contain a 64 bit memory which acts as the security code, controlling access. The code memory within the DS1651 Lock may be user programmed with a known

64 bit code, or the DS1651 can generate a 64 bit code from a random number generator within the DS1651. Once set, the code is nonvolatile, and can then be transferred to a DS1652 Key(s) under secure conditions.

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To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a DS1651 Lock will compare the requesting key's 64 bit code to the lock's programmed 64 bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

### **OPERATION DS1651 LOCK**

The main functional components of both the DS1651 and DS1652 are shown in Figures 1 and 2. The diagram shows that the internal functions of the lock and key are similar. From Figure 1, the primary components of the lock are its 64 bit wide registers. The 64 bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64 bit data memory records the 64 bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1651 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE				
kej0 an	0	Operation Mode: Receiving codes from key(s).				
0	1	Learn Mode: Program with user provided 64 bit codes.				
tool 1 rigin	0	Duplicate Mode: Transmit 64-bit code memory contents.				
at at blood	lgeod <b>a</b> libe tugai atab sitom sina	Learn Mode: Program with internally generated random 64 bits.				

The Learn modes and duplicate mode may only be entered from operation mode. The DS1651 samples the level of MODE1 and MODE2 10 ms after a low to high transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating.

In the Learn modes, the DS1651 Lock's code memory may be either programmed directly by the user, or programmed using a random set of 1's and 0's created by the DS1651's random number generator. A user must have physical access to the DS1651 to place it in Learn mode. To place the DS1651 Lock in Learn mode, the DS1651's  $V_{\rm CC}$  input must be at 5V minimum with,

mode1 or both mode1 and mode2 pins driven high, telling the DS1651 to enable the contents of its code memory to be rewritten. If mode1 is high, then the DS1651 enables its code memory to be rewritten using a user defined 64 bit code, which it expects to see on its data I/O pin. At the end of sending the 64 bit code to the DS1651, the mode1 pin must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes, DS1651 Lock".) If mode2 and mode1 are high, then the DS1651 Lock performs an internal operation in which it uses its internal random number generator to create a 64 bit pattern of 1's and 0's and load it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1651 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1651 to operation mode, before entering any other mode.

The DS1651 will not reprogram its 64 bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its mode2 and mode1 pins.

For the DS1651 Lock to transfer its code memory into a DS1652 Key the DS1651 Lock must be in duplication mode. To enter the duplication mode, the mode2 pin must be driven high. The transition from 0 to 1 on the mode2 pin, and its maintenance at 1 causes the DS1651 Lock to transmit a reset signal followed by its 64 bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64 bit code copy. The data input/output pin of the DS1651 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1651 and DS1652.

The DS1651 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 us is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written in the data memory for compari-

son to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1651 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1651 performs no operations, but waits for the next reset signal.

### **OPERATION DS1652 KEY**

The operation of the DS1652 Key is similar to that of the DS1651 (Figure 2). The key is programmed with code generated by the DS1651 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1651 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1651 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64-bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64-bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the SENDX input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to SENDX input being triggered (see diagram, Page 10-151).

### SERIAL PULSE PROTOCOL

The DS1651 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1651 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical 0 is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1651 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1651 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key may be returned to its operation mode for use.

### OPERATION, LOCK AND KEY

The DS1651 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1651 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64—bit codes, that can only be changed by having physical access to the lock. If known codes are not required, the DS1651 can generate its own 64—bit code randomly. If the random number generator of the DS1651 Lock is used, not even the person programming the lock knows the 64 bit code.

The DS1652 Key is programmed from the DS1651 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of the DS1651 Lock is limiting the manner by which a lock may program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1651 Lock. Therefore the only method of transferal is by physically connecting the device holding the DS1652 Key with the device holding the DS1651 Lock. A quick and efficient method of implementing this interface is illustrated on page 4.

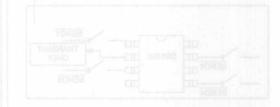
By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the Data I/O pin, the system key may accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1651 Lock

could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

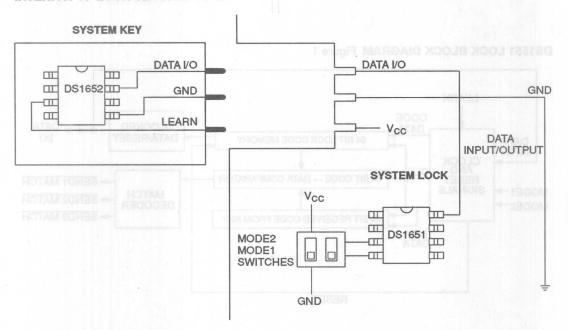
The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

- 1. limits who may program keys
- 2. limits who can generate codes for the lock
- limits who may, by generating a new code, invalidate the existing programmed keys.

As many keys as needed may be programmed. As required for security purposes or in case of the loss of a key, a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.



### INTERIOR OF LOCK SECURED AREA

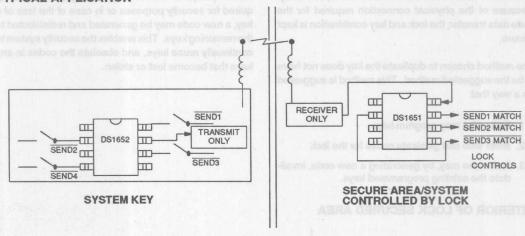


# TYPICAL APPLICATION

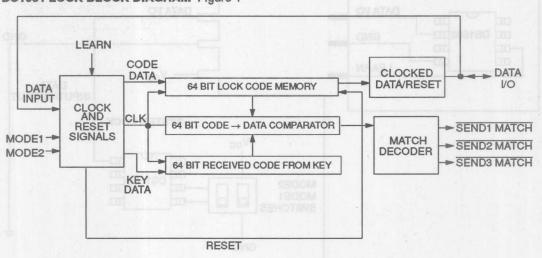
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/ output pin of the DS1652 Key to the DS1651's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1651 and DS1652's serial pulse protocol may be used to link the key to a lock.

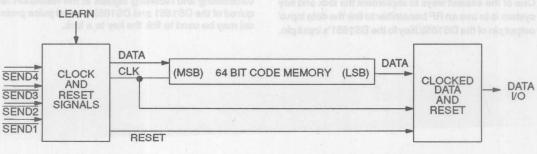
## TYPICAL APPLICATION



# DS1651 LOCK BLOCK DIAGRAM Figure 1



# DS1652 KEY BLOCK DIAGRAM Figure 2



021492 5/10

### **ABSOLUTE MAXIMUM RATINGS\***

-V-0.5V to +7.0V Voltage on Any Pin Relative to -V **Operating Temperature** -25°C to +75°C Storage Temperature -55°C to 125°C Soldering Temperature 260°C for 15 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(-25°C + 77°C) DS1651 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.5	5.0	7.0	V	leli deput
Logic 1 Input	V <sub>IH</sub>	2.0	Ver.	V <sub>CC</sub> +0.3	V	1, 6, 7, 8
Logic 0 Input	V <sub>IL</sub>	-0.3	I tol	+0.8	V	1, 6, 7, 8

### DC ELECTRICAL CHARACTERISTICS (-25°C to 75°C) DS1651

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I <sub>CC1</sub>	19125	3	4	mA	2
Supply Current, Learn Mode	I <sub>CC2</sub>	Uad .	3	4	mA	2
Supply Current, Idle State	I <sub>CC3</sub>	08	75	100	nA	2
Supply Current, V <sub>CC</sub> Pin, Learn Mode	I <sub>LRN</sub>	60	2	3	mA	AM TOKS
Output High, Voltage	V <sub>OH</sub>	2.4			V	1
Output High, Current	loн	6.1	80,	1	mA	qenus and
Output Low, Voltage	V <sub>OL</sub>	0.4	Well		V	1
Output Low, Current	l <sub>OL</sub>	4	The same	I Tovaa	mA	rani3 avito
I/O Leakage Current	I <sub>IO</sub>	-1		+1	μА	4

## DC ELECTRICAL CHARACTERISTICS

(-10°C to 70°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I <sub>CC1</sub>	-55°C	3	4	mA	2
Supply Current, Learn Mode	I <sub>CC2</sub>		3	4	mA	2
Supply Current, Idle State	I <sub>CC3</sub>	50	75	100	nA	2
V <sub>CC</sub> Voltage, Learn Mode	V <sub>L</sub>	5	6	7 one	V	1, 5, 6
Supply Current, Learn Mode	I <sub>LRN</sub>		2	3	mA	
Input Leakage (Data Input)	0 85-I <sub>L1</sub>	-1240	TIGHED E	+1	μА	3
Output High, Voltage	V <sub>OH</sub>	2.4	HAMBOL		V	1
Output High, Current	Іон	4	Jooy		mA	offely Velta
Output Low, Voltage	V <sub>OL</sub>	0.4	MIN		V	igni ipig
Output Low, Current	loL	1(8,0-	JgV.		mA	gic 0 Inpu

# AC ELECTRICAL CHARACTERISTICS DS1651 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

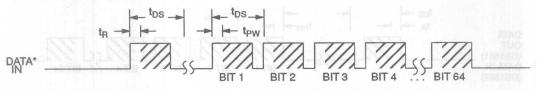
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t <sub>R</sub>	540	720	900	μѕ	riot0 vlack
Logic 1 Active	t <sub>1</sub>	90	120	150	μѕ	nu D vladu
Logic 0 Active	to	15	20	25	μѕ	unalv Gür
SEND1 MATCH, SEND2 MATCH, and SEND2 MATCH	t <sub>M</sub>	400	500	600	ms	boki mse iniH seto
Data Sample Window	t <sub>DS</sub>	1.5	2.0	2.5	ms	folkl tuetu
Active Signal Pulse Width, Data I/O	t <sub>PW</sub>	10	VoL	1080	μѕ	uspot Low
Active Signal Pulse Width SEND1 and SEND2	ts	100	Jol		ms	wour abque parked 0
Delay Between Last Mode Pin Transition to Operation Mode Change	t <sub>T</sub>		10		ms	

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

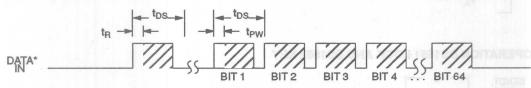
# LEARN MODE DS1651 LOCK; USER PROGRAMMING MARKET WERE SERVED STORE WITH A STATE OF THE PROGRAMMING WAS A STATE OF THE PROGRAM





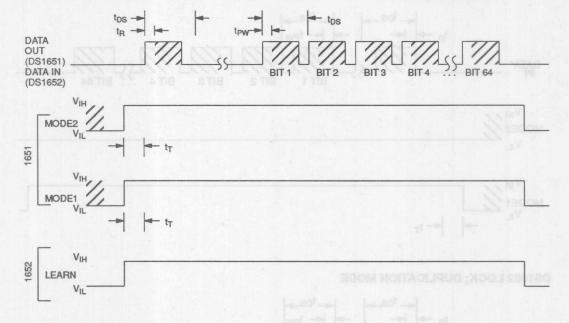


# **DS1652 LOCK; DUPLICATION MODE**

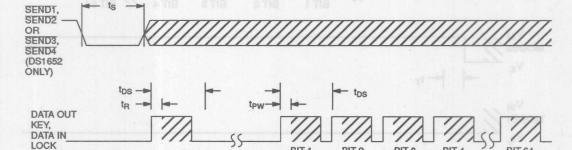




# LEARN MODE DS1652 KEY; LEARN MODE DS1651 LOCK, INTERNAL PROGRAMMING



# **OPERATION DS1651 LOCK AND DS1652 KEY**



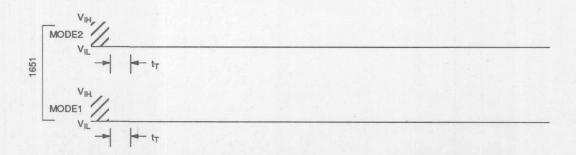
BIT 1

BIT 2

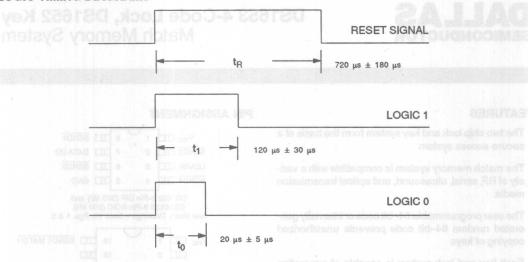
BIT 3

BIT 4

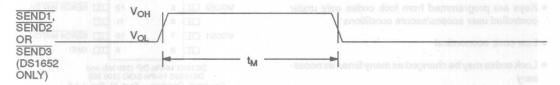
BIT 64



# LOGIC TIMING DIAGRAMS



# DS1651 LOCK, MATCH SIGNALS



When the DS1651 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	T TRIGGERED 64 CODE TRANSMITTED AS:								
SEND1	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND2	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	entry, gan	b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND3	b <sub>0</sub>	<u>b</u> 1	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND4	<u>b</u> 0	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>

### NOTES

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. Input leakage applies to DS1652 data input only.
- 4. Input/output leakage applies to the DS1651 data input/output pin.
- Input voltage on the LEARN pin is required to be in the Learn mode, for the DS1651 and DS1652 to properly accept new code data.
- 6. The DS1652 LEARN pin is internally pulled down with a  $10K\Omega$  resistor.
- 7. The DS1651  $\overline{\text{DUPL}}$  pin is internally pulled up with a 10K $\Omega$  resistor.
- 8. The DS1652 SEND1, SEND2, SEND3, and SEND4 inputs are internally pulled up with 10KΩ resistors.



# DS1653 4-Code Lock, DS1652 Key Match Memory System

#### **FEATURES**

- The two chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64—bit code or internally generated random 64—bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 4-code match conditions.
- Keys are programmed from lock codes only under controlled user access/secure conditions
- · Low cost, economical
- Lock codes may be changed as many times as necessary
- 3V operation, 5V for programming
- -25°C to +85°C operating range
- All stored 64-bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

#### PIN ASSIGNMENT

Vcc III	1	8	SEND1
SEND2	2	7	DATA I/C
LEARN III	3	6	SEND3
SEND4 III	4	5	GND

DS1652 8-Pin DIP (300 Mil) and DS1652S 8-Pin SOIC (200 Mil) See Mech. Drawings – Sect. 16, Pgs. 1 & 5



DS1653 16-Pin DIP (300 Mil) and DS1653S 16-Pin SOIC (300 Mil) See Mech. Drawings — Sect. 16, Pgs. 1 & 6

# **DS1652 PIN DESCRIPTION**

GND	- Ground
DATA I/O	- Serial Data Input/Output
SEND1	- Send Input 1
SEND2	- Send Input 2
SEND3	- Send Input 3
SEND4	- Send Input 4
LEARN	- Learn Input
Vcc	- +3V to +7V Input

### **DS1653 PIN DESCRIPTION**

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
Vcc	-	+3V to +7V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
SEND1 MATCH	-	Code Match Signal for SEND1
SEND2 MATCH	-	Code Match Signal for SEND2
SEND3 MATCH	-	Code Match Signal for SEND3
SEND4 MATCH	-	Code Match Signal for SEND4

controlling access. The code memory within the DS1653 Lock may be user programmed with a known 64 bit code, or the DS1653 can generate a 64-bit code from a random number generator within the DS1653.

#### DESCRIPTION

The DS1653 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1653 Lock and DS1652 Key contain a 64 bit memory which acts as the security code,

Once set, the code is nonvolatile, and can then be transferred to a DS1652 Key(s) under secure conditions.

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a DS1653 Lock will compare the requesting key's 64 bit code to the lock's programmed 64 bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

### **OPERATION DS1651 LOCK**

The main functional components of both the DS1653 and DS1652 are shown in Figures 1 and 2. The diagram shows that the internal functions of the lock and key are similar. From Figure 1, the primary components of the lock are its 64—bit wide registers. The 64 bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64—bit data memory records the 64—bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1653 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user provided 64 bit codes.
ecurpy c rich a loc	0	Duplicate Mode: Transmit 64-bit code memory contents.
euteur res epde la te euteut pla	propositie posositie tugai stab	Learn Mode: Program with in- ternally generated random 64 bits.

The Learn modes and duplicate mode may only be entered from operation mode. The DS1653 samples the level of MODE1 and MODE2 10 ms after a low to high transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating

In the Learn modes, the DS1653 Lock's code memory may be either programmed directly by the user, or programmed using a random set of 1's and 0's created by the DS1653's random number generator. A user must have physical access to the DS1653 to place it in Learn mode. To place the DS1653 Lock in Learn mode, the DS1653's V<sub>CC</sub> input must be at 5V minimum with, mode1 or both mode1 and mode2 pins driven high, telling the DS1653 to enable the contents of its code memory to be rewritten. If mode1 is high, then the DS1653 enables its code memory to be rewritten using a user defined 64-bit code, which it expects to see on its data I/O pin. At the end of sending the 64-bit code to the DS1653, the mode1 pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes, DS1653 Lock".) If mode2 and mode1 are high, then the DS1653 Lock performs an internal operation in which it uses its internal random number generator to create a 64-bit pattern of 1's and 0's and load it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1653 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1653 to operation mode, before entering any other mode.

The DS1653 will not reprogram its 64—bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its mode2 and mode1 pins.

For the DS1653 Lock to transfer its code memory into a DS1652 Key the DS1653 Lock must be in duplication mode. To enter the duplication mode, the mode2 pin must be driven high. The transition from 0 to 1 on the mode2 pin, and its maintenance at 1 causes the DS1653 Lock to transmit a reset signal followed by its 64-bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64 bit code copy. The data input/output pin of the DS1653 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1653 and DS1652.

The DS1653 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written in the data memory for comparison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1653 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1653 performs no operations, but waits for the next reset signal.

### **OPERATION DS1652 KEY**

The operation of the DS1652 Key is similar to that of the DS1653 (Figure 2). The key is programmed with code generated by the DS1653 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1653 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1653 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64 bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64 bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the SENDX input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to SENDX input being triggered (see diagram, page 10).

### SERIAL PULSE PROTOCOL

The DS1653 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1653 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical

one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1653 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1653 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key may be returned to its operation mode for use.

### **OPERATION, LOCK AND KEY**

The DS1653 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1653 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64 bit codes, that can only be changed by having physical access to the lock. If known codes are not required, the DS1653 can generate its own 64 bit code randomly. If the random number generator of the DS1653 Lock is used, not even the person programming the lock knows the 64 bit code.

The DS1652 Key is programmed from the DS1653 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of the DS1653 Lock is limiting the manner by which a lock may program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1653 Lock. Therefore the only method of transferal is by physically connecting the device holding the DS1652 Key with the device holding the DS1653 Lock. A quick and efficient method of implementing this interface is illustrated on page 4.

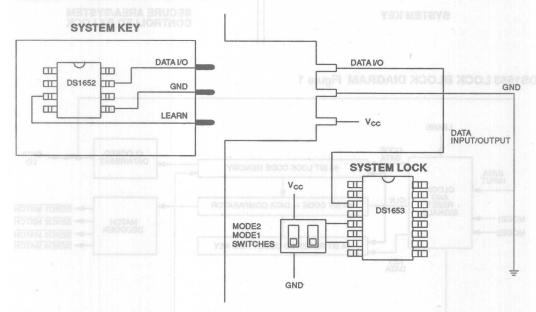
By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the Data I/O pin, the system key may accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1653 Lock could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

- 1. limits who may program keys
- 2. limits who can generate codes for the lock
- limits who may, by generating a new code, invalidate the existing programmed keys.

As many keys as needed may be programmed. As required for security purposes or in case of the loss of a key, a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.

### INTERIOR OF LOCK SECURED AREA



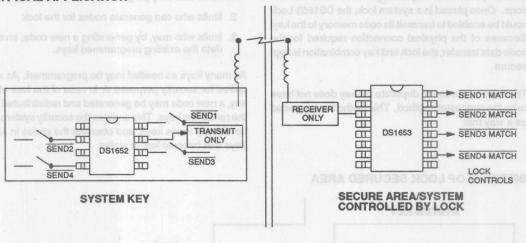
10

## TYPICAL APPLICATION

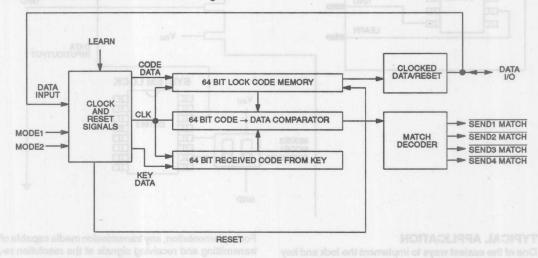
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1653's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1653 and DS1652's serial pulse protocol may be used to link the key to a lock.

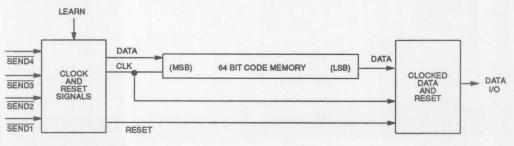
# TYPICAL APPLICATION



# **DS1653 LOCK BLOCK DIAGRAM** Figure 1



# DS1652 KEY BLOCK DIAGRAM Figure 2



# **ABSOLUTE MAXIMUM RATINGS\***

 Voltage on Any Pin Relative to -V
 -V -0.5V to +7.0V

 Operating Temperature
 -25°C to +85°C

 Programming Temperature
 -10°C to +85°C

 Storage Temperature
 -55°C to 125°C

 Soldering Temperature
 260°C for 15 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(-25°C + 85°C) DS1653 AND DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	3.0	5.0	7.0	My WO	Girl Adan
Logic 1 Input	VIH	2.0	-toV	V <sub>CC</sub> +0.3	V	1, 6, 8
Logic 0 Input	V <sub>IL</sub>	-0.3	101	+0.8	V	1, 6, 8

# DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1653

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I <sub>CC1</sub>	03.6	3	4	mA	2
Supply Current, Learn Mode	I <sub>CC2</sub>	00	3	4	mA	2
Supply Current, Idle State	I <sub>CC3</sub>	21	75	100	nA	2
Supply Current, V <sub>CC</sub> Pin, Learn Mode	I <sub>LRN</sub>	400	2	A3 AM	mA	AM FORE
Output High, Voltage	V <sub>OH</sub>	2.4			V HO	AM HIE
Output High, Current	I <sub>OH</sub>	a.r	ag/	.1	mA	atti Sampi
Output Low, Voltage	V <sub>OL</sub>	0.4	yest		Pulv Wel	otivit Signi
Output Low, Current	loL	4		TATES	mA	
I/O Leakage Current	IIO	-1		+1	μА	4

# DC ELECTRICAL CHARACTERISTICS

(-10°C to 85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	l <sub>CC1</sub>	1.0°01-	3	4	mA	2
Supply Current, Learn Mode	I <sub>CC2</sub>	0*089	3	4	mA	2
Supply Current, Idle State	I <sub>CC3</sub>	n of the des	75	100	nA	2
V <sub>CC</sub> Voltage, Learn Mode	V <sub>L</sub>	5	6 8 11	0 8/10/70 98 1	Voor	1, 5, 6, 7
Supply Current, Learn Mode	ILRN		2	3	mA	1, 5, 6, 7
Input Leakage (Data Input)	sae L1	-1 <sub>2550</sub>	памоо ы	STATISTO	μА	3
Output High, Voltage	V <sub>OH</sub>	2.4	Товина		VAR	1,9
Output High, Current	Іон	4 0.8	Vac	The same of the same	mA	dioV yiggui
Output Low, Voltage	Vol	0.4	T and		V	1, 9
Output Low, Current	loL	180	l av		mA	onle 9 Inor

# AC ELECTRICAL CHARACTERISTICS DS1653 LOCK AND DS1652 KEY

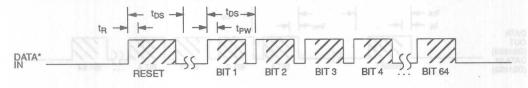
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t <sub>R</sub>	340	720	900	μs	ines Aidre
Logic 1 Active	t <sub>1</sub>	90	120	150	μs	and Ardido
Logic 0 Active	to	15	20	25	μѕ	nac Arddo
SEND1 MATCH, SEND2 MATCH, SEND3 MATCH, and SEND4 MATCH	t <sub>M</sub>	400	500	600	ms	sam Mode
Data Sample Window	t <sub>DS</sub>	1.5	2.0	2.5	ms	igiH suqtu
Active Signal Pulse Width, Data I/O	t <sub>PW</sub>	10	Vos.	1080	μѕ	woul fugtu
Active Signal Pulse Width SEND1 and SEND2	ts	100	l el		-ms	gsilseJ C
Delay Between Last Mode Pin Transition to Operation Mode Change	t <sub>T</sub>		10		ms	

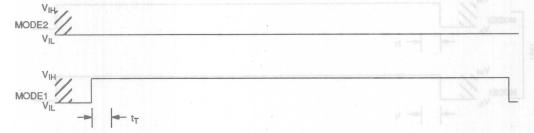
# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

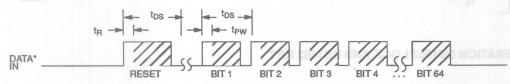
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

# LEARN MODE DS1653 LOCK; USER PROGRAMMING ON MEASURY EXCEPTION MEASURE AND ASSESSMENT AND ASSESSMENT OF THE PROGRAMMING OF MEASURE AND ASSESSMENT OF THE PROGRAMMING OF MEASURE AND ASSESSMENT OF THE PROGRAMMING OF THE PROGRA





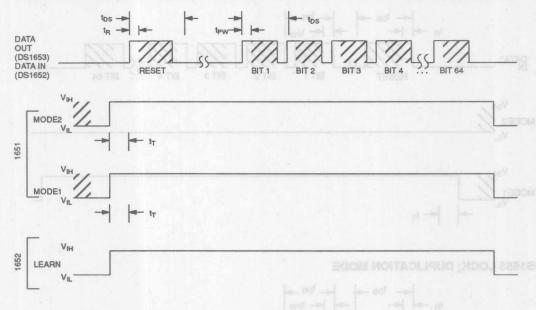
# **DS1653 LOCK; DUPLICATION MODE**



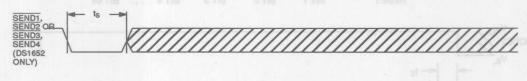


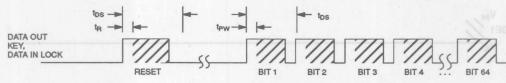
MODE1 VIL

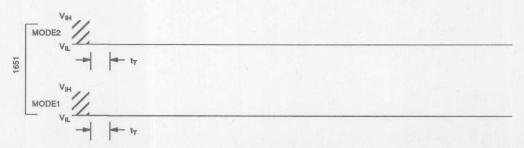
# LEARN MODE DS1652 KEY; LEARN MODE DS1653 LOCK, INTERNAL PROGRAMMING

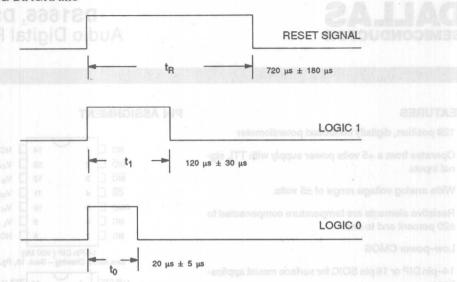


# **OPERATION DS1653 LOCK AND DS1652 KEY**

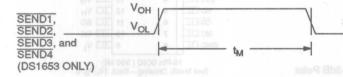








# DS1653 LOCK, MATCH SIGNALS



When the DS1653 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED			-	64 CODE	TRANSM	ITTED AS	:		
SEND1	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND2	<u>b</u> 0	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND3	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	`	b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>
SEND4	b <sub>0</sub>	b <sub>1</sub>	b <sub>2</sub> 00	b <sub>3</sub>	b <sub>4</sub>		b <sub>61</sub>	b <sub>62</sub>	b <sub>63</sub>

### NOTES

- 1. All voltages are referenced to ground.
- 2. Measured with outputs open.
- 3. Input leakage applies to DS1652 data input only.
- 4. Input/output leakage applies to the DS1653 data input/output pin.
- Input voltage on the LEARN pin is required to be in the Learn mode, for the DS1653 and DS1652 to properly accept new code data.
- 6. The DS1652 LEARN pin should be externally ties to ground when not in use.
- 7. Temperature range for programming is -10°C to +85°C.
- 8. The DS1652 SEND1, SEND2, SEND3, and SEND4 inputs are internally pulled up with 25KΩ resistors.
- 9. These output voltages are valid for a typical V<sub>CC</sub> of 5.0V ± 10%.



# DS1666, DS1666S Audio Digital Resistor

### **FEATURES**

- 128 position, digitally controlled potentiometer
- Operates from a +5 volts power supply with TTL signal inputs
- Wide analog voltage range of ±5 volts.
- Resistive elements are temperature compensated to ±20 percent end to end
- Low-power CMOS
- 14—pin DIP or 16 pin SOIC for surface mount applications
- Default position on power up sets wiper position at 10%
- Operating temperature range 0°C to 70°C

 Resolution/Step

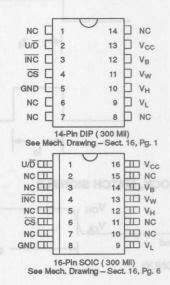
 Resistance values
 Low End
 High End
 -3dB Point

 DS1666-10
 10KΩ 24Ω 110Ω 1.1 MHz

 DS1666-50
 40KΩ 122Ω 554Ω 200 KHz

 DS1666-100
 100KΩ 243Ω 1.1KΩ 100 KHz

### **PIN ASSIGNMENT**



## **PIN DESCRIPTION**

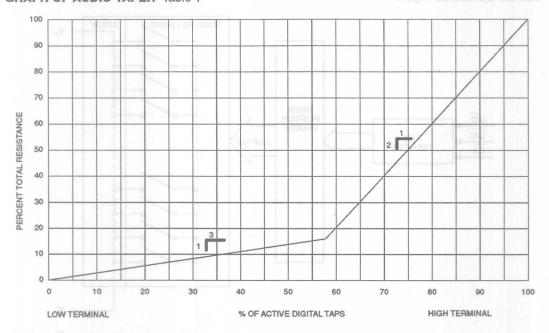
V <sub>H</sub>	nai ia c	High Terminal of Resistor
VL		Low Terminal of Resistor
V <sub>W</sub>	-	Wiper Terminal of Resistor
U/D	19	Up/Down Control
INC		Wiper Movement Control
CS		Chip Select for Wiper Movement
NC	150	No Connection
Vcc	4	+5 Volts
GND	-	Ground
VB	-	Substrate Bias -5 Volts

### DESCRIPTION

The DS1666 is a solid–state potentiometer which is set to value by digitally controlled resistive elements. The potentiometer is composed of 127 resistive sections. Between each resistive section and both ends of the potentiometer are TAP points accessible to the wiper. The position of the wiper on the resistance array is controlled by the  $\overline{CS}$ , U/ $\overline{D}$  and  $\overline{INC}$  inputs. The position of the wiper defaults to the 10% position on power up. The resolution of the DS1666 is shown in Table 1.

The DS1666 Digital Audio Resistor is uniquely designed to provide a potentiometer that is logarithmic rather than linear across its entire range. The lower half of the potentiometer advances 1% of total resistance for each 3% of scale advanced, providing for precise amplification of low volume signals. The upper half of the potentiometer advances 2% of resistance for every 1% of scale advanced, providing for the lower resolution gain required for high volume amplification.

### **GRAPH OF AUDIO TAPER** Table 1



### **OPERATION**

The CS, U/D and INC inputs control the position of the wiper along the resistor array (Figure 1). When CS is active (low), a high to low transition on the INC will increment or decrement an internal counter depending on the level of the U/D pin. When the U/D pin is low, the counter will decrement. When the U/D pin is high, the counter will increment. The state of the U/D pin can be changed while CS is active allowing for precise adjustment during calibration. The output of the counter is decoded to set the position of the wiper. When the CS input transitions to the high (inactive) level, the value of the counter is stored and the wiper position is maintained until power (V<sub>CC</sub>) is lost. When power is restored, the DS1666 returns to the default setting and positions the wiper to 10 percent. The value of the end-to-end and end-to-wiper position is indeterminate while V<sub>CC</sub> is not applied.

The DS1666 has a resistor array that resembles an audio taper potentiometer as shown in Table 1. Since the taper is not linear, exact resistance values for each of the 128 positions of the resistor is not specified. However, the end-to-end resistance is specified to be within ±20 percent of the stated resistor value over a temperature range of 0°C to 70°C.

### **ANALOG CHARACTERISTICS**

End-to-End Resistance Tolerance = ±20 percent Typical Noise = <120 dB/Hz REF:IV Temperature Coefficient = ±800 PPM/°C typical Resistance at tap #74=18% ± 2%of total resistance.

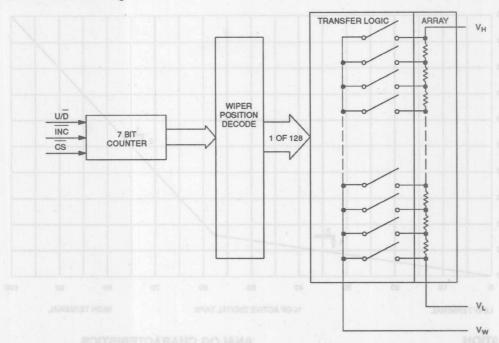
The high end of the potentiometer. This

### **PIN DESCRIPTIONS**

VH

3	terminal is capable of handling input voltages between ±5 volts.
V <sub>L</sub>	The Low end of the potentiometer. This terminal is capable of handling input voltages between $\pm 5$ volts.
V <sub>W</sub>	The wiper terminal of the potentiometer. The value of the wiper is controlled by the $U/\overline{D}$ and the $\overline{INC}$ pins.
Up/Down (U/D)	The $U/\overline{D}$ input controls the direction of the wiper movement when setting the potentiometer.
Increment (INC)	Toggling $\overline{\text{INC}}$ will move the potentiometer wiper by either incrementing or decrementing the counter.
Chip Select (CS)	The device is selected when $\overline{\text{CS}}$ input is low. The current counter value is stored when CS is returned high.

# **BLOCK DIAGRAM** Figure 1



# **MODE SELECTION** Figure 2

CS	ĪNC	U/D	MODE
L	37411918	PIM HESC	WIPER UP
era to i	~	L HV	WIPER DOWN
1	Н	X	STORE WIPER POSITION

# **ABSOLUTE MAXIMUM RATINGS\***

ADOCEO LE IMAXIMOM HATIMAS	
Voltage on CS, INC, U/D, and V <sub>CC</sub> Relative to Ground	-0.5V to +7.0V
Voltage on V <sub>H</sub> , V <sub>L</sub> , and V <sub>W</sub> Relative to Ground	-6.5V to +6.5V
Voltage on V <sub>B</sub>	-6.5V to Ground
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	+4.5	5.0	5.5	FgVre 3	ривит с
Input Logic 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5	V	1 80
Input Logic 0	V <sub>IL</sub>	-0.5		+0.8	V	- 1
V <sub>H</sub> , V <sub>L</sub> , V <sub>W</sub> Voltage	V <sub>R</sub>	V <sub>B</sub> -0.3		V <sub>CC</sub> +0.3	V	1
V <sub>B</sub> Voltage	V <sub>B</sub>	-5.5		GND	V	1

### DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to }70^{\circ}\text{C}, V_{\text{CC}} = 5.0\text{V} \pm 10\%)$ 

		Management	and the same of th		. 00	
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc		0.1	5	mA	3
Input Leakage	ILI	-1	45	+1	μА	2
Wiper Resistance	R <sub>W</sub>		350	650	Ω	- Eu
Wiper Current	I <sub>W</sub>		-1		mA	3

CAPACITANCE

 $(t_{\Delta} = 25^{\circ}C)$ 

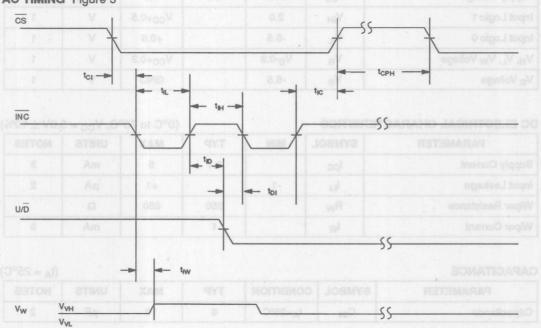
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Capacitance	CIN	t <sub>A</sub> =25°C	6	10	pF	2

### AC ELECTRICAL CHARACTERISTICS

 $(t_A = 0^{\circ}C \text{ to } 70^{\circ}C, V_{CC} = +5V \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CS to INC Setup	t <sub>Cl</sub>	100			ns	V go again
INC High to U/D Change	t <sub>ID</sub>	100			ns	meT egato
U/D to INC Setup	t <sub>DI</sub>	1			μs	B) Bremore
INC Low Period	and eget till a ed v	500	onal operatio	ly and lunct	o ens	de e ei ald
INC High Period	t <sub>IH</sub>	validaden 1	ancega and softe vem er	o anottoez i	μѕ	alcayed In I
INC Inactive to CS Inactive	t <sub>IC</sub>	500			ns	
CS Deselect Time	t <sub>CPH</sub>	100	такоо в	MTAN390	ns	ECONANE





### NOTES

- 1. All voltages are referenced to ground.
- 2. This parameter is periodically sampled and not 100% tested.
- 3. Typical values are for t<sub>A</sub> = 25°C and nominal supply voltages.
- 4. Wiper output open circuited.

### **AC TEST CONDITIONS**

Input Pulse Levels 0V to 3V Input Rise and Fall Times 10 ns Input Level 1.5V

# DS1667 Digital Resistor with OP AMP

### **FEATURES**

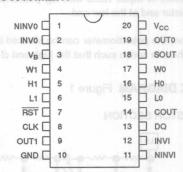
- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power up is 50%
- Resistive elements are temperature compensated to ±20% end to end
- Two high gain wide bandwidth operational amplifiers
- Low power CMOS design
- Applications include analog—to—digital and digital—to analog converters, variable oscillators, and variable gain amplifiers
- 20-pin DIP package or optional 20-pin SOIC surface mount package
- Operating temperature range of 0°C to 70°C
- Resistance Values

	NT
DS1667-10:	
DS1667-50:	
DS1667-100:	

# DESCRIPTION

The DS1667 is a dual—solid state potentiometer that is adjustable by digitally selected resistive elements. Each potentiometer is composed of 256 resistive elements. Between each resistive section of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistive array is set by an 8-bit register that controls which tap point is connected to the wiper output. Each 8-bit register can be read or written by sending or receiving data bits over a 3-wire serial port. In addition, the resistors can be stacked such that

### **PIN ASSIGNMENT**



20-Pin DIP (300 Mil) and 20-Pin SOIC See Mech. Drawings - Sect 16, Pgs.1 & 6

# PIN DESCRIPTION

Vcc	-	+5 Volt Supply
GND	-	Ground
L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W0, W1	-	Wiper End of Resistor
VB	-	Substrate Bias and OP AMF
		Negative Supply
SOUT	-	Wiper for Stacked
		Configuration
RST		Serial Port Reset Input
DQ	-	Serial Port Input/Output
CLK	-	Serial Port Clock Input
COUT	-	Cascade Serial Port Output
NINVO, NINVI	-	Noninverting OP AMP Input
INVo, INVI	-	Inverting OP AMP Input
OUT0. OUT1	_	OP AMP Outputs

a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1667 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same. The DS1667 also contains two high gain wide bandwidth operational amplifiers. Each amplifier has both the inverting and non-inverting inputs and the output available for user configuration. The operational amplifiers can be paired with the resistive ele-

ments to perform such functions as analog to digital conversion, digital to analog conversion, variable gain amplifiers, and variable oscillators.

### **OPERATION - DIGITAL RESISTOR SECTION**

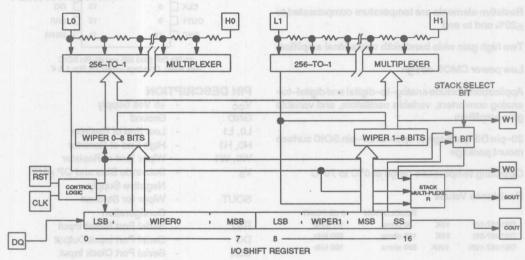
The DS1667 contains two potentiometers, each of which has its wiper set by a value contained in an 8 bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end.

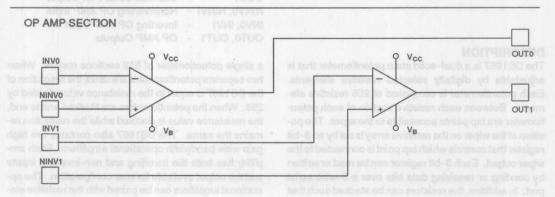
In addition, the potentiometer can be stacked by connecting them in series such that the high end of poten-

tiometer 0 is connected to the low end of potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (SOUT). A zero written to the stack multiplexer will connect wiper 0 to the SOUT pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is presented at the SOUT pin.

### **BLOCK DIAGRAM** Figure 1

### RESISTOR SECTION





Information is written to and read from the wiper 0 and wiper 1 registers and the stack select bit via the 17-bit I/O shift register. The I/O shift register is serially loaded by a 3 wire serial port consisting of RST, DQ, and CLK. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17 bit shift register only when the RST input is at a high level. While at a high level, the RST function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until RST is taken to a low level, which terminates data transfer. While RST input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O shift register while RST is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The next 8 bits to be entered are those specifying the wiper 1 setting. The MSB of these 8 bits is sent first. The next 8 bits to be entered are those specifying the wiper 0 setting, sent MSB first. The 17th bit to be entered, therefore, will be the least significant bit of the wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, sending other than 17 bits can produce indeterminate potentiometer settings.

As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port

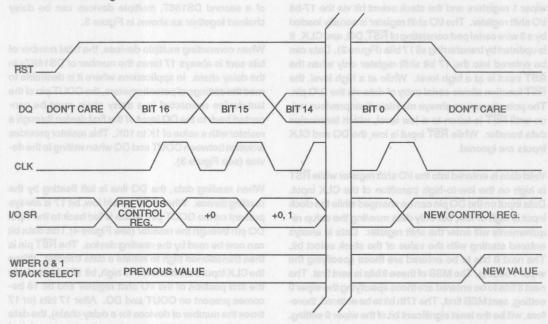
pin (COUT). By connecting the COUT pin to the DQ pin of a second DS1667, multiple devices can be daisy chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1667s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the COUT pin of the last device connected in a daisy chain must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between COUT and DQ when writing to the device (see Figure 3).

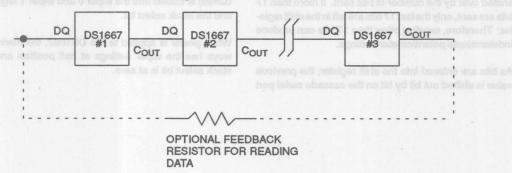
When reading data, the DQ line is left floating by the reading device. When RST is held low, bit 17 is always present on the COUT pin, which is fed back to the input DQ pin through the resistor (see Figure 4). This data bit can now be read by the reading device. The RST pin is then transitioned high to initiate a data transfer. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on COUT and DQ. After 17 bits (or 17 times the number of devices for a daisy chain), the data has shifted completely around and back to its original position. When RST is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the wiper 0 and wiper 1 registers and the stack select bit.

When power is applied to the DS1667, the device always has the wiper settings at half position and the stack select bit is at zero.

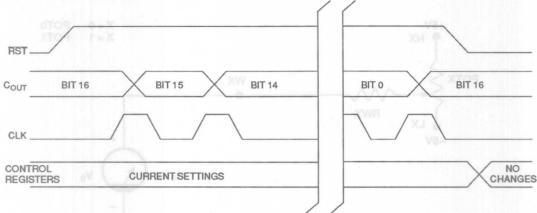
# WRITING DATA Figure 2



# **CASCADING MULTIPLE DEVICES** Figure 3



# **READING DATA** Figure 4



### **DS1667 LINEARITY MEASUREMENTS**

An important specification for the DS1667 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1667 is shown in Figure 5. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW which is typically 400 ohms. For any given setting N for the pot, the expected voltage output at SOUT is:

$$VO = -5 + [10 \times (N/256)]$$
 (in volts)

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above, and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/256 or 0.03906 volts. The equation for the absolute linearity of the DS1667 is:

$$\frac{V_{O}(\text{actual}) - V_{O}(\text{expected})}{\text{LSB}} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1667 is  $\pm$  1 LSB typical.

Relative linearity is a comparison of the difference of actual output voltages of two successive taps and the difference of the expected output voltages of two successive taps. The expected difference of output voltages is 1 LSB or 0.03906V for the measurement system of Fig-

ure 5. Relative linearity is expressed in terms of an LSB and is given by the equation:

$$\frac{\Delta V_{O}(actual) - LSB}{LSB} = RL$$

The specification for relative linerity of the DS1667 is  $\pm$  0.5 LSB typical.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (RL) versus wiper setting for a typical DS1667 at 25°C.

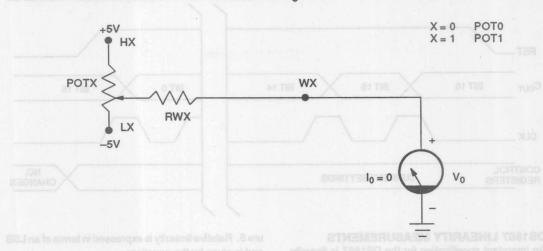
# DESCRIPTION AND OPERATION - OP AMP SECTION

The DS1667 contains two operational amplifiers which are ideal for operation from a single 5V supply and ground or from  $\pm$ 5V supplies (see Figure 1). An internal resistor divider defines the internal reference of the op amp to be halfway between the power supplies, i.e.:

$$\frac{V_{DD} + V_B}{2}$$

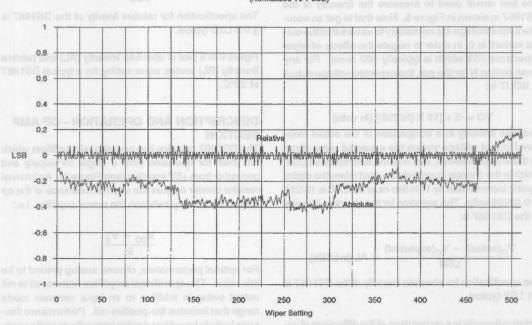
For optimal performance, choose analog ground to be this value. The operational amplifiers feature rail to rail output swing in addition to an input common mode range that includes the positive rail. Performance features include broad band noise immunity as well as voltage gain into realistic loads specified at both 600 ohms and 2K ohms. High voltage gain is produced with low input offset voltage and low offset voltage drift. Current consumption is less than 1.9 mA per amplifier and the device is virtually immune to latchup.

# **LINEARITY MEASUREMENT CONFIGURATION** Figure 5

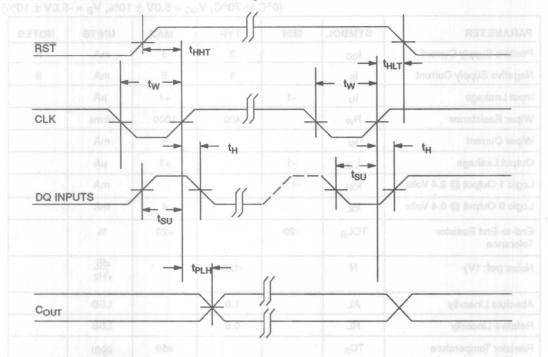


# DS1667 ABSOLUTE AND RELATIVE LINEARITY Figure 6

Absolute and Relative Linearity (Normalized To 1 LSB)



# TIMING DIAGRAM: RESISTOR SECTION Figure 7



### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground (V <sub>B</sub> = GND)	-0.5V to +7.0V
Voltage on Resistor Pins when V <sub>B</sub> = -5.5V	-5.5V to +7.0V
Voltage on V <sub>B</sub>	-5.5V to GND
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS RESISTOR SECTION

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	Vcc	+4.5	5.0	5.5	٧	1
Input Logic 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5	٧	1
Input Logic 0	V <sub>IL</sub>	-0.5	U.S. U.S.	+0.8	٧	1
Negative Supply Voltage	V <sub>B</sub>	-5.5		GND	٧	1
Resistor Inputs	L, H, W	V <sub>B</sub> - 0.5		V <sub>CC</sub> + 0.5	V	2

## DC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C,  $V_{CC}$  = 5.0V  $\pm$  10%,  $V_{B}$  = -5.0V  $\pm$  10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Current	Icc		3 74	5	mA	8
Negative Supply Current	IB		3	5	mA	8
Input Leakage	lu	-1	Y	+1	μА	
Wiper Resistance	Rw	4	400	1000	ohms	OUK
Wiper Current	lw			1	mA	
Output Leakage	ILO	-1		+1	μА	
Logic 1 Output @ 2.4 Volts	Гон	-1.0	W -		mA	
Logic 0 Output @ 0.4 Volts	loL		HE	4	mA	Mill Mexic
End-to-End Resistor Tolerance	TOLR	-20		+20	%	
Noise (ref: 1V)	N	1)	-120	-	d <u>B</u> √Hz	
Absolute Linearity	AL		1.0		LSB	Ceur
Relative Linearity	RL		0.5		LSB	
Resistor Temperature Coefficient	TCR			850	ppm °C	Frusoe

## CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

	AND THE PERSON NAMED IN COLUMN 1			177		
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN	iol O°08s		5	pF	dering Ted
Output Capacitance	C <sub>OUT</sub>	of the devic	al operation	rollony bas	pF	onte a el eld

 PARAMETER
 SYMBOL
 RBM
 TYP
 MAX
 UNITS
 NOTES

 PARAMETER
 SYMBOL
 RBM
 TYP
 MAX
 UNITS
 NOTES

 Positive Supply Voltage
 V<sub>CO</sub>
 +4.5
 6.0
 5.6
 V
 1

 Input Logic 1
 V<sub>IR</sub>
 2.0
 V<sub>CC</sub>+0.5
 V
 1

 Input Logic 0
 V<sub>IL</sub>
 +0.5
 +0.8
 V
 1

 Negative Supply Voltage
 V<sub>B</sub>
 -5.5
 GND
 V
 1

 Resistor Inputs
 L, H, W
 V<sub>B</sub> - 0.5
 V<sub>CC</sub> + 0.6
 V
 2

## AC ELECTRICAL CHARACTERISTICS RESISTOR SECTION (0°C to 70°C, $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX		UNITS	NOTES
CLK Frequency	f <sub>CLK</sub>	SAA	NSW 3	10		MHz	STEMAR!
Width of CLK Pulse	t <sub>W</sub>	50	7.0	187 L		ns	- 648H WS
Data Setup Time	t <sub>SU</sub>	30		1839		ns	WANISH ME
Data Hold Time	t <sub>H</sub>	10		MH		ns	Brogu este
Propagation Delay Time Low to High Level Clock to Output	t <sub>PLH</sub>	081		50		ns notaleel	3
RST High to Clock Input High	tннт	50		TVAL	eel	ns V	meter tuc
RST Low from Clock Input High	t <sub>HLT</sub>	50		VF(r	esi	ns	nut Refern

### OPERATIONAL AMPLIFIER SECTION DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}\text{C to } 70^{\circ}\text{C V}_{CC} = 5.0\text{V} \pm 10\%, \text{V}_{B} = -5.0\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage	Vos		5	10	mV	AN I DIN DUNESUN
Input Offset Voltage Drift	V <sub>OSD</sub>		10	1287-1771	uV/°C	O ORO . O I have i
Common Mode Rejection	CMR	SATE N. AND SERVICES	62	ar an isalan	dB	AV AVOIDADA
Positive Power Supply Rejection	+PS <sub>R</sub>	V0.8-= <sub>8</sub> V	62	gV ,eonam	dB	go leed average of
Negative Power Supply Rejection	-PS <sub>R</sub>		62		dB	4
Input Common Mode Voltage Range	C <sub>CCM</sub>	V <sub>B</sub> +1.5V		V <sub>CC</sub>	٧	OF AMPS SIBLES
Large Signal Voltage Gain		and the same of	106	8	dB	$R_L = 2K\Omega$
Large Signal Voltage Gain		9	96		dB	$R_L = 600K\Omega$
Output Swing	V <sub>SWGH</sub>	4.6	4.7		٧	$R_L = 2K\Omega \text{ toGND}$
Output Swing	V <sub>SWGL</sub>	1 5	-4.7	-4.6	٧	$V_B = -5V$
Output Swing	V <sub>SWGH</sub>	4.5	4.6		V	$R_L = 600\Omega \text{ toGND}$
Output Swing	V <sub>SWGL</sub>		-4.6	-4.5	٧	$V_B = -5V$
Output Current	Vo, SOURCE	13	58	Ω 088	mA	V <sub>O</sub> = 0 Volts
Output Current	V <sub>O, SINK</sub>	13	63	2	mA	V <sub>O</sub> = +5 Volts

### OPERATIONAL AMPLIFIER SECTION AC ELECTRICAL CHARACTERISTICS

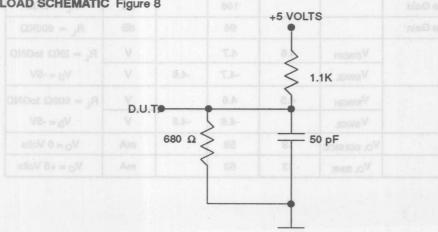
 $(0^{\circ}\text{C to }70^{\circ}\text{C V}_{CC} = 5.0\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	V <sub>SL</sub>	0.7	2	ALTO LA	V/µs	6
Gain Bandwidth Product	GBP		2.5		MHz	5
Phase Margin	PM		75		deg	5
Gain Margin	GM		20		dB	5
Amp to Amp Isolation	AAI		130	11.0	dB	o High Level Clock to
Input Referred Voltage Noise	IRVF		100	THIN	nV/√Hz	F=1 KHz
Input Referred Current Noise	IRVI		.0002	Tarl	pA/ √Hz	F=1 KHz
Total Harmonic Distortion	HD		0.1		%	$F = 10 \text{ kHz AV} = -10 \text{ RL} = 2K\Omega \text{ V}_{O} = 1\text{V}_{PP}$

### **NOTES**

- 1. All voltages are referenced to ground.
- 2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction
- 3. Measured with a load as shown in Figure 8.
- 4. Over a frequency range of 0 1 KHz.
- 5. Load is  $R_L = 600 \Omega$   $C_L = 10 pF$
- 6.  $V_{DD} = +5.0 \text{V}$   $V_{B} = -5.0 \text{V}$  connected as voltage follower with 10V step input and  $R_{L} = \infty$ .
- 7. To achieve best op amp performance, V<sub>DD</sub> = +5.0V V<sub>B</sub> = -5.0V and analog ground = 0V. In general analog ground =  $\frac{V_{DD} + V_{B}}{2}$ .
- 8. OP AMPS idle, no load.

### **LOAD SCHEMATIC** Figure 8



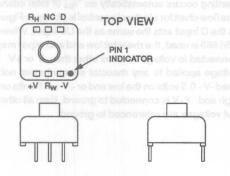


## DS1668, DS1669, DS1669S Dallastat<sup>TM</sup> Electronic Digital Rheostat

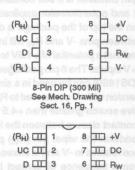
### **FEATURES**

- Replaces mechanical variable resistors
- Available as the DS1668 with manual interface or the DS1669 integrated circuit
- Human engineered interface provides easy control with DS1668
- Electronic interface provided for digital as well as manual control
- Wide differential input voltage range between 4.5 and 8 volts
- · Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8 pin SOIC and 8 pin DIP packages for DS1669
- Standard resistance values for Dallastat
  - DS1668/DS1669-10 ~ 10KΩ
  - DS1668/DS1669–50 ~ 50KΩ
  - DS1668/DS1669-100 ~ 100KΩ

### **PIN ASSIGNMENT DS1668**



### **PIN ASSIGNMENT DS1669**



(RL) 4 5 V-8-Pin SOIC (200 Mil) See Mech. Drawing Sect. 16, Pg. 5

### **PIN DESCRIPTION DS1669**

RH	- Resistor High End (Option)	
Rw	- Resistor Wiper	
RL	- Resistor Low End	
-V, +V	- Voltage Inputs	
UC	- Up Contact Input	
D	- Digital Input	
DC	- Down Contact Input	
NC	- No Connect	

### **PIN DESCRIPTION DS1668**

+V	- Positive Voltage Input
-V	- Negative Voltage
Rw	- Resistor Wiper
DIB V-br	- Digital Input
RH	- Resistor High End
NC	- No Connection - Pin Missing

### DESCRIPTION

The Dallastat is a digital rheostat or potentiometer which is adjusted to a desired value by a contact closure input. Alternatively, the desired setting can be achieved from a digital source input. When supplied as a 6 pin device, the contact closure is provided on the top of the package. In this configuration (DS1668), -V is connected to R<sub>I</sub> on the bottom side of the package, and R<sub>W</sub>, +V, D and RH are single connections on the bottom side of the package. The 6 pin Dallastat is a self contained substitute for rheostat and potentiometer applications. Any time the button on the top of the package is depressed the resistance between pins -V and Rw will increase or decrease provided that a potential of +4.5V to +8V exist between -V and +V inputs. The 8 pin packaged versions of the Dallastat (DS1669) can be used in a similar manner as the 6 pin version with -V connected to R1:+V connected to a positive source greater than +4.5 volts relative to -V, and a contact closure between the inputs and -V. Under this condition the wiper pin (Rw) provides a variable resistance relative to -V and is increased or decreased based on a sequence of contact inputs between UC, DC, or D, and -V.

Both the DS1668 and DS1669 can also be controlled by a digital input which functions in parallel with a contact closure or instead of contact closure. In addition, the DS1669 can be configured with and up/down two button arrangement.

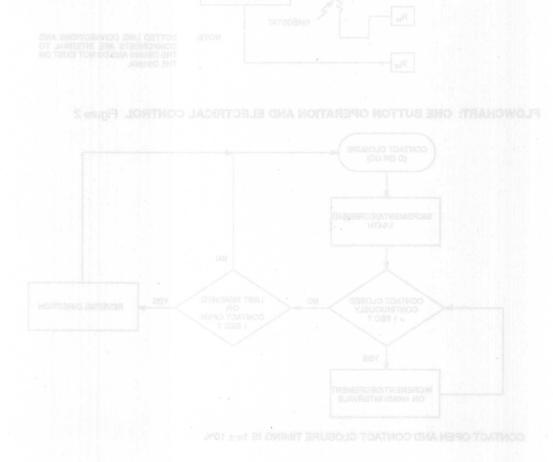
### **OPERATION**

The main elements of the Dallastat are shown in the block diagram of Figure 1. The diagram shows that the rheostat or variable resistor setting is determined by the value of a 64 to 1 muxer which is controlled by the input interpreter. The input interpreter takes a UC, DC, or D input, and sends control information to the multiplexer. The way the interpreter derives the control information is key to the operation of the Dallastat. The dotted lines shown in the block diagram are included in the DS1668 device and serve as a typical application example for the use of the DS1669 DIP and SOIC devices. As shown, a pushbutton contact is between UC and -V and pulls the input of an "OR" gate to the negative supply. Note that "D" assumes a logic high level when not connected. When the input of the OR gate is first connected low, the interpreter sends a pulse to the multiplexer which will either increment or decrement the rheostat wiper position 1/64 of the total taper (see flow diagram

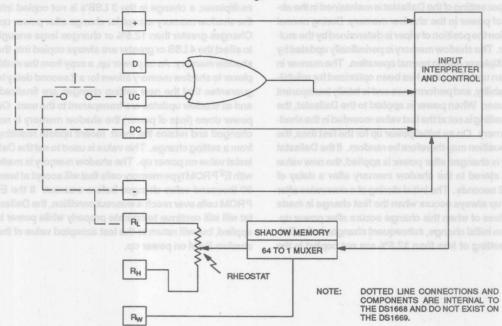
Figure 2 and 3). Increment or decrement determination is based on prior activity. A single input from contact closure of a duration of greater than 1 ms is sufficient to cause a wiper position change of 1/64 of total. Subsequent inputs will increment or decrement 1/64 of total for each additional contact closure. However, if the contact input remains active for greater than 1 second, increments/decrements of 1/64 of total occur at intervals of 100 ms for as long as the input is active or until the top or bottom of the rheostat taper is reached. Anytime that input activity stops for a period of time greater than 1 second, the next action taken as a result of subsequent input activity will be reversed; i.e., if the Dallastat was incrementing, it will decrement, and if decrement was the prior action, the next action taken will be increment. If input activity is maintained for a period of time such that the upper or lower limits of the rheostat are reached, successive action is in the opposite direction. Total time of movement from one end of the taper to the other requires 64 X 100 ms + 1 second or 7.4 seconds. The DS1669 version of the Dallastat can be configured for two button operation such that the DC input can be used for decrementing and the UC input is then used only for incrementing. Upon power up, the device will internally sense the impedance between the DC input and V+. For this reason, the DC input must be connected to +V when not in use. Otherwise, the DS1669 version of the Dallastat performs as described above with the contact input attached external to the device package. Connection between contact inputs and -V of less than 10K is all that is required to be interpreted as activity. Alternatively, the D input accepts a low going signal of 0.8 volts maximum with respect to -V. The input pulse width must exceed 1 us to guarantee recognition. Successive input pulses can be any length apart provided they are not separated by more than 1 second. As with manual inputs, increment/decrement action reverses if input activity stops for a period of time greater than 1 second. If the D input is held low for more than 1 second, incrementing/decrementing occurs automatically on 1/64 of total intervals. The flow chart for electronic control is shown in Figure 2, as the D input acts the same as the UC input. When the DS1669 is used, the rheostat low end and wiper may be connected to voltage sources other than -V or +V. The voltage applied to any rheostat element must not exceed -V - 0.5 volts on the low end or +V + 0.5 volts on the high end. If -V is connected to ground, then all other input voltages are referenced to ground.

### NONVOLATILE WIPER SETTINGS

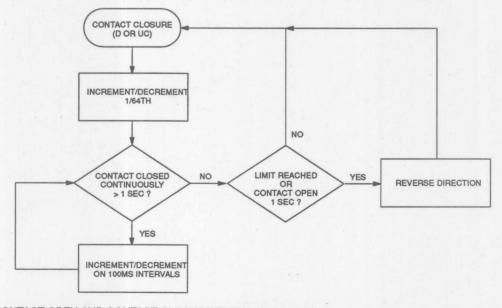
The wiper setting of the Dallastat is maintained in the absence of power in the shadow memory. During normal operation the position of wiper is determined by the multiplexer. The shadow memory is periodically updated by the multiplexer during normal operation. The manner in which an update occurs has been optimized for reliability, durability, and performance and is totally transparent to the user. When power is applied to the Dallastat, the wiper setting is set at the last value recorded in the shadow memory. On an initial power up for the first time, the wiper position may therefore be random. If the Dallastat setting is changed after power is applied, the new value will be stored in the shadow memory after a delay of about 2 seconds. The initial storing of a new value after power up always occurs when the first change is made regardless of when this change occurs after power up. After the initial change, subsequent changes in the Dallastat setting of less than 12.5% are not copied in the shadow memory. Since the Dallastat contains a 64 to 1 multiplexer, a change in the 3 LSB's is not copied into the shadow memory except for change after power up. Changes greater than 12.5% or changes large enough to affect the 4 LSB or greater are always copied into the shadow memory. As on power up, a copy from the multiplexer to shadow memory allows for a 2 second delay to guarantee that the new setting changes are finalized, and all shadow updates are transparent to the user. On power down (loss of power) the shadow memory is not changed and retains the most recent update resulting from a setting change. This value is used to set the Dallastat value on power up. The shadow memory is made with E2 PROM type memory cells that will accept at least 80 thousand value changes before wearout. If the E2 PROM cells ever reach a wearout condition, the Dallastat will still continue to operate properly while power is applied, but will return to the last accepted value of the shadow RAM on power up.



### DS1668 DALLASTATTM BLOCK DIAGRAM Figure 1

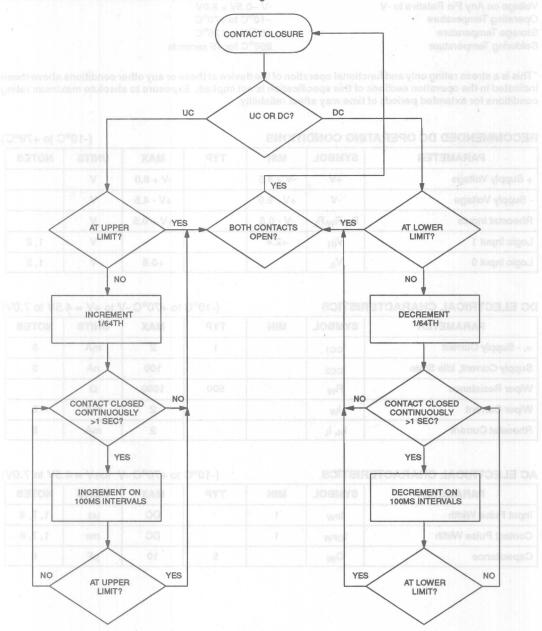


### FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 2



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1s ± 10%

### FLOWCHART: TWO BUTTON OPERATION Figure 3



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 sec. ± 10%

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to -V
Operating Temperature
Storage Temperature
Soldering Temperature

-V -0.5V + 8.0V -10°C to +70°C -55°C to 125°C 260°C for 15 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(-10°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 4.5		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 4.5	V	
Rheostat Inputs	R <sub>H</sub> ,R <sub>W</sub> ,R <sub>L</sub>	-V - 0.5	108	+V + 0.5	V	
Logic Input 1	ViH	+2.4		1	V	1,2
Logic Input 0	V <sub>IL</sub>			+0.8	V	1,2

### DC ELECTRICAL CHARACTERISTICS

 $(-10^{\circ}\text{C to } +70^{\circ}\text{C} - \text{V to } + \text{V} = 4.5\text{V to } 7.0\text{V})$ 

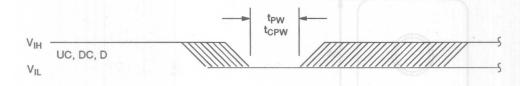
DO EFFORMATIONE SHALLAS	1211101100		(100	101100		.0 0 00 110
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I <sub>CC1</sub>		1	2	mA	3
Supply Current, Idle State	I <sub>CC2</sub>			100	nA	9
Wiper Resistance	R <sub>W</sub>		500	1000	Ω	
Wiper Current	lw			2	mA	5
Rheostat Current	I <sub>H</sub> , I <sub>L</sub>			2	mA	5

### **AC ELECTRICAL CHARACTERISTICS**

 $(-10^{\circ}\text{C to } +70^{\circ}\text{C} - \text{V to+V} = 4.5\text{V to } 7.0\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	tpW	1		DC	μs	1, 7, 8
Contact Pulse Width	t <sub>CPW</sub>	. 1		DC	ms	1, 7, 8
Capacitance	CIN		5	10	pF	6

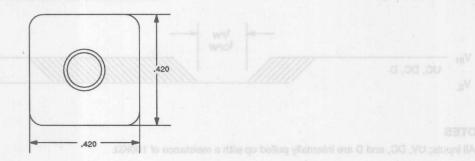
### **TIMING DIAGRAM**

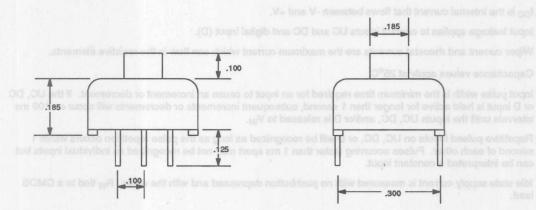


### NOTES

- 1. All inputs; UV, DC, and D are internally pulled up with a resistance of 100KΩ.
- 2. Input logic levels are referenced to -V.
- 3. I<sub>CC</sub> is the internal current that flows between -V and +V.
- 4. Input leakage applies to contact inputs UC and DC and digital input (D).
- 5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
- 6. Capacitance values apply at 25°C.
- 7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V<sub>IH</sub>.
- Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1
  second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but
  can be interpreted a constant input.
- Idle state supply current is measured with no pushbutton depressed and with the wiper. R<sub>W</sub> tied to a CMOS load.

### **DS1668 PUSHBUTTON DIMENSIONS**





TH

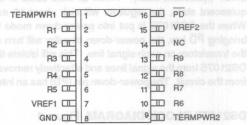
## DALLAS

## DS2107S SCSI Terminator

### **FEATURES**

- Fully compliant with SCSI and SCSI-2 standards
- Provides active termination for 9 signal lines
- Laser-trimmed 110 ohm termination resistors have 1% tolerance
- Low dropout voltage
- 16-pin plastic SOIC package
- Power-down mode isolates termination resistors from the bus

### **PIN ASSIGNMENT**



16-Pin SOIC (300 mil) See Mech. Drawing - Sect. 16, Pg. 6

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### DESCRIPTION MAD ON

The SCSI-2 standard recommends the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS2107S SCSI Terminator, which is fully compliant with the standard, enables the designer to gain the benefits of active termination: greater immunity to volt-

age drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS2107S integrates a regulator and nine precise switched 110 ohm termination resistors into a monolithic IC.

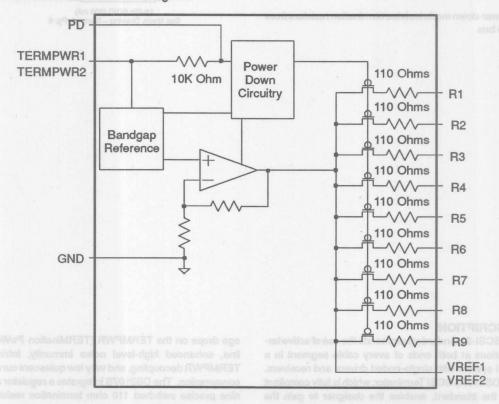
### **FUNCTIONAL DESCRIPTION**

The DS2107S consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level which is fed to a buffer amplifier. The buffer produce s a 2.85V level and is capable of sourcing 24 mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator will pull the signal line to 2.85V (quiescent state). When all lines settle in the quiescent state, the regulator will sink about 10 mA. When the DS2107S is put into power-down mode by bringing PD low, the power-down circuitry will turn off the transistors on each signal line. This will isolate the DS2107S from the signal lines and effectively remove it from the circuit. The power-down pin (PD) has an inter-

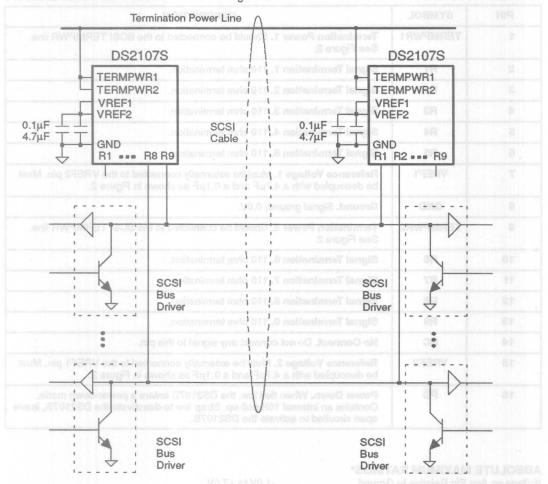
nal 10K ohm pull-up resistor. To place the DS2107S into an active state, the  $\overline{PD}$  pin should be left open circuited.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS2107S requires parallel 0.1  $\mu\text{F}$  and 4. 7  $\mu\text{F}$  capacitors connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit wide SCSI bus arrangement ("A" Cable), two DS2107S's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In a 16-bit wide SCSI bus arrangement ("P" Cable), three DS2107S's would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

### **DS2107S BLOCK DIAGRAM** Figure 1



### **TYPICAL SCSI BUS CONFIGURATION** Figure 2



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020792 3/5

### **PIN DESCRIPTION** Table 1

PIN	SYMBOL	DESCRIPTION
1	TERMPWR1	Termination Power 1. Should be connected to the SCSI TERMPWR line. See Figure 2.
2	R1	Signal Termination 1. 110 ohm termination.
3	R2	Signal Termination 2. 110 ohm termination.
4	R3	Signal Termination 3. 110 ohm termination.
5	R4	Signal Termination 4. 110 ohm termination.
6	R5	Signal Termination 5. 110 ohm termination.
7	VREF1	Reference Voltage 1. Must be externally connected to the VREF2 pin. Must be decoupled with a $4.7\mu F$ and a $0.1\mu F$ as shown in Figure 2.
8	GND	Ground. Signal ground; 0.0V.
9	TERMPWR2	<b>Termination Power 2.</b> Should be connected to the SCSI TERMPWR line. See Figure 2.
10	R6	Signal Termination 6. 110 ohm termination.
11	R7	Signal Termination 7. 110 ohm termination.
12	R8	Signal Termination 8. 110 ohm termination.
13	R9	Signal Termination 9. 110 ohm termination.
14	NC	No Connect. Do not connect any signal to this pin.
15	VREF2	Reference Voltage 2. Must be externally connected to the VREF1 pin. Must be decoupled with a $4.7\mu F$ and a $0.1\mu F$ as shown in Figure 2.
16	PD	Power Down. When tied low, the DS2107S enters a power-down mode. Contains an internal 10K pull-up. Strap low to deactivate the DS2107S, leave open circuited to activate the DS2107S.

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -1.0V to +7.0V 0°C to +70°C -55°C to 125°C 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V <sub>TP</sub>	4.00		5.25	V	
PD Active	V <sub>PDA</sub>	-0.3		0.8	٧	
PD Inactive	V <sub>PDI</sub>	2.0		V <sub>TP</sub> +0.3	V	

### DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I <sub>TP</sub>	greben		245 15	mA mA	1,3 1,4
Power Down Current	I <sub>PD</sub>			750	μА	1,2,5
Termination Resistance	R <sub>TERM</sub>	108	110	112	ohms	1,2

### **REGULATOR CHARACTERISTICS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V <sub>REF</sub>	2.79	2.85	2.91	V	1,2
Drop Out Voltage	V <sub>DROP</sub>		0.8	1.0	V	1.3
Line Regulation	LI <sub>REG</sub>		0.1	0.25	%	1,4
Load Regulation	LO <sub>REG</sub>		1	2	%	1,2

### NOTES

- 1. 4.00V < TERMPWR < 5.25V.
- 2. 0.0V < signal lines < 3.0V.
- 3. All signal lines = 0.0V.
- 4. All signal lines open.
- 5.  $\overline{PD} = 0.0V$ .

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

Intelligent Sockets

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

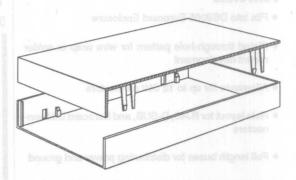
**Packages** 



## DS9005 Eurocard Enclosure

### **FEATURES**

- Low-cost molded enclosure
- Two-piece, snap together construction
- Made of rugged, flame-retardant polyester PBT plastic
- Accepts DS9006 SIP Stik Motherboard or any other single size Eurocard printed circuit board
- Can be custom machined to allow for connector requirements
- Component clearance of .230" solder side, 1.000" circuit side using .062" board
- Smooth indents on bottom side for rubber bumpers
- Hole knockouts for mounting



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See Mech. Drawing - Sect. 16, Pg. 21

### DESCRIPTION

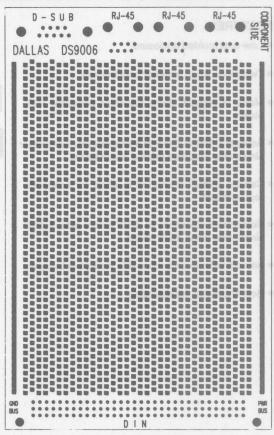
The DS9005 Eurocard Enclosure is a rugged, twopiece snap together plastic enclosure for any standalone system application. The PCB is offset in the enclosure to allow for components such as transformers and SIP Stiks to be positioned on the topside of the board while still leaving room for standard IC packages and discretes on the bottom side of the board. The housing is constructed of flame-retardant polyester PBT plastic to allow for applications requiring a very wide range of temperatures and is highly resistant to most chemicals. The size of the board and location of I/O connectors should match the DS9006 SIP Stik Motherboard. Applications include control units, handheld remote communications, and security systems.



## DS9006 SIP Stik Motherboard

### **FEATURES**

- Fits into DS9005 Eurocard Enclosure
- Plated through-hole pattern for wire wrap or solder mount development
- Allowance for up to 12 Stik connectors
- Hole layout for RJ45, D-SUB, and Eurocard DIN connectors
- Full length buses for distributing power and ground
- 1700 hole array for 0.1" center ICs and Stiks



See Mech. Drawing - Sect. 16, Pg. 22

### **DESCRIPTION**

The DS9006 SIP Stik Motherboard is a developmental printed circuit board for prototyping circuit designs which utilize Stik prefabs and/or RJ11/45 connector schemes. Many SIP Stiks mate with connectors that have staggered rows of pins. This makes it difficult to prototype these modules since most off-the-shelf wire wrap boards have a grid of 0.1" center holes. The DS9006 contains several rows of holes that are offset to accommodate both SIP Stiks and standard 300 mil and 600 mil DIPs.

Hole patterns for three RJ11/45, one 9-pin D-SUB, and 64/96-pin Eurocard connectors are located on the ends of the PCB in a right angle fashion to enable the finished circuit board assembly to mount in the DS9005 enclosure. This allows the designer to have a "complete" looking unit for presentation while still in the prototyping stage of design.

## **DALLAS**SEMICONDUCTOR

## DS9006K SIP Stik Prototyping Kit

### **FEATURES**

- DS9005 Eurocard Enclosure
- DS9006 SIP Stik Motherboard
- Sample connectors for 30-, 35-, and 40-contact SIP Stiks
- Adaptor pins for wire wrap
- Application note

### 3-D PACKAGING BOOSTS DENSITY

SipStik
Prefabs
DSxxxx
SipStik
Connectors
DS9071
SipStik
Motherboard
DS9006
Enclosure
DS9005

Eurocard Form Factor Shown. Stiks, RJ45, D—Sub, and DIN not included.

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### DESCRIPTION

The DS9006K SIP Stik Prototyping Kit includes a printed circuit board for prototyping SIP Stiks. The wire—wrapped unit can then be housed in a molded enclosure for standalone applications. An application note

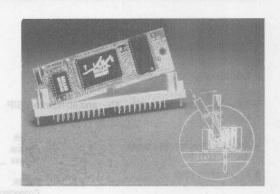
explains how to maximize use of the D\$9006 SIP Stik Motherboard printed circuit board using SIP Stiks. See data sheets for the D\$9005 Eurocard Enclosure and D\$9006 for more information on these items.



## DS907x SIP Stik Connectors

### **FEATURES**

- Provides snap-in connection between SIP Stiks and motherboard
- Provides 200 grams minimum contact force on JE-DEC standard modules
- Redundant contacts
- Low insertion force
- Heat-resistant housing (rated at 200°C)
- .050" and .100" centerlines as specified in table below
- Reference AMP Inc. MICROEDGE<sup>TM</sup> SIMM connector catalog for more detailed specifications.



Part Number DS9071-30V	Description 30 contact vertical position	Ref. AMP Part # 821828-2	Length (in.) 3.800
DS9071-30I	.100" pitch 30 contact inclined position .100" pitch	821876–2	3.800
DS9071-35V	35 contact vertical position .100" pitch	821828–3	4.300
DS9071-35I	35 contact inclined position .100" pitch	821876–3	4.300
DS9071H-35R	35 contact high profile right angle position .100" pitch	3-382488-5	4.300
DS9072-40V	40 contact vertical position .050" pitch	821918–2	2.950
DS9072H-40R	40 contact high profile right angle position .050" pitch	4-382486-0	2.950
DS9072L-40R	40 contact low profile right angle position .050" pitch	4-382480-0	2.950
DS9072-68V	68 contact vertical position .050" pitch	821-824-7	4.350
DS9072-68I	68 contact inclined position .050" pitch	8219076	4.350
DS9072H-68R	68 contact high profile right angle position .050" pitch 68 contact low profile right	6-382486-8	4.350
DS9072L-68R	68 contact low profile right angle position .050" pitch	6-382480-8	4.350
DS9072-72V	72 contact vertical position .050" pitch	821824–8	4.550
DS9072-72I	72 contact inclined position .050" pitch	821907–7	4.550
DS9072H-72R	72 contact high profile right	7–382486–2	4.550
DS9072L-72R	angle position .050" pitch 72 contact low profile right angle position .050" pitch	7–382480–2	4.550

Also available are 40-position DIP-to-SIP and SIP-to-DIP adaptors for development of DS2250 Micro Stik products.

**Part Number** 

Description

DS9075

SIP-to-DIP Adaptor 40 contact, horizontal DIP plug with 40 contact, low profile vertical position,

.050 pitch SIMM connector DIP-to-SIP Adaptor

DS9076

40 contact, .050 pitch, vertical SIMM edge card with 40 contact, vertical DIP

socket.

Also available are 40-position DIP-to-SIP and SIP-to-DIP adapters for development of DS2250 Micro Stift

Part Mumber Oseors

aragan

Description SIP (6-DIP Adaptor

050 pixoh SilviM connector

3IP-to-SIP Adaptor 10 contact, .050 pitch, vertical SIMM edge card with 40 contact, vertical DIP codyst. **General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

## **Automatic Identification**

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

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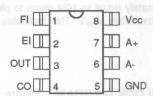


## DS1203S-B1 MicroPower Receiver Chip

### **FEATURES**

- Input channel continuously listens for input signals up to 250 KHz
- Ultra low-power listening gives longevity to the 3-volt supply
- 25 mV P-P input signal drives output to supply levels
- Electronic freshness seal eliminates power consumption during storage
- Applications include RF, IR, or magnetic front end for wireless devices
- · Space-saving; small outline surface mount package

### PIN CONNECTIONS



8-PIN SOIC (150 MIL)

See Mechanical Drawing Section 16, pg. 5

### **PIN NAMES**

EI

Vcc - 3-volt Supply

GND - Ground

FI - Freshness Input

- Enable Input

OUT - Signal Output

CO - Cycle Output

A+ - Non-inverting Input

A- Inverting Input

### DESCRIPTION

The DS1203S-B1 MicroPower Receiver Chip is an ultra low-power comparator circuit designed to listen for signals of up to 250 KHz. Input signals as small as 25 mV peak-to-peak are presented at the output as full power supply level signals. The DS1203S-B1 makes an ideal front end for wireless communication links via RF, IR, ultrasound or magnetic field. The ultra low power feature

allows remote applications to be permanently powered by a single three-volt lithium energy source capable of lasting over ten years. A freshness seal can disconnect the power supply so that energy loss is avoided during periods of storage. The freshness seal is activated or deactivated through the use of a pulse packet protocol and the Freshness Input pin.

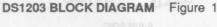
### **OPERATION**

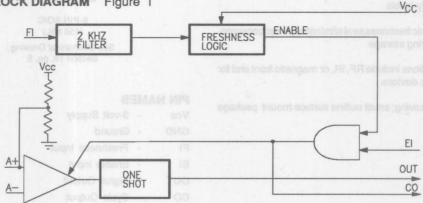
A block diagram of the DS1203S-B1 MicroPower Receiver Chip is shown in Figure 1. The device consists of a comparator which can be enabled by two sources. The enable input (EI) can be used to turn on the comparator directly, provided the freshness seal has been enabled. When the comparator is enabled, signals present at inputs A+ and A- of a magnitude greater than 25 mV peak-to-peak produce voltage swings between power supply input and ground at the output. In addition, the A+ input has a bias resistor of R<sub>approximately equal to 10M ohms to place the A+</sub> pin at approximately Vpp/2. This facilitates differential reception.

### FRESHNESS SEAL

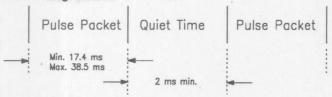
The freshness seal input pin (FI) is used to either stop or start DS1203S-B1 power consumption. This input accepts a pulse packet which is comprised of a series of pulses, representing either a logic 0 or a logic 1. separated by a 2-millisecond quiet time. Each pulse packet has a minimum aperture time of 17.4 milliseconds and a maximum aperture time of 38.5 milliseconds (see Figure 2). When the seal is broken, the comparator continuously listens for activity at the inputs. When the seal is intact, no listening occurs and the DS1203S-B1 enters a no-power consumption mode.

Within this aperture time, a logic 0 is represented as 32 to 47 pulses. A logic 1 is represented as 48 to 63 pulses. The type of pulse packet command, either a seal or a break, is illustrated in Figure 3.

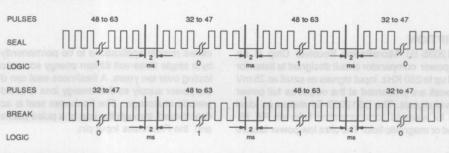




FRESHNESS SEAL Figure 2



### **SEAL AND BREAK COMMAND** Figure 3



012892 2/3

## 10

### **ABSOLUTE MAXIMUM RATINGS'**

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature 0.5V to +7V 0°C to 70°C -55°C to +125°C 260°C for 10 sec.

Soldering Temperature 260°C for 10 sec.

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>cc</sub>	2.5	3.0	5.5	Volts	sa e <b>1</b> i niritiy
Input Logic 1	V <sub>IH</sub> D IST	2.0	es llan	V <sub>cc</sub> +0.3	Volts	1, 2
Input Logic 0	V <sub>ILE</sub> THE BUCK WITH	-0.3	of qu	0.8	Volts	1, 2
Input Sensitivity	V <sub>SIN</sub> T OVA	25	20		mVolts	AMP WES
FI Input Logic 1	V <sub>IHF</sub>	2.0	brus qu	V <sub>cc</sub> +0.3	Volts	161400-810
FI Input Logic 0	V <sub>ILF</sub>	-0.3		0.4	Volts	1

### DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V<sub>cc</sub>=2.5 to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	Battery Ippul	-1.0	brue abdean	1.0	μА	mia Ismoini
Output Logic 1	V <sub>OH</sub>	V <sub>cc</sub> -0.3	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	KIND DIESE DE	Volts	1
Output Logic 0	V <sub>OL</sub>	LIONIII	SERVICE DE SER	0.4	Volts	1
Operating Current	I <sub>cc</sub> (Unit)	GND	aluqui tohus	3	μА	5
Power Down Current	I <sub>CC1</sub>	IPIT		50	μА	3
Output Current Logic 1	I <sub>OH</sub>	BUOU	11300	250	μА	STOR BITTER D
Output Current Logic 0	lou	X1	,10101	500	μΑ 20 να	Cleatronic
Propagation Delay	t <sub>PD</sub>	N.IO	elito	30	μS	4
Comparator Sensitivity	V <sub>SINE</sub>	25	20		mVpk-pk	6
Comparator Frequency	C <sub>FREQ</sub>	0		250	KHz	
Comparator Input Resistance	R <sub>IMP</sub>	1 +A -A			M ohm	
Input Capacitance	C <sub>IMP</sub>			5	pF	IT9IRQE I

### NOTES:

- 1. All voltages are referenced to ground.
- 2. Applies to the El pin only.
- 3. Power drain from Vcc input when freshness seal is enabled; 2 µA when freshness seal is broken.
- 4. Propagation delay from comparator inputs to output.
- 5. Only for V<sub>cc</sub>< 3.5 volts.
- 6. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.



# DS1209S-B1 Wireless to 3-Wire Converter Chip

### **FEATURES**

- Adapts a wireless device to a 3-wire serial port (DQ, CLK, and RST\ signals)
- Up to 65,536 devices can be uniquely addressed within the same wireless proximity
- Receives IR, RF, or magnetic pulses as small as 25 millivolts peak-to-peak and frequencies up to 250 KHz
- Low-power operation for both battery backup and battery operate modes
- Makes allowances for extra or missing pulses induced by noise in transmission path
- Counts input pulse packets to interpret data and commands
- Internal state machine generates commands and routes data to and from the 3-wire serial port
- Output pin can gate a variety of transmitting devices
- Simplex 1-wire port can override comparator inputs for input/output to 3-wire serial port
- 3-wire serial port connects to large family of products: DS1201 Electronic Tag, DS1204U Electronic Key, DS5000 Soft Microcontroller, DS1280 3-Wire to Bytewide Converter Chip

### DESCRIPTION

The DS1209S-B1 Wireless to 3-Wire Converter Chip is a low-power CMOS device designed to implement an addressable, full-duplex wireless to 3-wire communications channel. An internal state machine interprets pulse packets which are received at the comparator input pins and routes data to and from the 3-wire serial port. The TX output pin provides a return transmission link for data received from the 3-wire serial port and can gate a variety of transmitting devices. The low-power input comparator, internal to the DS1209S-B1, is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-

### **PIN CONNECTIONS**

VBAT II 1	990 00 16	D	BATREF
VCCO II 2	15	D	A-
VCCI II 3	14	D	A+
FO II 4	V 99:13	b	Floor
TRI II 5	12	D	RST\
DOTRI II 6	11	b	DQ
IIN/OUT II 7	10	I	CLK
GND II 8	V 9	D	TX

(300 MIL) See Mechanical Drawing Section 16, pg. 6

### PIN NAMES (\ Denotes Condition Low)

BATREF	Battery Reference
VBAT	Battery Input
V <sub>cco</sub>	Switched Output
V <sub>cci</sub>	+5V Input
1IN/OUT	1-Wire Input/Output Port
GND	Ground gnilland
TRI	Tri-state DQ, CLK, RST\ Input
DQ TRI	Tri-state Only DQ Input
TX	Wireless Transmit
RST\	RESET (3-Wire Port)
CLK	Clock (3-Wire Port)
DQ	Data Input/ Output (3-Wire Port)
FI/FO	Freshness Seal Input/Output
A+	Non-Inverting Comparator Input
A-	Inverting Comparator Input

peak and frequencies of up to 250 KHz. The DS1209S-B1 also contains a 16-bit chip select value which is stored in the internal command prefix register. This chip select value allows up to 65,536 devices to be uniquely addressed within the same wireless proximity. The 1-wire input/output pin can be used to override the comparator inputs and allow a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. Additionally, a sophisticated power switching circuit is provided which allows for both battery backup and battery operate modes.

### PIN DESCRIPTIONS

 $m V_{BAT}$ -This input is designed to be connected to a battery with a voltage range between 2.5 and 4.0 volts. When  $m V_{CCI}$  is grounded, the DS1209S-B1 acts as a battery-operated device and power is supplied from the  $m V_{BAT}$  pin at all times. This input should NEVER be grounded. If single supply operation is selected, this pin MUST be the power input for the device.

 $m V_{cci}$  - This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to the  $\rm V_{cco}$  pin as long as  $\rm V_{cci}$  is greater than  $\rm V_{BAT}$ . However, when  $\rm V_{BAT}$  is the greater, its voltage will be output. When both  $\rm V_{cci}$  and  $\rm V_{BAT}$  inputs are used, the DS1209S-B1 is in the battery backup mode.  $\rm V_{cci}$  should be grounded when not being used.

 $\rm V_{cco}$  - Switched  $\rm V_{BAT}$  or  $\rm V_{cci}$  output.  $\rm V_{cco}$  will always be the greater of  $\rm V_{BAT}$  or  $\rm V_{cci}$ 

BAT<sub>REF</sub> - This output pin represents the battery voltage input (V<sub>BAT</sub>) less 0.6 volts. It is designed to be connected to the battery input pin on the attached 3-wire device.

1IN/OUT - This input/output pin provides an override for the comparator inputs and allows a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. The pin acts as an input pin for pulse packets containing both command and data input to the 3-wire serial port. Data is also output on the same pin when memory content is read via the 3-wire serial port.

FI/FO - The FI (Freshness In) and FO (Freshness Out) pins combine to give the DS1209S-B1 a method of conserving battery power until placed in service and determine if the low power consumption mode has been entered. The FI pin is used to start (break freshness seal) or stop (enable freshness seal) the continuous power consumption of the comparator on the DS1209S-B1 that is connected to the comparator input pins A+ and A-(Figure 6).

A+,A--These are the inputs for the low-power comparator

TRI-This input is used to tri-state the 3-wire outputs CLK, RST, and DQ. The TRI pin is active in a high state.

DQ TRI - This input is used to tri-state the 3-wire DQ pin only. The DQ TRI pin is active in a high state.

TX - This output pin contains the data which is output from the 3-wire serial port. In a typical application this pin is used to key the wireless transmitter which will send data back to a wireless receiver. RST\ - This output signal is the reset signal for the 3-wire serial port. When RST\ is at high level, the 3-wire port is active and data can be written into or read from the port.

CLK - This output signal is the clock signal for the 3-wire serial port. The clock signal synchronizes data into and out of the DQ line of the 3-wire serial port.

DQ - This input/output is the data input/output for the 3-wire serial port. In a typical application, RST\, CLK, and DQ connect directly to the RST\, CLK, and DQ pins on the DS1204 Electronic Key, DS1201 Electronic Tag, DS1207 TimeKey, or DS1280 3-Wire to Bytewide Converter Chip.

GND - This pin is the ground.

### **OPERATION**

The principle blocks of circuitry contained within the DS1209B-S1 are shown in Figure 1. During normal input conditions, pulse packets present at the comparator input pins pass through the input selector to the pulse counter. The 1-wire port is selected for data input by exception when data is present at the 1-wire port. This data will override the comparator inputs. The 1-wire port pin will be discussed in more detail later in this text. Input pulses arriving at the pulse counter are deciphered into various command codes which affect the command prefix shift register, the state machine, and ultimately the 3-wire serial port. The various command codes are listed in Table 1.

Pulse packets are input to the pulse counter with a 50 us dead time after the last pulse in each packet. The DS1209S-B1 uses the dead time to determine how many pulses were sent and the action to be taken. In addition, if input to the pulse counter is low (inactive) for longer than 1.5 mS, the DS1209S-B1 will time out, reset the command prefix shift register, and place the state machine into an inactive state.

As can be seen in the block diagram of Figure 1 and the command codes listed in Table 1, the input pulses are sent in two different directions. If a pulse packet of 100 pulses (greater than 90) arrives at the pulse counter, the next 24 pulse packets are sent to the command prefix shift register and the state machine is set inactive. The 100-pulse packet always sets the state machine to inactive regardless of any action which may have been occurring (aborts current action/conversation).

The 24 pulse packets which go to the command prefix shift register will cause a normal wake-up or mask wake-up, a read of the chip select bits, a write of the chip select bits, or a lock of the chip select bits. The chip select bits make up the first 16 bits of the 24-bit command prefix shift register. The last eight bits comprise the function field. See Figure 2 and Table 2.

### NORMAL WAKE-UP AND MASK WAKE-UP

Wake-up refers to the sequence of 24 20- or 40-pulse packets received after a 100-pulse packet is sent to set the DS1209S-B1. The 24 pulse packets contain a 16-bit chip select and 8-bit function code which will cause the device state machine to become active. A normal wakeup requires all 16 chip select bits to be matched to those stored on the device before the device becomes active. A masked wake-up requires only a partial match, starting with the least significant bit pair (bit 0,1) and proceeding to the most significant bit pair left unmasked. For example, if the wake-up command (see Table 2) having function code 00011101 -- "mask CS bits 10-15" -- is issued to the DS1209S-B1, then chip select bits 0 through 9 must be correctly matched before the device will become active. The following step-by-step procedure will illustrate normal and mask wake-up:

- 1. First, a 100-pulse packet is sent to the comparator input pins, which puts the state machine into an inactive state.
- 2. Issue wake-up or mask wake-up by sending the 8-bit function code followed by the 16 chip select bits to enable the state machine. The command prefix register is always loaded by sending write zeros (20-pulse packets) or write ones (40-pulse packets). The loaded pulse packets are compared to values stored in the 8-bit Function Code Table and the previously stored 16 chip select bits (storing the chip select values will be covered later).

Pulse packets of 50 to 89 pulses are ignored when loading the command prefix shift register. A pulse packet of greater than 90 pulses always initializes the command prefix shift register back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wake-up is decoded, the command prefix shift register will no longer allow data bits to be written into it and the enable output will become active and remain active until another 100-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corresponding to the number of pulses received as shown in Table 1.

A pulse packet of 80 pulses, followed by a 20-pulse packet, followed by a 40-pulse packet, enables the beacon mode of the state machine. Beacon mode turns on and off the TX pin at a 5 KHz rate for 1.2 seconds. In a typical application utilizing the DS6065A, this signal can be used to key a transmitter (the DS6065A operates at 303.875 MHz), which allows a base unit to lock onto the transmitted beacon.

The DS1209S-B1 is now placed in the active state by issuing a 60-pulse packet which takes RST\ high on the 3-wire serial port. This same 60-pulse packet also turns off the beacon if it has not already timed out. With RST\ high, a conversation can now take place between devices placed on the 3-wire port (DS1201, DS1204U, DS1207, or DS1280) from the comparator inputs, and data is returned to the sending unit via the TX pin. As pulse packets continue to be received, the device attached to the 3-wire port will be written and read using 20-and 40-pulse packets and reset with a 60-pulse packet. The reset pulse packet will take RST\ low until the next pulse packet is detected after the 50 us dead time. When data is read from the 3-wire port, it is always sent to the TX pin for transmission back to the sending unit.

- 4. If an 80-pulse packet is received, the state machine will go to an inactive state but still remains alert for new pulse packets.
- 5. If no pulse packets are received for more than 1.5 mS, the DS1209S-B1 will time out, initialize the command prefix shift register, and set the state machine back to the inactive state. The DS1209S-B1 now waits for new inputs to the protocol serial shift register which begin with a 100-pulse packet.

### **READING THE CHIP SELECT BITS**

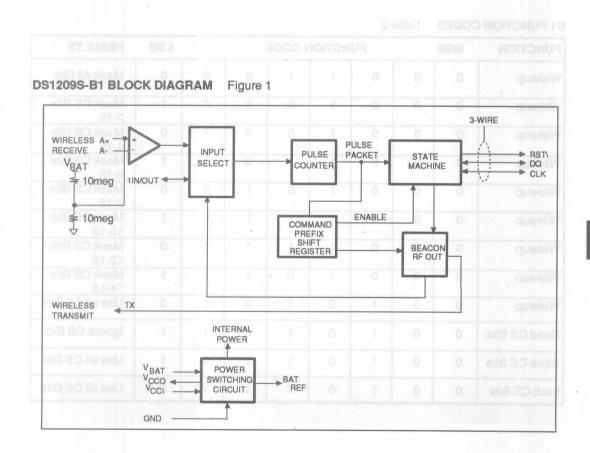
The 16-bit chip select (CS) value stored in the command prefix shift register can be determined in several ways. In fact, an exhaustive search could be implemented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 216 possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the unmasked chip select fields as each set of bits is identified. However, the simplest method of determining the 16-bit CS value is to read the 16-bit value directly. The following step-by-step procedure will illustrate how to read the chip select bits.

1. Wake up the DS1209S-B1 by using the mask all function code. This is accomplished by sending a 100-pulse packet followed by 24 20-pulse and 40-pulse packets. The first eight pulse packets must match the mask all function code. The last 16 pulse packets can be any combination of 20- and 40-pulse packets as the 16 CS bits are masked. Next, the beacon mode of the state machine is enabled by sending an 80-pulse packet followed by a 20- and then a 40-pulse packet. If the beacon mode has been enabled, it should be disabled after receiver lock-on by sending a 60-pulse packet to the comparator inputs.

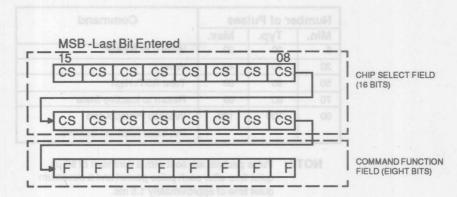
## B1 COMMAND CODES Table 1 MASTYAS TIS SETENDES THE XISSES QUARMOOTINAS

Number of Pulses			Command		
Min.	Тур.	Max.	File and Aller Billion of Annual		
5	20	29	Write 0 or READ		
30	40	49	Write 1		
50	60	69	Take RST\ High		
70	80	89	Return to Inactive State		
90	100	109	Initialize Protocol and Put State Machine Inactive		

NOTE: Pulse packets are sent with a minimum of 50 μs quiet time after each pulse packet and a maximum quiet time of approximately 1.5 ms.



## 24-BIT COMMAND PREFIX SHIFT REGISTER BIT PATTERN Figure 2



### **B1 FUNCTION CODES** Table 2

FUNCTION	MSB	MSB FUNCTION CODE							RESULTS
Wakeup	0	0	0	1	1	0	0	0	Mask All Bits
Wakeup	0	0	0	1	0	0	0	1	Mask CS Bits 2-15
Wakeup	0	0	0	1	0	0	1	0	Mask CS Bits 4-15
Wakeup	0	0	0	1	100	0	101.18	1	Mask CS Bits 6-15
Wakeup	0	0	0	1	0	1	0	0	Mask CS Bits 8-15
Wakeup	0	0	0	GHA	uo1	1	0	1	Mask CS Bits 10-15
Wakeup	0	0	0	1	1	1	1	0	Mask CS Bits 12-15
Wakeup	0	0	0	1	0	1	1	1	Mask CS Bits 14-15
Wakeup	0	0	1	0	1	0	0	0	Use all CS Bits
Read CS Bits	0	0	1	0	1	0	1	1	Ignore CS Bits
Store CS Bits	0	0	1	0	1	1 Agw	0	1 TABV	Use all CS Bits
Lock CS Bits	0	0	1	0	1	11100	10 1	0	Use all CS Bits

- 2. Now load the DS1209S-B1 command prefix shift register with the read CS bits function code. This is accomplished by sending a 100-pulse packet followed by 24 20- or 40-pulse packets. As before, the first eight pulse packets must match the read CS bits function code. However, the last 16 pulse packets can be any combination of 20- and 40-pulse packets, as the 16 CS bits are ignored. During the 24-bit command prefix shift register load, pulse packets of 60 and 80 are ignored. As usual, pulse packets of 100 will initialize the command prefix shift register and set the state machine inactive.
- 3. If the 8-bit function code in the command prefix shift register is correctly matched, then for each 20-pulse packet (read command) received at the comparator input pins, one bit of the 16-bit CS field will be read at the TX pin, the LSB of the field appearing first. Thus, it will receive 16 packets of 20 pulses each to read the entire CS field. If more than 16 read pulse packets are sent to the comparator input pins in this mode, the DS1209S-B1 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 40, 60, or 80 pulses are ignored and 100-pulse packets will initialize the command prefix shift register and set the state machine inactive. This is a non-destructive read and can be aborted at any time during the read process.
- 4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 20- and 100-pulse packet are ignored by the state machine. As usual, the 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

### STORING THE CHIP SELECT BITS

In order to store a new value into the chip select bits of the protocol shift register, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the procedure described in the "Reading Chip Select Bits" section. After obtaining the existing chip select values, a new value can be entered by using the step-by-step procedure which follows:

1. Load the proper 24-bit pattern into the command prefix shift register for storing the chip select bits. This pattern consists of 24 20-pulse and 40-pulse packets. The first eight packets must match the stored CS bits function code. The last 16 pulse packets must match the existing CS bits. During the 24-bit shift register load, only 20- and 40-pulse packets are accepted while 60- and 80-pulse packets are ignored. As always, 100-pulse packets will initialize the command prefix shift register and set the state machine inactive.

- 2. If the 8-bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 20-pulse and 40-pulse packets are accepted. Pulse packets of 60 and 80 are ignored and 100-pulse packets cause the stored CS bit command to abort, initializing the command prefix shift register and returning the state machine to inactive. The DS1209S-B1 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new packets will continue to shift in, storing the last 16 packets that are received.
- 3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 100-pulse packet, which will initialize the command prefix shift register and return the state machine to an inactive state. A timeout of 1.5 mS will have the same effect as a 100-pulse packet.

### LOCKING THE CHIP SELECT BITS

The design of the DS1209S-B1 allows for both battery backup and battery operation. The device consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the command prefix shift register CS bits, are nonvolatile. A special latch is provided so that upon initial power up (when battery is first connected) the nonvolatile chip select bits can be written with a store CS function code.

The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip select bits cannot be changed until power is removed (battery disconnected) from the DS1209S-B1. The lock CS bit can be accomplished by the following step-by-step procedure.

- 1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.
- 2. The 8-bit function code for locking the CS bits is transmitted, followed by the 16-bit chip select value. Only 20- and 40-pulse packets are accepted; 60- and 80-pulse packets are ignored. A 100-pulse packet will cause the lock CS bits to abort, initializing the command prefix shift register and returning the state machine to the inactive state.
- 3. Once the 24-bit command prefix shift register is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.
- 4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock CS operation the main state machine is disabled so that all pulse

packets have no effect. As usual, a 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

### POWER SWITCHING CIRCUIT

As shown in the block diagram of Figure 1, the DS1209S-B1 can receive its power from two different sources: the V<sub>ccl</sub> input or the V<sub>BAT</sub> input. The DS1209S-B1 is designed to work off of a battery supply as low as 2.5 volts. However, if an alternate supply is available, it can be connected to the V<sub>cci</sub> pin. A voltage level of 3 volts minimum is required on the  $V_{\rm BAT}$  pin for proper operation. With both the  $V_{\rm CCI}$  pin and the  $V_{\rm BAT}$  pin attached to appropriate power sources, the DS1209S-B1 will automatically select the supply input which is the higher level. If only one power source is connected, it MUST be connected to the V<sub>BAT</sub> input. The V<sub>BEF</sub> output is designed specifically to supply power to a connected 3-wire device such as a DS1204U, DS1201, DS1207, or DS1280. The V<sub>BEE</sub> output is equal to the V<sub>BAT</sub> input less a voltage drop of about 0.5 volts. This pin is capable of sourcing a current of 2 mA.

### PULSE PACKETS wood to almuome Jackson

The minimum time between pulse packets is 50 us and the idle time of 1.5 mS will always cause the protocol shift register to initialize and the state machine to go inactive.

Pulse packets range from 20 pulses to 100 pulses, depending on the action to be taken (see command codes in Table 1). If a read pulse packet is detected, data is to be read from a device connected on the 3-wire serial port and the TX pin will become active high for a logic 1 or remain low for a 0. Time is allotted beyond the 50 us between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 375 us window. If a logic 0 is being sent, the TX pin will remain low for the entire window. If a logic 1 is being sent, the TX pin will be driven to high level within a maximum of 75 us and will remain high for a minimum of an additional 150 us.

However, if a minimum of four pulses is received at the comparator inputs, the TX pin activity is terminated on the assumption that a logic 1 has been received and the sending unit has started the next pulse packet. The timing diagram of Figure 3 illustrates the comparator output and the TX pin timing relationship.

### COMPARATOR OPERATION

The low-power comparator inputs are brought out to the user on the A+ and A- pins. The low- power input comparator is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz.

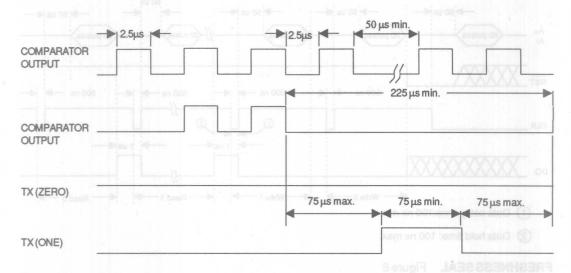
### 1IN/OUT

This pin is an input/output one-wire signal port designed to override the comparator input pins and multiplex the TX pin on a single connection. Data is input on the port pin using a frequency of one-half the comparator input frequency with a symmetrical high and low time of 5 us ± 20%. Therefore, the time between pulse packets is 2X the time allotted between pulse packets when 250 KHz is used. If a read pulse packet is detected, time is allotted beyond the 100 us between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 450 us window. If a logic 1 is being sent, the 1 IN/OUT pin will remain low for the entire window. If a logic 0 is being sent, the 1IN/OUT pin will be tri-stated to a high impedance state by the DS1209B and should be pulled high using a pullup resistor. This high impedance state will occur within a maximum of 150 us and remain for a maximum of 150 us. The 1IN/OUT pin is guaranteed to be inactive after a third 150 us time period. The timing diagram of Figure 4 illustrates the 1IN/OUT timing.

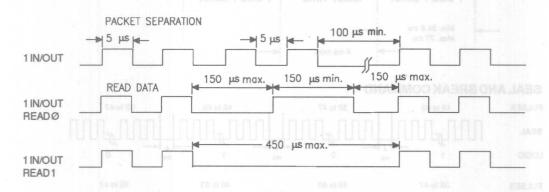
### RST, CLK, AND DQ

The 3-wire serial port on the DS1209S-B1 consists of the RST\, CLK, and DQ signals. These signals are designed to connect directly to the CLK, RST\, and DQ lines of various 3-wire devices, such as the DS1204U, DS1207. DS1201, or DS1280. The RST\pin on the DS1209S-B1 is driven to a high level whenever a 60-pulse packet is received by the state machine. The RST\signal remains high until a 80- or 100-pulse packet is received or until 1.5 mS has elapsed without activity at the comparator inputs. The CLK pin on the DS1209S-B1 is normally high until the RST\signal is high. When RST\ is high and a 20- or 40pulse packet is received by the state machine (indicating a "read from" or "write to" the 3-wire port), the CLK pin is driven low for a period of 500 ns minimum to 1.0us maximum. If data is being read from a device on the 3wire serial port, it will become valid within 200 ns of the falling edge of the clock returned to the sending unit. The output will be a high level for a logic 1 or remain at low level for a logic 0. If data is being written to a device on the 3wire serial port, then data will be sent from the state machine to the DQ line prior to the falling edge of the clock. This data will remain valid until the clock transitions back to a high level. The TX pin remains low while data is being written to the 3-wire serial port. A timing diagram for the 3-wire serial port is shown in Figure 5. For more detailed information on the 3-wire serial port, see the data sheets on the DS1201, DS1207, or DS1280.

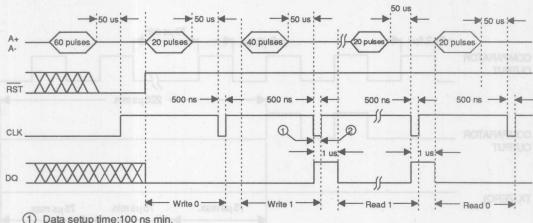
#### **COMPARATORINPUTTIMING** Figure 3



#### 1IN/OUTTIMING Figure 4



#### RST, CLK, AND DQ TIMING Figure 5

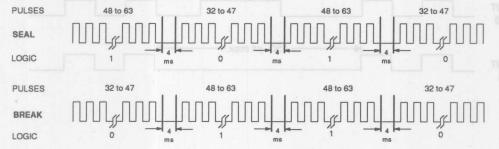


- (1) Data setup time:100 ns min.
- (2) Data hold time: 100 ns max.

#### FRESHNESS SEAL Figure 6



#### SEAL AND BREAK COMMAND



#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage On Any Pin Relative to Ground Storage Temperature Operating Temperature Soldering Temperature

0.5V to +7V -55° to +125°C 0° to 70° C 260° for 10 sec.

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Input	V <sub>cci</sub>	3.0	5.0	5.5	Volts	1,2
Battery input	V <sub>BAT</sub>	2.5		4.0	Volts	1,2
Input Logic 1	V <sub>IH</sub>	2.0		V <sub>cc</sub> +0.3	Volts	1,3
Input Logic 0	V <sub>IL</sub>	-0.3		0.8	Volts	1

#### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5 V, V<sub>BAT</sub> = 3 V, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Reference	V <sub>REF</sub>	V <sub>BAT</sub> -0.7		V <sub>BAT</sub>	Volts	1
Switched Voltage Out	V <sub>cco</sub>	V <sub>cci</sub> -0.3		gringe	Volts	1,4
Switched Current Out	Icco	3	4	0.	mA Maria	ni baeng dinao
Operating Current	I <sub>cc</sub>		2 0 %	75	uAm brutered	met gr6sregO e
Standby Current	I <sub>cc1</sub>			2	uA	7
Output Logic 1	V <sub>OH</sub> MING	V <sub>cc</sub> -10%		ES	Volts	MA 1,3 UO
Output Logic 0	V <sub>OL</sub>		Raigt	0.4	Volts	Electrofile Ident
Output Current Logic 1	I <sub>OH</sub>		nformation	250	uA	« Chlo-based dat
Output Current Logic 0	olonamib (A)			500	uA	eacher adace
Comparator Leakage Current	FIL.	-1.0	Ngnia s r	1.0 fw faori o	uA aeteoinumicates	8 Economically
Comparator Sensivity	V <sub>SINE</sub>	25	20		mV	9
Comparator Frequency	C <sub>FREQ</sub>	40	nuane ioc	250	KHz	w williditeconso
Comparator Input Resistance	R <sub>IMP</sub>	1	sceptacle	n gnitsm r	M ohm	al equita-nico à
Input Capacitance	C <sub>IO</sub>	ACCE	sinemno	5	pF   19914 33	Durable stainle

#### NOTES

- 1. All voltages are referenced to ground.
- When both the battery and supply pins are being used, V<sub>CCI</sub> should be at least 500 mV higher than V<sub>BAT</sub> when V<sub>CCI</sub> is supplying power.
- 3.  $V_{\rm CC}$  applies to the greater of  $V_{\rm CCI}$  or  $V_{\rm BAT}$  depending on which input is supplying power.
- 4.  $V_{\rm CCO}$  is either  $V_{\rm CCI}$  -0.3 V or  $V_{\rm BAT}$  -0.3 V.
- 5.  $I_{cco}$  is current coming from  $V_{BAT}$  or  $V_{cci}$  depending on which input is supplying power.
- Operating current comes from V<sub>CCI</sub> or V<sub>BAT</sub> depending on which is supplying power and if power is consumed by the DS1209S-B1 when comparator or 1-wire is active.
- 7. With freshness seal not broken, receiver standby current is 50 nA.
- Leakage current applies to all inputs except V<sub>cci</sub> and V<sub>BAT</sub>. 1 IN/OUT, TRI, and DQTRI have 150 μA max. leakage to ground.
- 9. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.



# DS1990 Touch Serial Number

#### **DS1990 SPECIAL FEATURES**

- Unique 48-bit serial number
- Low-cost electronic key for access control
- 8-bit CRC for checking data integrity
- Can be read in less than 5 msec
- Operating temperature range: -40 to +85° C

#### **TOUCH FAMILY FEATURES**

- Electronic identification by momentary contact
- Chip-based data carrier compactly stores information
- · Can be accessed while affixed to object
- Economically communicates to host with a single digital signal
- Standard 16mm diameter and 1-Wire protocol ensure compatibility with Touch Memory family
- · Coin-shape is self-aligning with mating receptacles
- Durable stainless steel case resists environmental hazards
- Unique, factory-lasered 48-bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing
- Presence detect signal announces connection to host

# Data Data Dimension Tolerance: + 005

Dimension Tolerance: ±.005
(All dimensions shown in millimeters)

R3 PACKAGE

#### CONTACTS

Rim Ground Inner Face Data

#### **ACCESSORIES**

DS9092 Touch Memory Probe, Hand-Grip

or Panel Mount

DS9093 Touch Memory KeyRing Mount

DS9094 Touch Memory Clip

DS9096 Self-Stick Adhesive Pad

#### ORDERING INFORMATION

DS1990-R3 R3 Package

#### DESCRIPTION

The DS1990 Touch Serial Number is a rugged data carrier that acts as an electronic serial number for automatic identification. The DS1990 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return.

The durable MicroCan package is highly resistant to

environmental hazards such as dirt, moisture and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1990 to be easily used by human operators. Accessories permit the DS1990 to be mounted on plastic key fobs, photo-ID badges, printed-circuit boards or any smooth surface of an object. Applications include access control, work-in-progress tracking, tool management and inventory control.

#### OPERATION is belowed and referent and ent

The DS 1990's internal ROM is accessed via a single data line. The 48-bit serial number, family code and CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

#### 1-Wire Protocol

The 1-Wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1990 is a slave device. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence. For a more detailed protocol description, refer to Application Note #23, "Using the 1-Wire Protocol."

Hardware Configuration - The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection. The DS1990 is an open drain part with an internal circuit equivalent to that shown in Figure 2. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 3. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

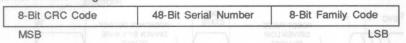
The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 uS. all of the slave devices on the bus will be reset.

#### Transaction Sequence

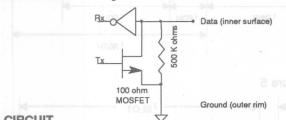
The sequence between the bus master and the DS1990 is as follows:

> Presence Detect 1-Wire Command Word Family Code 48-Bit Serial Number **CRC** Byte

#### **DS1990 MEMORY MAP** Figure 1

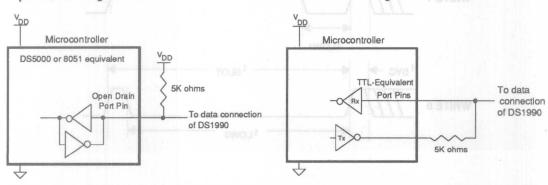


#### **DS1990 EQUIVALENT CIRCUIT Figure 2**



#### **BUS MASTER CIRCUIT** Open Drain Figure 3A

#### Standard TTL Figure 3B



021192 2/7

Reset/Presence Detect - All transactions on the 1-Wire bus begin with a reset. The DS1990 is reset by holding the data line low for more than 480µS. (When the DS1990 is not connected to the bus, it is held in reset by an internal pull-down, but when connected to the bus, the data line is pulled high and the part is taken out of reset and is ready to issue its presence detect.)

After detecting a high data line, the DS1990 waits  $15\mu S$  minimum and issues its presence detect. This presence detect is a low-going pulse that lasts a minimum of  $60\mu S$ . This response to the reset pulse lets the bus master know that the DS1990 is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from the noise as devices are taken on and off the bus. Refer to the timing diagram in Figure 4.

After the DS1990 has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of  $1\mu$ S. This  $1\mu$ S interval is like a frame sync. After each bit is transmitted on the bus, there is a frame pulse to sync up for the next transmission.

Once the bus master has detected a presence on the bus, it transmits the read command 0Fh to the DS1990 LSB first. This will set the DS1990 into the transmit mode.

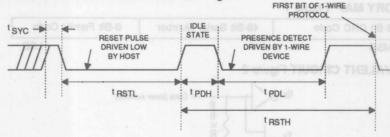
After receipt of the read command, the DS1990 will send back, in order, the 8-bit family code (01h for the DS1990), the 48-bit serial number and the 8-bit CRC, with the LSB of each field sent first.

#### Transmitting /Receiving Data

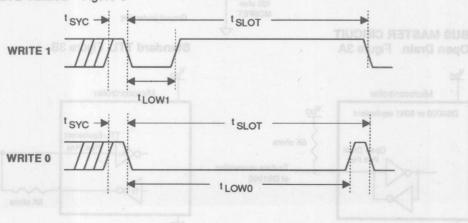
All communications on the 1-Wire bus begin with the reset and presence detect sequence. The bus master then transmits the 1-Wire read command to tell the DS1990 to get ready to transmit data. To transmit the first bit of the Read command word, the master pulls the bus low for  $1\mu s$ . This low-going edge informs the DS1990 that the first bit is being sent. After  $1\mu S$ , the master does one of two things:

- Holds the line low for an additional 60µS to output a zero (write a 0) or,
- Lets the bus go high for an additional 60μS (write a 1).

#### 1-WIRE RESET/PRESENCE DETECT TIMING Figure 4



#### 1-WIRE WRITE TIMING Figure 5



The state of the bus during this 60µS time phase determines the value of the bit. This process is repeated until all eight bits are transmitted. Refer to the timing diagram in Figure 5.

The bus master now reads in order, LSB first of each field, the family code, serial number and CRC. A read cycle is similar to a write cycle. It is started with the bus master pulling the bus low for 1µS. This informs the DS1990 that it should have its data on the bus no later than the 1µS from the falling edge. After the 1µS, the bus master lets go of the bus and lets the DS1990 drive the bus. The DS1990 must then hold the data on the bus for an additional 14uS minimum (59uS maximum). During this holding time, the bus master reads the state of the bus. The bus master should read data from the bus within 15µS after the falling edge. The entire cycle for a bit lasts a minimum of 60µS (120µS maximum) from the falling edge. At the end of the cycle, the bus master must drive the bus high for 1µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 6 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1990 must be reset.

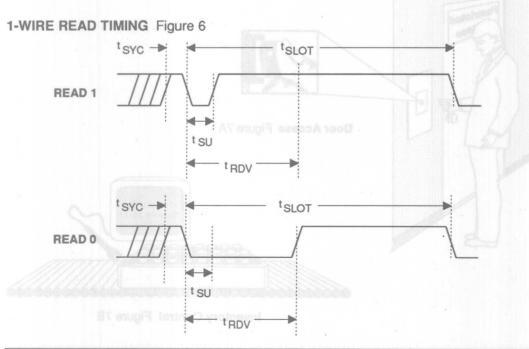
#### CRC GENERATION

To validate the data transmitted from the DS1990, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1990. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but *not* over the stored CRC value itself. If the two CRC values match, the transmission is error-free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the 5000 Soft Microcontroller which is compatible with the 8031/51 Microcontroller family. The procedure DO\_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. It should be noted that the variable CRC needs to be initialized to 0 before the procedure is executed. Each byte of the data is then placed in the accumulator and DO\_CRC is called to update the CRC variable. After all the data has been passed to DO\_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is:

$$CRC = X^8 + X^5 + X^4 + 1$$

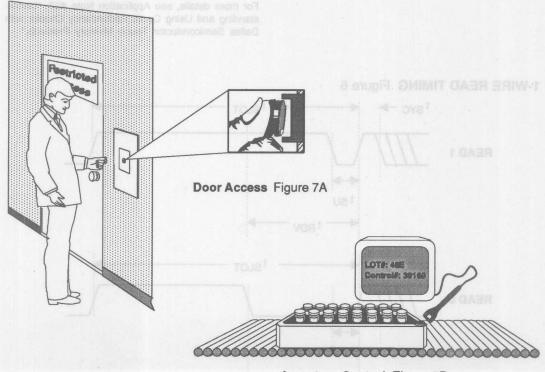
For more details, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."



#### CRC ASSEMBLY LANGUAGE PROCEDURE Table 1 q and 2400 and grid to desid and

DO_CRC:	PUSH	ACC	; save the accumulator
	PUSH	B	; save the B register
	PUSH	ACC	; save bits to be shifted
	MOV	B,#8	; set shift = 8 bits
CRC_LOOP:	XRL	A,CRC	; calculate CRC
	RRC	A	; move it to the carry
	MOV	A,CRC	; get the last CRC value
	JNC	ZERO	; skip if data = 0
	XRL	A,#18H	; update the CRC value
ZERO: and a property of the country	RRC MOV POP RR PUSH DJNZ POP POP POP RET	A CRC,A ACC A ACC B,CRC_LOOP ACC B ACC	; position the new CRC ; store the new CRC ; get the remaining bits ; position the next bit ; save the remaining bits ; repeat for eight bits ; clean up the stack ; restore the B register ; restore the accumulator

#### **DS1990 APPLICATIONS**



**Inventory Control** Figure 7B

#### **ABSOLUTE MAXIMUM RATINGS\***

Voltage On Data Pin Relative to Ground Operating Temperature Storage Temperature -0.5V to +7V -40°C to 85°C -55°C to +125°C

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(-40°C to 85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5		5.5	Volts	1
Pull-up Voltage	V <sub>PUP</sub>	4.5	NESKI	5.5	Volts	1 098180

#### DC ELECTRICAL CHARACTERISTICS

 $(V_{cc} = 5V + 10\%, -40^{\circ}C \text{ to } 85^{\circ}C)$ 

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V <sub>IL</sub>	-0.5	840A.) 310	0.4	Volts	6
Input Logic High	V <sub>IH</sub>	3.0	5.0	5.5	Volts	4, 6
Output Logic Low @ 4mA	V <sub>OL</sub>		A A	0.4	Volts	6
Output Logic High	V <sub>OH</sub>			5.5	Volts	6
Input Resistance	R		500K		Ohms	2
Operating Charge	I <sub>OP</sub>			30	nC	5,6

#### AC ELECTRICAL CHARACTERISTICS

 $(-40^{\circ}\text{C to }85^{\circ}\text{C}, \ V_{_{IH}} = 5\text{V} \pm 10\%)$ 

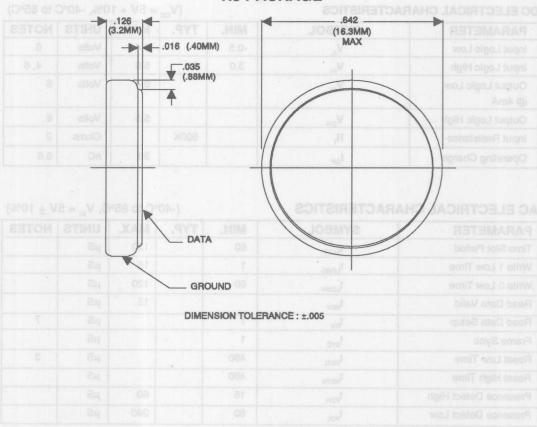
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t <sub>slot</sub>	60	Albert	120	μS	
Write 1 Low Time	t <sub>LOW1</sub>	1		15	μS	
Write 0 Low Time	t <sub>LOW0</sub>	60	080	120	μS	
Read Data Valid	t <sub>RDV</sub>			15	μS	
Read Data Setup	t <sub>su</sub>	ANT JUNE AND ADDRESS	Carrier Carrier		μS	7
Frame Sync	t <sub>syc</sub>	1			μS	
Reset Low Time	t <sub>RSTL</sub>	480			μS	3
Reset High Time	t <sub>RSTH</sub>	480			μS	
Presence Detect High	t <sub>PDH</sub>	15		60	μS	
Presence Detect Low	t <sub>PDL</sub>	60		240	μS	

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Input is pulled to ground.
- 3. An additional reset or communications sequence cannot begin until the reset high time has expired.
- 4. V<sub>IN</sub> is a function of the external pull-up resistor and the V<sub>CC</sub> supply.
- 5. 30 nanocoulombs per 72 time slots @ 5.0V.
- 6.  $@V_{cc} = 5.0$  volts with a 5K pull-up to  $V_{cc}$  and a maximum time slot of 120 $\mu$ s.
- 7. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1µS of this falling edge and will remain valid for 14µS minimum (15µS total from falling edge on 1-Wire).

#### **DS1990 TOUCH SERIAL NUMBER**

#### **R3 PACKAGE**



# **DALLAS**SEMICONDUCTOR

## DS1991 Touch MultiKey

#### **DS1991 SPECIAL FEATURES**

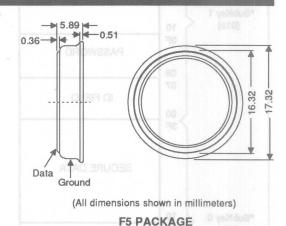
- 1,152-bit secure read/write, nonvolatile memory
- Secure memory cannot be deciphered without matching 64-bit password
- Memory is partitioned into 3 blocks of 384 bits each
- 64-bit password and ID fields for each memory block
- 512-bit scratchpad ensures data transfer integrity
- Operating temperature range: -20° to +70° C
- Over 10 years of data retention

#### **TOUCH MEMORY FEATURES**

- Electronic identification by momentary contact
- Chip-based data carrier compactly stores information
- · Can be accessed while affixed to object
- Economically communicates to host with a single digital signal
- Standard 16mm diameter and 1-Wire protocol ensure compatibility with Touch Device family
- · Coin shape is self-aligning with mating receptacles
- Durable stainless steel case resists environmental hazards
- Unique, factory-lasered 48-bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing or snap-in flange
- · Presence detect signal announces connection to host

#### **DESCRIPTION**

The DS1991 Touch MultiKey is a rugged data carrier that acts as three separate electronic keys, offering 1,152 bits of secure, read/write nonvolatile memory. Each key is 384 bits long with distinct 64-bit password and public ID fields. The password field must be matched in order to access the secure memory. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return.



CONTACTS	
Rim	Ground
Inner Face	Data

#### **ACCESSORIES**

DS9092	Touch Memory Probe, Hand-Grip or

Panel Mount

DS9093F Touch Memory KeyRing Mount

DS9094F Touch Memory Clip

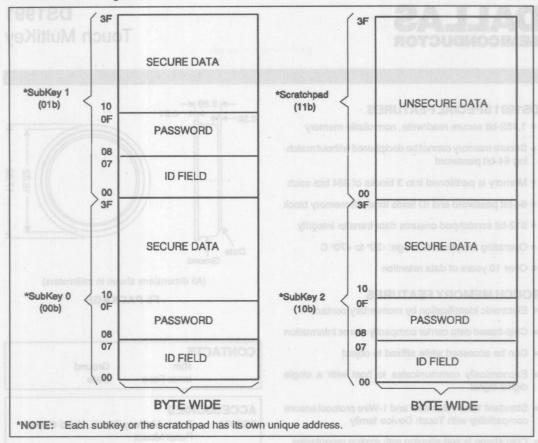
DS9096 Self-Stick Adhesive Pad

#### ORDERING INFORMATION

DS1991L-F5 10 year expected life, flanged rim, 5.89mm thickness

The 512-bit scratchpad serves to ensure integrity of data transfers to secure memory. A 64-bit factory-lasered ROM provides a unique identity to each DS1991, with an 8-bit family code, a 48-bit serial number, and an 8-bit CRC. The family code for the DS1991 is 02h. in order to access the secure memory. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground

#### **MEMORY MAP** Figure 1



return. The 512-bit scratchpad serves to ensure data integrity of transfers to secure memory. A 64-bit factory-lasered ROM provides a unique identity to each DS1991, with an 8-bit family code, a 48-bit serial number, and an 8-bit CRC. The family code for the DS1991 is 02h.

The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1991 to be easily used by human operators. Accessories permit the DS1991 to be mounted on plastic key fobs, photo-ID badges, printed-circuit boards or any smooth surface of an object. Applications include secure access control, debit tokens, work-in-progress tracking, electronic travelers and proprietary data.

#### **OPERATION**

The DS1991 is accessed via a single data line using the

1-Wire protocol. The communication sequence has two distinct subsequences: the 1-Wire device selection sequence and the device-specific command sequence. The 1-Wire sequence precedes the device-specific command sequence to identify the particular device on the bus. This protocol is described in detail in the following section, "1-Wire Protocol."

The DS1991 has six device-specific commands: Scratchpad Write, Scratchpad Read, Subkey Write, Subkey Read, Set Password and Move Block.

#### **COMMAND WORD**

The DS1991 is controlled through the command word. After the device is selected, the command word is written. The command word is comprised of three fields, each one byte long. The least significant byte is the function code field. This field defines the six commands that can be executed. The second byte is the address field. The first six bits of this field define the starting address of the

command. The last two bits of this field are the subkey address code. The third byte of the command word is a

complement of the second byte (Figure 2). Each command in the command word is address-specific

#### COMMAND WORD STRUCTURE Figure 2

Command Field:

MSB

A<sub>7</sub>-A<sub>0</sub>

C<sub>7</sub> C<sub>6</sub> C<sub>5</sub> C<sub>4</sub> C<sub>3</sub> C<sub>2</sub> C<sub>1</sub> C<sub>0</sub>

B<sub>7</sub> B<sub>6</sub> B<sub>5</sub> B<sub>4</sub> B<sub>3</sub> B<sub>2</sub> B<sub>1</sub> B<sub>0</sub>

A<sub>7</sub> A<sub>6</sub> A<sub>5</sub> A<sub>4</sub> A<sub>3</sub> A<sub>2</sub> A<sub>1</sub> A<sub>0</sub>

BYTE 1

	BYTE 2	sabilait baassassa bas CI arti baltimi vav
B <sub>7</sub> -B <sub>6</sub>		
, ,	2 hits specifying which partition is to be accessed	
	OI COUNCY I	
	10 SubKoy 2	
	11—Scratchpad	
B <sub>s</sub> -B <sub>o</sub>	Address Field:	lubKey Write
* *	6 bits that define the starting byte address in the scrate	chpad or any subkey

	YTE 3 angoni ai browesso ent 11 Jose natihw nert al brow		
C <sub>7</sub> -C <sub>6</sub> Parti	Partition Identifier Field:	ne transaction is terminated. Otherwise, the data	
	bit for bit complement of byte 2		
C <sub>5</sub> -C <sub>0</sub>	Address Field:	command ward, cata can be communisty weight intil the end of the secure subject is reached or until	
	bit for bit complement of byte 2		

#### **COMMAND CONFIGURATIONS** Figure 3

Byte 1

one averidue ont Byte 2 exidua beloelea enti mont

Command	Valid Commands	Valid Subkeys Address	Valid Addresses
ScratchPad Write	96ha a wasa araaw	ant 116 due ent mon	00h-3Fh
ScratchPad Read	69h	arts to 11b a erts litrus	00h-3Fh
Subkey Write	99h	00b, 01b, 10b	10h-3Fh
SubKey Read	66h	00b, 01b, 10b	10h-3Fh
Set Password	5Ah	00b, 01b, 10b	00h
Move Block	3Ch	00b, 01b, 10b	00h

NOTE: Byte 3 is complement of byte 2

and therefore precludes the use of certain subkey codes and starting address locations (Figure 3).

#### **SUBKEY COMMANDS**

Each of the subkeys within the DS1991 is accessed individually. Transactions to read and write data to a secured subkey start at the address defined in the command word and proceed until the device is reset or the end of the subkey is reached. The three commands that operate on the secure subkeys are Set Password, Secure Data Write, and Secure Data Read.

#### Set Password

The Set Password command is used to enter the ID and password of the selected subkey. This command will erase all of the data stored in the secure area as well as over writing the ID and password fields with the new data. The DS1991 has a built-in check to ensure that the proper subkey was selected. The sequence begins by reading the ID field of the selected subkey; the ID of the subkey to be changed is then written into the part. If the IDs do not match, the sequence is terminated. Otherwise, the subkey contents are erased and 64 bits of new ID data are written followed by a new 64-bit password. The command sequence is shown in Figure 4.

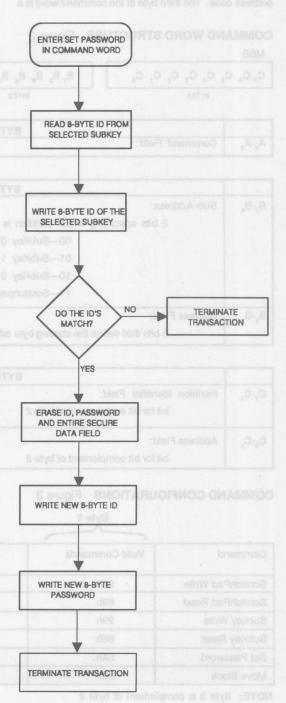
#### **SubKey Write**

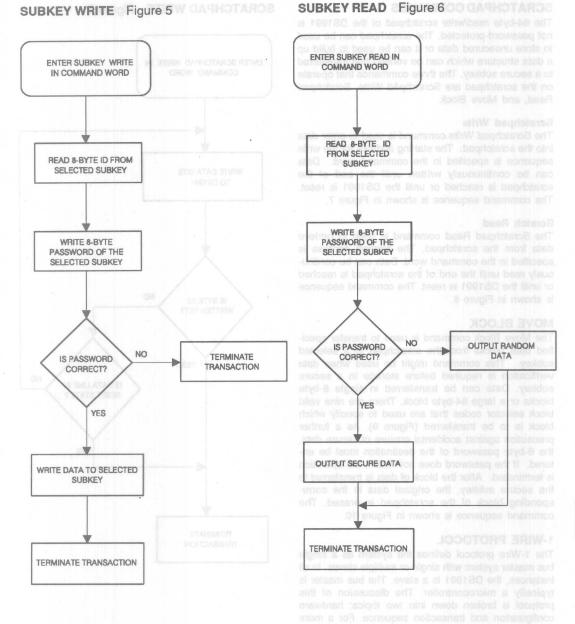
The Subkey Write command is used to enter data into the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the transaction is terminated. Otherwise, the data following is written into the secure area. The starting address for the write sequence is specified in the command word. Data can be continuously written until the end of the secure subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 5.

#### SubKey Read

The Subkey Read command is used to retrieve data from the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the DS1991 will transmit random data. Otherwise the data can be read from the subkey. The starting address is specified in the command word. Data can be continuously read until the end of the subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 6.

#### SET PASSWORD Figure 4





#### SCRATCHPAD COMMANDS

The 64-byte read/write scratchpad of the DS1991 is not password-protected. The scratchpad can be used to store unsecured data or it can be used to build up a data structure which can be verified and transferred to a secure subkey. The three commands that operate on the scratchpad are Scratchpad Write, Scratchpad Read, and Move Block.

#### Scratchpad Write

The Scratchpad Write command is used to enter data into the scratchpad. The starting address for the write sequence is specified in the command word. Data can be continuously written until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 7.

#### Scratch Read

The Scratchpad Read command is used to retrieve data from the scratchpad. The starting address is specified in the command word. Data can be continuously read until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 8.

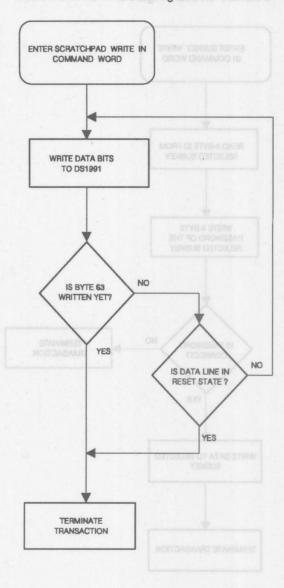
#### **MOVE BLOCK**

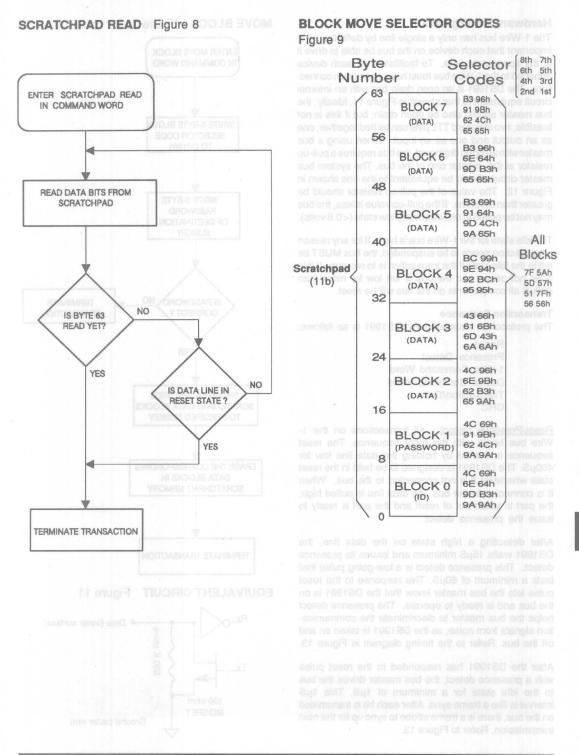
The Move Block command is used to transfer specified data blocks from the scratchpad to a selected subkey. This command might be used when data verification is required before storage in a secure subkey. Data can be transferred in single 8-byte blocks or a large 64-byte block. There are nine valid block selector codes that are used to specify which block is to be transferred (Figure 9). As a further precaution against accidental erasure of secure data, the 8-byte password of the destination must be entered. If the password does not match, the operation is terminated. After the block of data is transferred to the secure subkey, the original data in the corresponding block of the scratchpad is erased. The command sequence is shown in Figure 10.

#### 1-WIRE PROTOCOL

The 1-Wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1991 is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence. For a more detailed protocol description, refer to Application Note 23, "Using the 1-Wire Protocol."

#### SCRATCHPAD WRITE Figure 7





#### Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain connections. The DS1991 is an open drain part with an internal circuit equivalent to that shown in Figure 11. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 12. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur, and the bus is left low for more than 480µS all components on the bus will be reset.

#### **Transaction Sequence**

The protocol for accessing the DS1991 is as follows:

Reset
Presence Detect
1-Wire Command Word
Device Command Word
Transaction/Data
CRC

Reset/Presence Detect - All transactions on the 1-Wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 480μS. The DS1991 is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high; the part is taken out of reset and the part is ready to issue the presence detect.

After detecting a high state on the data line, the DS1991 waits  $15\mu S$  minimum and issues its presence detect. This presence detect is a low-going pulse that lasts a minimum of  $60\mu S$ . This response to the reset pulse lets the bus master know that the DS1991 is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise, as the DS1991 is taken on and off the bus. Refer to the timing diagram in Figure 13.

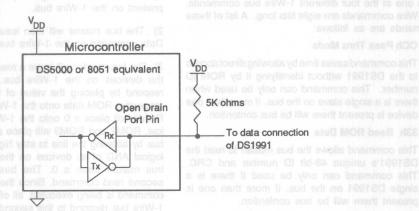
After the DS1991 has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of  $1\mu S$ . This  $1\mu S$  interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 13.

# MOVE BLOCK Figure 10 ENTER MOVE BLOCK IN COMMAND WORD WRITE 8-BYTE BLOCK SELECTOR CODE TO DS1991 WRITE 8-BYTE **PASSWORD** OF DESTINATION SUBKEY NO TERMINATE IS PASSWORD CORRECT TRANSACTION YES TRANSFER SPECIFIED SCRATCHPAD DATA BLOCKS TO SPECIFIED SUBKEY **ERASE THE CORRESPONDING DATA BLOCKS IN** SCRATCHPAD MEMORY TERMINATE TRANSACTION **EQUIVALENT CIRCUIT** Figure 11 Data (inner surface) ohms × 500 100 ohm

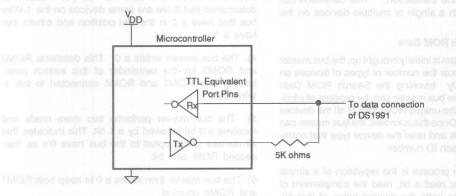
MOSFET

Ground (outer rim)

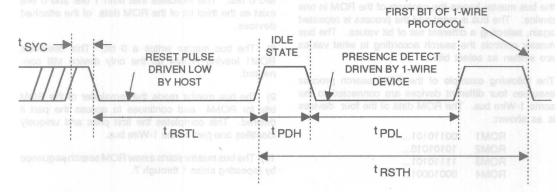
#### BUS MASTER OPEN DRAIN CIRCUIT Figure 12A



## BUS MASTER STANDARD TTL CIRCUIT Figure 12B



#### RESET/PRESENCE DETECT SEQUENCE Figure 13



#### 1-Wire Command Word

Once the bus master has detected a presence it can issue one of the four different 1-Wire bus commands. All 1-Wire commands are eight bits long. A list of these commands are as follows:

#### **CCh Pass Thru Mode**

This command saves time by allowing direct access to the DS1991 without identifying it by ROM ID number. This command can only be used when there is a single slave on the bus. If more than one device is present there will be bus contention.

#### 33h Read ROM Data

This command allows the bus master to read the DS1991's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1991 on the bus. If more than one is present there will be bus contention.

#### 55h Match ROM Data

This mode allows the bus master to single out a specific DS1991 on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple devices on the bus

#### F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the unique ROM data of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple three-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-Wire bus. The ROM data of the four devices is as shown:

ROM1 00110101... ROM2 10101010... ROM3 11110101... ROM4 00010001... The search process is as follows:

- 1) The bus master begins by resetting all devices present on the 1-Wire bus.
- The bus master will then issue the Search ROM Data command on the 1-Wire bus.
- 3) The bus master will issue a read command to all of the devices on the 1-Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the bus master sees a 0. The bus master issues a second read command. Since the Search ROM data command is being executed, all of the devices on the 1-Wire bus respond to this second read command by placing the complement of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-Wire bus that have a 0 in the first position and others that have a 1.
- 4) The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-Wire bus.
- 5) The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
- The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
- 7) The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
- 8) The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
- 9) The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-Wire bus.
- 10) The bus master starts a new ROM search sequence by repeating steps 1 through 7.

- 11) The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
- 12) The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
- 13) The bus master starts a new ROM search by repeating steps 1 through 3.
- 14) The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
- 15) The bus master executes two read time slots and receives two zeros.
- 16) The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.
- 17) The bus master reads the remainder of the ROMbits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.
- 18) The bus master starts a new ROM search by repeating steps 13 through 15.
- 19) The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
- 20) The bus master reads the remainder of the ROMbits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

#### Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-Wire device on each ROM Search operation. The time required to derive the part's unique ID is:

$$960\mu S + (8 + (3 + 64)) \times 60\mu S = 12.96mS$$

The bus master is therefore capable of identifying 77 different 1-Wire devices per second.

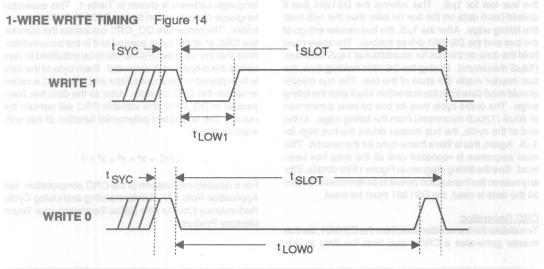
Additionally, the data obtained from the two reads of each set of three have the following interpretations:

- 00 There are still devices attached which have conflicting bits in this position.
- 01 All devices still coupled have a zero bit in this bit position.
- 10 All devices still coupled have a one bit in this bit position.
- 11 There are no devices active on the 1-Wire bus.

#### Transmitting/Receiving Data

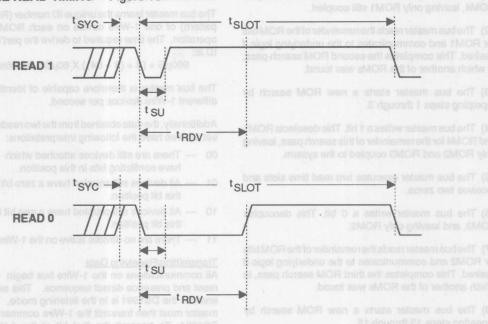
All communications on the 1-Wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1991 is in the listening mode. The bus master must then transmit the 1-Wire command to the DS1991. To transmit the first bit of the 1-Wire bus command word, the master pulls the bus low for 1µS. This low-going edge informs the DS1991 that the first bit is being sent. After 1µS, the master does one of two things: We amail out at aid. This is the frame syling

- 1) Holds the line low for an additional 60µS to output a 0 (write a zero) or,
- 2) Lets the bus go high for an additional 60µS (write a 1).



021192 11/14

#### 1-WIRE READ TIMING Figure 15



The state of the bus during this  $60\mu S$  time phase determines the value of the bit. This is the frame sync mentioned earlier. This process is repeated until all the 8 bits are transmitted. Refer to the timing diagram in Figure 14.

The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1uS. This informs the DS1991 that it should have data on the bus no later than the 1µS from the falling edge. After the 1µS, the bus master lets go of the bus and the DS1991 drives the bus. The slave must hold the data on the bus for an additional 14µS minimum (59uS maximum). During the DS1991 holding time, the bus master reads the state of the bus. The bus master should read data from the bus within 15µS after the falling edge. The entire cycle time for one bit lasts a minimum of 60uS (120uS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 15 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1991 must be reset.

#### **CRC** Generation

To validate the transmitted data from the DS1991, the bus master generates a CRC value from the data as it is

received. This generated value is compared to the value stored in the last eight bits of the DS1991. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. If the two CRC values match, the transmission is error-free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the DS5000 Soft Microcontroller. The procedure DO\_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. Note that the variable CRC needs to be initialized to zero before the procedure is executed. Each byte of the data is then placed in the accumulator and DO\_CRC is called to update the CRC variable. After all the data has been passed to DO\_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is:

$$CRC = x^8 + x^5 + x^5 + 1$$

For a detailed explanation of the CRC computation, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

#### CRC ASSEMBLY LANGUAGE PROCEDURE Table 1 some season and a solid to a language process of the contract of the c

DO_CRC:	PUSH	ACC	4194	; save the accumulator	
211	PUSH	В	00	; save the B register	
Sin	PUSH	ACC		; save bits to be shifted ; set shift = 8 bits	
	MOV	B,#8		, set stillt = o bits	
CRC_LOOP:	XRL	A,CRC	09	; calculate CRC	
84	RRC	A		; move it to the carry	
a Bu	MOV JNC	A,CRC ZERO		; get the last CRC value ; skip if data = 0	
Shill	XRL	A,#18H	17	; update the CRC value	
LIS I			480	;	
ZERO:	RRC MOV	A CRC,A	480	; position the new CRC ; store the new CRC	
	POP	ACC	15	; get the remaining bits	
	RR PUSH	ACC	08	; position the next bit ; save the remaining bits	
	DJNZ POP	B,CRC_LOC	OP	; repeat for eight bits ; clean up the stack	
	POP POP	B ACC		; restore the B register ; restore the accumulator	
	RET			vidgue meteva of epstlov dullug	ug lamakeV

#### PHYSICAL SPECIFICATIONS

Size See mechanical drawing
Weight 3.3 gms (F5 package)

Humidity 90% RH at 50°C Altitude 10,000 feet

Expected Service Life

DS1991L-F5 10 years at 25°C (150 million transactions - see note 4)

Safety The DS1991 contains a small battery which is a lithium type (DS1991L-F5). These parts should never be incinerated or exposed to fire. Contact the appropriate government agency for any special disposal precautions with regard to lithium-powered devices.

# ELECTRICAL SPECIFICATIONS ABSOLUTE MAXIMUM RATINGS\*

Voltage on any Pin Relative to Ground

Operating Temperature

Storage Temperature

-0.5V to +7.0V

-20°C to +70°C

-20°C to +70°C

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(V <sub>PUP</sub>	=	1.5	to	6.0V,	-20°	to	+70°C)	
-------------------	---	-----	----	-------	------	----	--------	--

				, FUF	The second secon	
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V <sub>IL</sub>	-0.3	11	0.2	Volts	
Input Logic High	V <sub>IH</sub>	1.1	1/	6.0	Volts	
Ouput Logic Low @4mA	V <sub>OL</sub>			0.4	Volts	
Output Logic High	V <sub>OH</sub>		V <sub>PUP</sub>	6.0	Volts	1,2
Input Resistance	R,		500K	7.4	Ohms	3

<sup>\*</sup>V<sub>PUP</sub> = external pull-up voltage

#### AC ELECTRICAL CHARACTERISTICS (-20°C to +70°C)

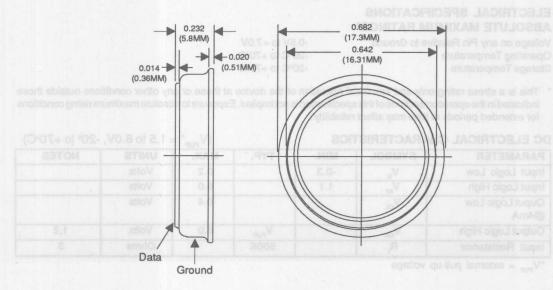
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t <sub>slot</sub>	60	B	120	μS	
Write 1 Low Time	Md B = Mt <sub>LOW1</sub>	. 1	84,8	15	μS	
Write 0 Low Time	t <sub>Lowo</sub>	60	ngn a	120	μS	000
Read Data Valid	en of a t <sub>RDV</sub>		A	15	μS	
Read Data Setup	t <sub>su</sub>	1	DPG-AL	V CRA	μS	6
Frame Sync	t <sub>syc</sub>	1	H878,A	JAX	μS	
Reset Low Time	t <sub>RSTL</sub>	480		000	μS	ethysis trisier
Reset High Time	t <sub>RSTH</sub>	480	A,ORO	VOM	μS	5
Presence Detect High	t <sub>PDH</sub>	15	AGG	60	μS	
Presence Detect Low	t <sub>PDL</sub>	60	DOA	240	μS	

#### NOTES

- 1. All voltages are referenced to ground.
- 2. V<sub>PUP</sub>=external pullup voltage to system supply.
- 3. Input pulldown resistance to ground.
- 4. A transaction is defined here as reading the entire scratchpad memory.
- 5. An additional reset or communication sequence cannot begin until the reset high time has expired.
- 6. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1 µS of this falling edge and will remain valid for 14 µS minimum (15 µS total from falling edge on 1-Wire).

#### **DS1991 TOUCH MULTIKEY**

#### F5 PACKAGE





## DS1992/DS1993 1K-Bit/4K-Bit Touch Memory DS1994 4K-Bit Plus Time Touch Memory

#### **SPECIAL FEATURES**

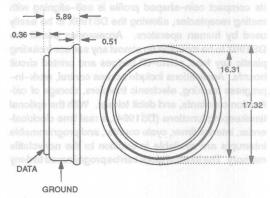
- 4096 bits of read/write nonvolatile memory (DS1993 and DS1994)
- 1024 bits of read/write nonvolatile memory (DS1992)
- 256-bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256—bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Contains real time clock/calendar in binary format (DS1994)
- Interval timer can automatically accumulate time when power is applied (DS1994)
- Programmable cycle counter can accumulate the number of system power-on/off cycles (DS1994)
- Programmable alarms can be set to generate interrupts for interval timer, real time clock, and/or cycle counter (DS1994)
- Write protect feature provides tamper–proof time data (DS1994)
- Programmable expiration date that will limit access to SRAM and timekeeping (DS1994)
- Clock accuracy is better than ±1 minute/month (DS1994)
- Operating temperature range from -20°C to +70°C
- Over 10 years of data retention

#### **COMMON TOUCH MEMORY FEATURES**

- Electronic identification by momentary contact
- Chip—based data carrier compactly stores information
- · Can be accessed while affixed to object
- Economically communicates to host with a single digital signal at 16.6K bits per second
- Standard 16 mm diameter and 1—wire protocol ensure compatibility with Touch Device family
- Coin shape is self-aligning with mating receptacles

- Durable stainless steel case resists environmental hazards
- Unique, factory—lasered, 48 bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing or snap-in flange, spring clip or magnetic holder
- Presence detect signal announces connection to host

#### PIN ASSIGNMENT



(All dimensions shown in millimeters)

#### CONTACTS

Rim Ground Inner Face Data

#### **ACCESSORIES**

DS9092 Touch Memory Probe, Hand=Grip or Panel Mount

DS9093F Touch Memory Key Ring Mount
DS9094F Touch Memory Clip

DS9096 Self-Stick Adhesive Pad DS9098 Surface Mount Retainer

#### ORDERING INFORMATION

DS1992L-F5 10 year data retention, F5 package DS1993L-F5 10 year data retention, F5 package DS1994L-F5 10 year data retention, F5 package

#### DESCRIPTION

The DS1992/DS1993/DS1994 Touch Memory (hereafter referred to as DS199X) is a rugged read/write data carrier that acts as a localized database that can be easilv accessed with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the Touch Memory is attached. Data is transferred serially via the 1-wire protocol which requires only a single data lead and a ground return. The memory is organized into 256-bit pages and data is first written into a page at a time using a 256-bit scratchpad then trasferred to memory for enhanced data integrity. A 48-bit serial number is factory lasered into each DS199X to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS199X to be easily used by human operators. Accessories permit the DS199X to be mounted on almost any surface including plastic key fobs, photo-ID badges and printed circuit boards. Applications include access control, work-inprogress tracking, electronic travelers, storage of calibration constants, and debit tokens. With the optional timekeeping functions (DS1994), a real time clock/calendar, interval timer, cycle counter, and programmable interrupts are available in addition to the nonvolatile memory. The internal clock can be programmed to deny

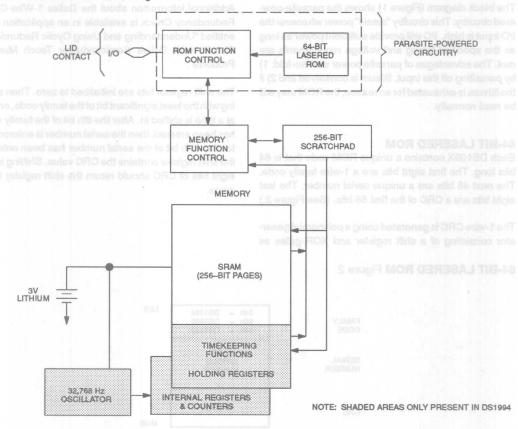
memory access based on absolute time/date, total elapsed time, or the number of accesses. These features allow the DS1994 to be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, interval timer, and event scheduler.

#### **OVERVIEW**

The DS199X has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 1024-bit (DS1992) or 4096-bit (DS1993 and DS1994) SRAM, and 4) timekeeping registers (DS1994). The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands (Figure 6).

#### DS199X BLOCK DIAGRAM Figure 1



#### PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for an reason, the ROM may still be read normally.

#### **64-BIT LASERED ROM**

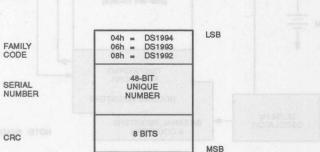
Each DS199X contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as

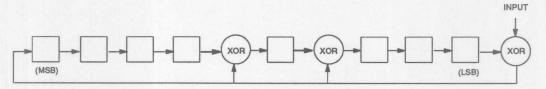
shown in Figure 3. The polynomial is  $X^8 + X^5 + X^4 + 1$ . Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

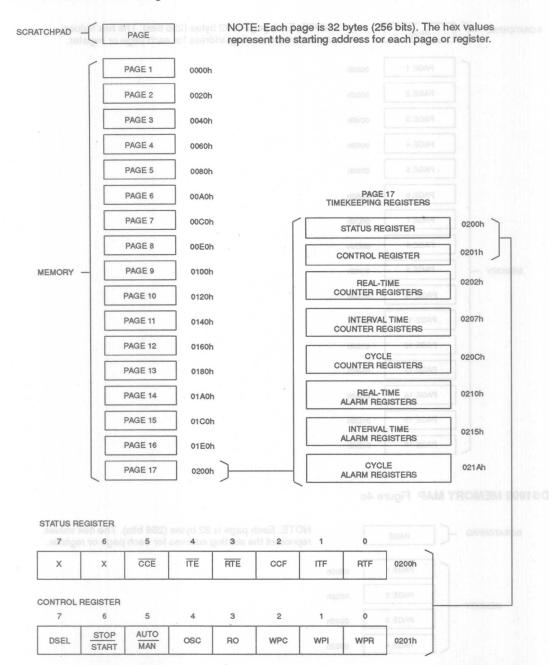
#### 64-BIT LASERED ROM Figure 2



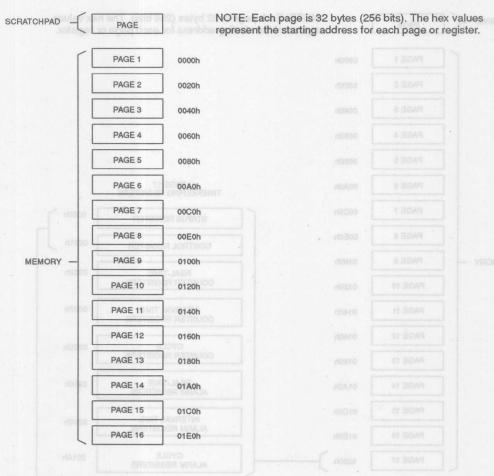
#### 1-WIRE CRC CODE Figure 3



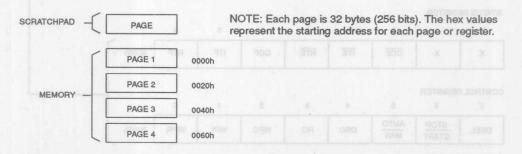
#### DS1994 MEMORY MAP Figure 4a



#### DS1993 MEMORY MAP Figure 4b



#### DS1992 MEMORY MAP Figure 4c



#### **MEMORY**

The memory map in Figure 4 shows a 32-byte page called 'the scratchpad and additional 32-byte pages called memory. The DS1992 contains pages 1 though 4 which make up the 1024-bit SRAM. The DS1993 and DS1994 contain pages 1 through 16 which make up the 4096-bit SRAM. The DS1994 also contains page 17 which has only 30 bytes that contain the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

#### **TIMEKEEPING (DS1994)**

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

#### Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

#### Interval Timer MANAGO MORTOMUS VISONISM

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/MAN bit in the

control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/START bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

#### **Cycle Counter**

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

#### **Alarm Registers**

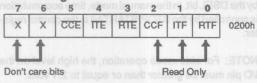
The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)



#### STATUS/CONTROL REGISTERS (DS1994)

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

**Status Register** 



0 RTF Real-time clock alarm flag
1 ITF Interval timer alarm flag
2 CCF Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

RTE Real-time interrupt enable
ITE Interval timer interrupt enable
CCE Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

#### Control Register ( and balled as moded as well

7	6	5	4	3	2	1	0	
DSE	STOP START	AUTO MAN.	osc	RO	WPC	WPI	WPR	0201h

WPR Write protect real-time clock/alarm registers
WPI Write protect interval timer/alarm registers
WPC Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3 RO Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1992/DS1993/DS1994 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4 OSC Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5 AUTO/MAN Automatic/Manual Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/START bit.

6 STOP/START Stop/Start (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7 DSEL Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is  $123\pm2$  ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is  $3.5\pm0.5$  ms.

#### MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

#### **ADDRESS REGISTERS** Figure 5

SETBAM .	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	<b>T7</b>	Т6	T5	T4	ТЗ	T2	T1	ТО
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	Т9	Т8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

#### Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

#### Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

#### Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained

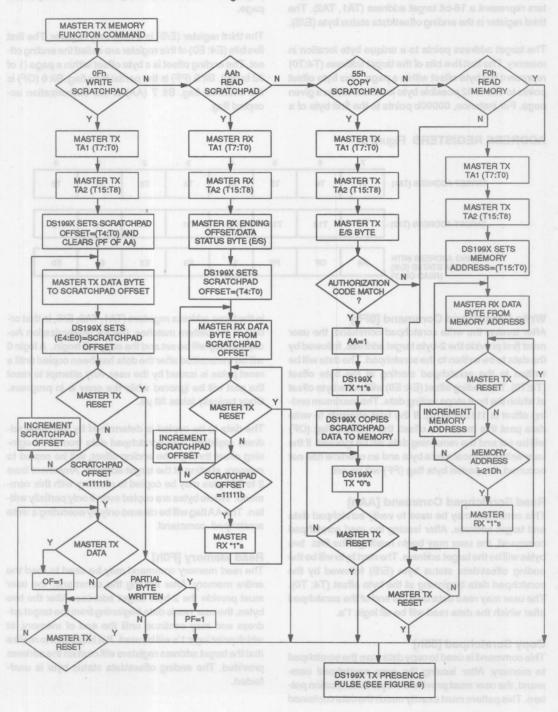
in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the user. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30  $\mu s$ .

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

#### Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

#### **MEMORY FUNCTION FLOW CHART** Figure 6



# 12

### MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
a write proXT bit is s	on Reset	Reset pulse (480–960 μs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
takes plac XThen on	offeringer of the open To	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
ebnam TX notionut y	omam baar bna 00h na baar	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	. 00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX OF	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX "O" olo	"t", may not ldOO then beek to a	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
litate this, «XT device	el oT amiliata 26h sedila	TA1 ) . Mateve eue ani
TX	00h	TA2 AUTHORIZATION CODE
quivalent toXTat show	fluorio lementi 07h w nierio	E/S a Josephia will ovalla a sa savariad X99
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX Dis yla	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX MUST	auz ad of abson 00h sons die	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX seed like a	<128 bytes (DS1992)> <512 bytes (DS1993)> <542 bytes (DS1994)>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

# WRITE PROTECT/PROGRAMMABLE EXPIRATION (DS1994)

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1994 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

#### WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm	Interval Timer Interval Time Alarm	Cycle Counter Cycle Counter Alarm
ss=0026h ) offset=7, flags=0	WPR WPI WPC	WPR WPI WPC	WPR WPI WPC
	RO SE DESER	RO OSC* STOP/START** AUTO/MAN	RO OSC* DSEL

<sup>\*</sup> Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".

#### 1-WIRE BUS SYSTEM

The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS199X behaves as a slave. The exception is when the DS1994 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

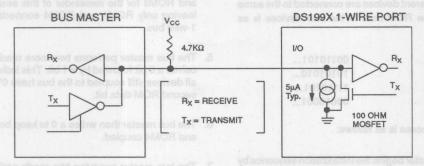
#### HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS199X is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus has a maximum data rate of 16.6K bits per second and requires a pull-up resistor of approximately  $5K\Omega$ .

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480  $\mu$ S, all components on the bus will be reset.

<sup>\*\*</sup> Forced to a logic "0".

# **HARDWARE CONFIGURATION Figure 8**



## TRANSACTION SEQUENCE

The protocol for accessing the DS199X via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

#### INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS199X is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

#### **ROM FUNCTION COMMANDS**

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

#### Read ROM [33h]

This command allows the bus master to read the DS199X's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS199X on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

# Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS199X on a multidrop bus. Only the DS199X that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

# Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

# Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus

#### Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101
ROM2	10101010
ROM3	11110101
ROM4	00010001

The search process is as follows:

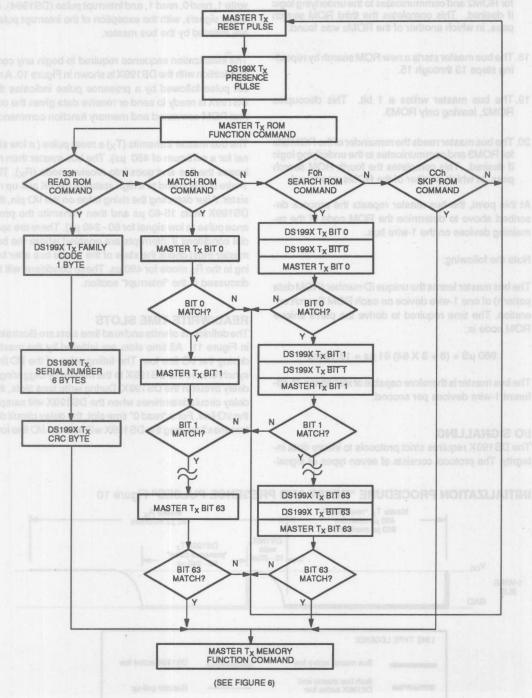
- The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
- The bus master will then issue the search ROM command on the 1-wire bus.
- 3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low, ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a

The data obtained from the two reads of the 3-step routine have the following interpretations:

- There are still devices attached which have conflicting bits in this position.
- All devices still coupled have a 0 bit in this bit position.
- All devices still coupled have a 1 bit in this bit position.
- There are no devices attached to the 1-wire bus.

- The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
- The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
- The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
- The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
- The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
- The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.
- 10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
- The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
- 12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
- 13. The bus master starts a new ROM search by repeating steps 1 through 3.
- 14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
- The bus master executes two read time slots and receives two zeros.
- 16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

# **ROM FUNCTIONS FLOW CHART** Figure 9



pass, in which another of the HOMs was found.

- The bus master starts a new ROM search by repeating steps 13 through 15.
- The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
- 20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

At this point, the bus master repeats the process described above to determine the ROM code of the remaining devices on the 1-wire bus.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960 \mu S + (8 + 3 \times 64) 61 \mu s = 13.16 ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

#### I/O SIGNALLING

The DS199X requires strict protocols to insure data integrity. The protocol consists of seven types of signal-

are initiated by the bus master.

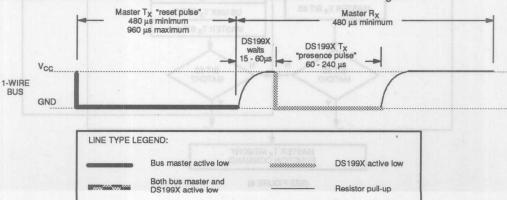
The initialization sequence required to begin any communication with the DS199X is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS199X is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits ( $T_X$ ) a reset pulse (a low signal for a minimum of 480  $\mu$ s). The bus master then releases the line and goes into receive mode ( $R_X$ ). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS199X waits 15-60  $\mu$ s and then transmits the presence pulse (a low signal for 60 - 240  $\mu$ s). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the  $R_X$  mode for 480  $\mu$ s. These conditions will be discussed in the "Interrupt" section.

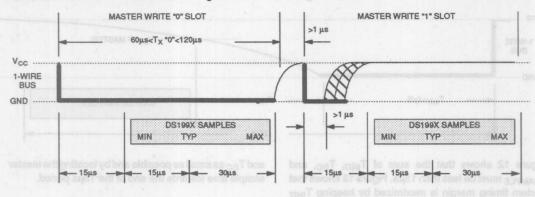
#### **READ/WRITE TIME SLOTS**

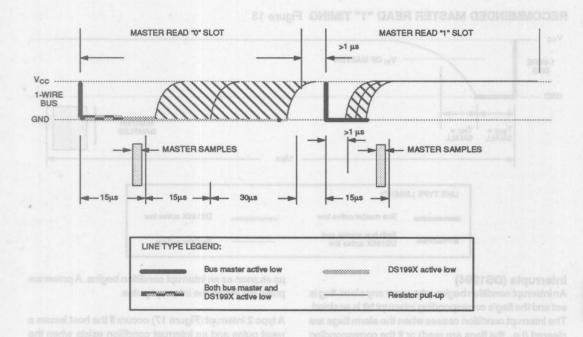
The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS199X to the master by triggering a delay circuit in the DS199X. During write time slots, the delay circuit determines when the DS199X will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS199X will hold the I/O line low.

# **INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES"** Figure 10



# **READ/WRITE TIMING DIAGRAM** Figure 11





# **DETAILED MASTER READ "1" TIMING Figure 12**

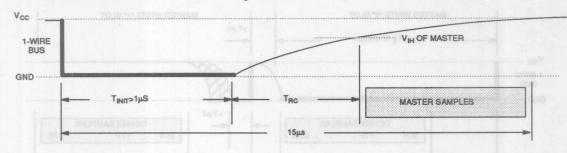
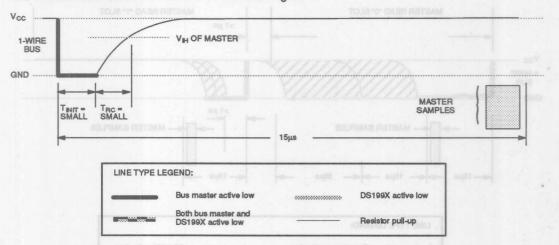


Figure 12 shows that the sum of  $T_{INIT}$ ,  $T_{RC}$ , and  $T_{SAMPLE}$  must be less than 15 $\mu$ s. Figure 13 shows that system timing margin is maximized by keeping  $T_{INIT}$ 

and T<sub>RC</sub> as small as possible and by locating the master sample time towards the end of the 15µs period.

# **RECOMMENDED MASTER READ "1" TIMING** Figure 13



# Interrupts (DS1994)

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled.

On the 1-wire port, the DS1994 responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 14) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960  $\mu$ s to 3840

μs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

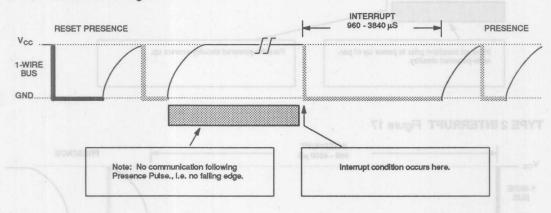
A type 2 interrupt (Figure 17) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960  $\mu s$  to 4800  $\mu s$ . A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected. Special cases exist as follows:

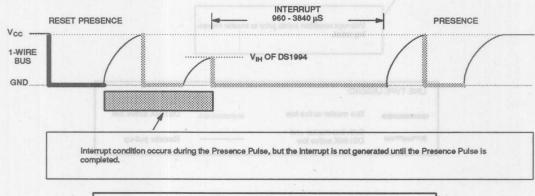
Special Case A (Figure 15): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

Special Case B (Figure 16): If an interrupt condition exists while the parasite-powered circuitry is powered down (i.e., I/O has been low for ≫1s), a type 1 interrupt will occur after the first presence pulse following I/O going high, just as in Special Case A.

# **TYPE 1 INTERRUPT** Figure 14



# TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15



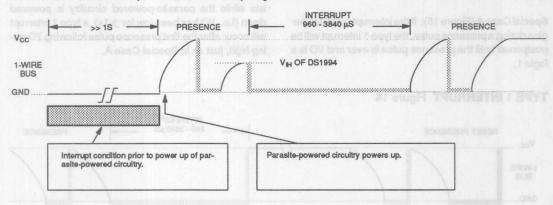
LINE TYPE LEGEND:

Bus master active low

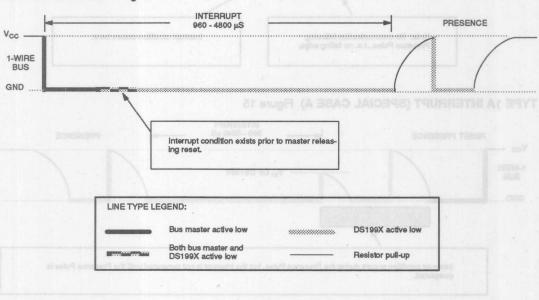
Both bus master and
DS199X active low

Resistor pull-up

# TYPE 1B INTERRUPT (SPECIAL CASE B) Figure 16



# **TYPE 2 INTERRUPT** Figure 17



# PHYSICAL SPECIFICATIONS

Size Weight Humidity Altitude Expected Service Life Safety See mechanical drawing 3.3 grams (F5 package) 90% RH at 50°C 10,000 feet 10 years at 25°C

The DS199X contains a small battery which is a lithium type. These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium—powered devices.

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground Operating Temperature Storage Temperature -0.5V to +7.0V -20°C to 70°C -20°C to +70°C

\* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### DC ELECTRICAL CHARACTERISTICS

(V<sub>PUP</sub>=2.8°C to 6.0V, -20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.2		V <sub>CC</sub> +0.3	V	1
Logic 0	V <sub>IL</sub>	-0.3		+0.8	V /	\\\\1
Output Logic Low @ 1 mA	VoL			0.4	V	11
Output Logic High	V <sub>OH</sub>		V <sub>PUP</sub>	6.0	V	1, 2

# CAPACITANCE

 $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	CIN/OUT			800	pF	6

# AC ELECTRICAL CHARACTERISTICS

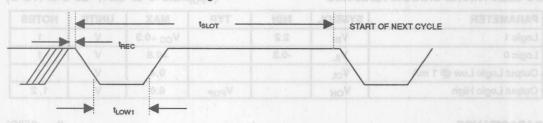
(-20°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	tslot	60		120	μѕ	1777
Write 1 Low Time	t <sub>LOW1</sub>	1		15	μѕ	
Write 0 Low Time	t <sub>L</sub> owo	60		120	μs	
Read Data Valid	t <sub>RDV</sub>			15	μs	
Read Data Setup	tsu	1			μs	5
Interrupt	t <sub>INT</sub>	960		4800	μs	8
Recovery Time	tREC	1			μs	
Reset Time High	trsth	480			μs	4
Reset Time Low	tRSTL	480		960	μs	7
Presence Detect High	t <sub>PDHIGH</sub>	15		60	μs	
Presence Detect Low	tpDLOW	60		240	μs	

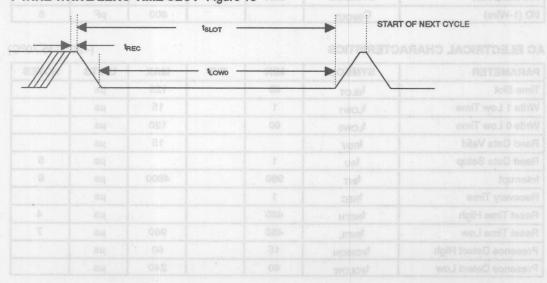
#### NOTES

- 1. All voltages are referenced to ground.
- 2. V<sub>PUP</sub> = external pull-up voltage.
- 3. Input load is to ground.
- 4. An additional reset or communication sequence cannot begin until the reset high time has expired.
- 5. Read data setup time refers to the time the host must pull the 1-wire bus low to read a bit. Data is guaranteed to be valid within 1 μs of this falling edge and will remain valid for 14 μs minimum. (15 μs total from falling edge on 1-wire bus.)
- 6. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V<sub>CC</sub>, 5 μs after power has been applied, the parasite capacitance will not affect normal communications.
- DS1994 requires a maximum low time for a reset pulse of 960 µs because of the possibility of an interrupt occuring.
- 8. DS1994 only.

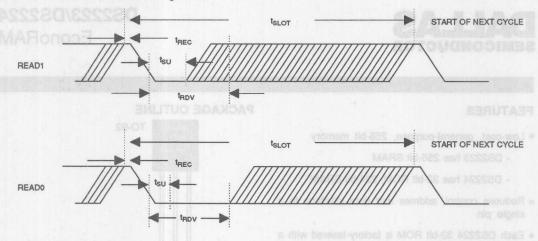
# 1-WIRE WRITE ONE TIME SLOT Figure 18



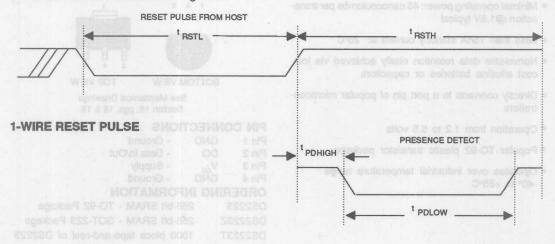
# 1-WIRE WRITE ZERO TIME SLOT Figure 19



# 1-WIRE READ TIME SLOTS Figure 20



# 1-WIRE PRESENCE DETECT Figure 21





DS2223/DS2224 EconoRAM

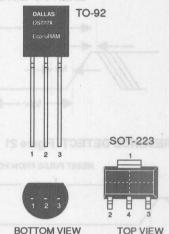
#### **FEATURES**

- · Low-cost, general-purpose, 256-bit memory
  - DS2223 has 256-bit SRAM
  - DS2224 has 32-bit ROM, 224-bit SRAM
- Reduces control, address and data interface to a single pin
- Each DS2224 32-bit ROM is factory-lasered with a unique serial number
- Minimal operating power: 45 nanocoulombs per transaction @1.5V typical
- Less than 15nA standby current at 25°C
- Nonvolatile data retention easily achieved via lowcost alkaline batteries or capacitors
- Directly connects to a port pin of popular microcontrollers
- Operation from 1.2 to 5.5 volts
- Popular TO-92 plastic transistor package
- Operates over industrial temperature range -40° to +85°C

#### DESCRIPTION

The DS2223 and DS2224 EconoRAMs are fully static, micro-powered, read/write memories in low-cost TO-92 packages. The DS2223 is organized as a serial 256 x 1 bit static read/write memory. The DS2224's first 32 bits are lasered in with a unique ID code at the time of manufacture; the remaining 224 bits are static read/write memory. Signaling necessary for reading or writing is reduced to just one interface lead.

### PACKAGE OUTLINE



See Mechanical Drawings Section 16, pgs. 18 & 19

256-bit SRAM - TO-92 Package

#### PIN CONNECTIONS

DS2223

Pin 1	GND	- Ground
Pin 2	DQ	- Data In/Out
Pin 3	Vcc	- Supply
Pin 4	GND	- Ground

#### ORDERING INFORMATION

DS2223Z	256-bit SRAM - SOT-223 Package
DS2223T	1000 piece tape-and-reel of DS2223
DS2223Y	2500 piece tape-and-reel of DS2223Z
DS2224	32-bit serial number (ROM), 224-bit SRAM - TO-92 Package
DS2224Z	32-bit serial number (ROM), 224-bit SRAM - SOT-223 Package
DS2224T	1000 piece tape-and-reel of DS2224
DS2224Y	2500 piece tape-and-reel of DS2224Z
DS2224-XXX	Portion of ROM code has a custom code -TO-92 Package
DS2224Z-XXX	(Portion of ROM code has a custom

code-SOT-223 Package

DS2224T-XXX 1000 piece tape-and-reel of DS2224-XXX

DS2224Y-XXX 2500 piece tape-and-reel of DS2224Z-XXX

# **OPERATION**

All communications to and from the EconoRAM are accomplished via a single interface lead. EconoRAM data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction. Note that once a specific transaction has been initiated, either a read or a write, it must be completed for all memory locations before another transaction can be started.

#### WRITE TIME SLOTS

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one-microsecond recovery time between individual write cycles.

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot. (See Figure 1.)

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot. (See Figure 2.)

#### **READ TIME SLOTS**

The host generates read time slots when data is to be read from the EconoRAM. A read time slot is initiated when the host pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the EconoRAM is then valid for the next 14 microseconds minimum. The host therefore must stop driving the DQ pin to read its state one to 15 microseconds from the start of the read slot (see Figure 3). At some point between 15 and 60 microseconds into the read time slot, the DQ pin will pull back high via the external pullup resistor (30 microseconds typically). All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

#### **COMMAND WORD**

The command word consists of 8 bits that are transmitted LSB first from the host to the EconoRAM with write time slots (see Figure 4). The first bit of the command word is set to a logic 1 level. This indicates to the EconoRAM that a command word is being written. The next two bits are the select bits which denote the physical address of the EconoRAM that is to be accessed (set to 00 currently). The remaining five bits determine whether a read or a write operation

is to follow. If a write operation is to be performed, all five bits are set to a logic 1 level. If a read operation is to be performed, any or all of these bits are set to a logic 0 level. All eight bits of the command word are transmitted to the EconoRAM with a separate time slot for each bit.

#### READ OR WRITE TRANSACTION

Read or write transactions are performed by initializing the EconoRAM to a known state, issuing a command word, and then generating the time slots to either read EconoRAM contents or write new data. Each transaction consists of 264 transaction time slots. Eight are for the command word and 256 are for the data bits being transferred. (See Figure 5.) Once a transaction is started, it must be completed for all memory bits before another transaction can begin.

To initially set the EconoRAM into a known state, 264 Write Zero time slots must be sent to it. These Write Zero time slots will not corrupt the data in the EconoRAM since a command word has not been written. This operation will increment the address pointer internal to the EconoRAM to its maximum count value. Upon reaching this maximum value, the EconoRAM will ignore all additional Write Zero time slots issued to it and the internal address pointer will remain locked at the top count value. This condition is removed by the reception of a Write One time slot, typically the first bit of a command word.

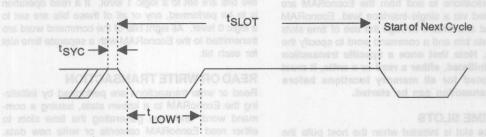
Once the EconoRAM has been set into a known state, the command word is transmitted to the EconoRAM with eight write time slots. This resets the address pointer internal to the EconoRAM and prepares it for the appropriate operation, either a read or a write.

After the command word has been received by the EconoRAM, the host initiates the appropriate data transfer operation. In the case of a read transaction, the host issues 256 read time slots. In the case of a write transaction, the host issues 256 write time slots. As stated previously, these time slots, either read or write, cannot be intermixed within the same transaction cycle.

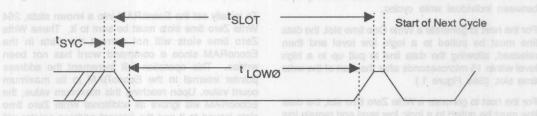
#### HOST SYSTEM INTERFACE

The host system must have an open drain driver with a pull-up resistor of approximately 5K ohms to system  $V_{\infty}$  on the data signal line. The EconoRAM has an internal open-drain driver with a 500K ohm pull-down resistor to ground (see Figure 8). The open-drain driver allows the EconoRAM to be powered by a small standby energy source, such as a single 1.5 volt alkaline battery, and still have the ability to produce CMOS/TTL output levels. The pulldown resistor holds the DQ pin at ground when the EconoRAM is not connected to the host.

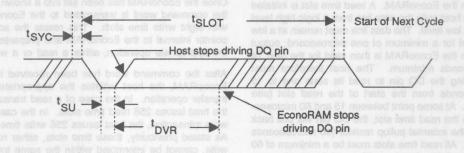
# WRITE ONE TIME SLOT Figure 1



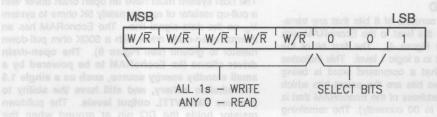
# WRITE ZERO TIME SLOT Figure 2



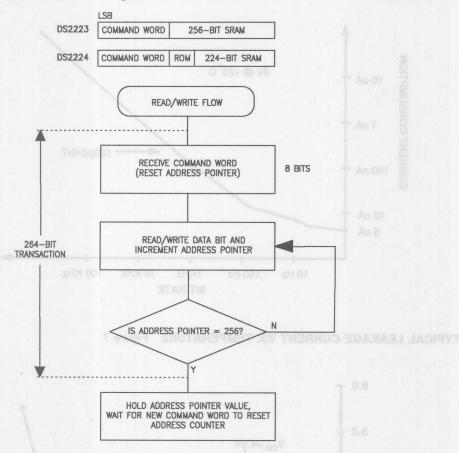
# READ DATA TIME SLOTS Figure 3



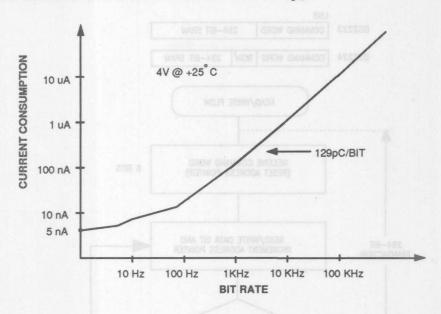
# COMMAND WORD Figure 4



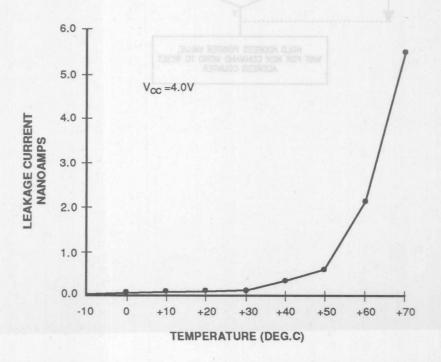
# READ/WRITETRANSACTION Figure 5



TYPICAL CURRENT CONSUMPTION VS. BIT RATE Figure 6



# TYPICAL LEAKAGE CURRENT VS. TEMPERATURE Figure 7



## **ABSOLUTE MAXIMUM RATINGS**

5 to +6.5 Volts 0°C to +85°C
5°C to +125°C

# RECOMMENDED DC OPERATING CONDITIONS

(DS2223/DS2224 -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Pin	DQ	-0.5		6.0	Volts	les tomes
Supply Voltage	V <sub>cc</sub>	1.2		5.5	Volts	1

# DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V<sub>cc</sub>= 2.0 - 5.5V, -40° to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	OI VIL	-0.5	0.4	0.8	Volts	1V BBQ
Input Logic High	V <sub>IH</sub>	V <sub>cc</sub> -0.5	wad	6.0	Volts	1V stsQ
Sink Current	31 15	00 1	2		mA	4 660
Output Logic Low	V <sub>oL</sub>		uel	0.4	Volts	148 msO,
Output Logic High	V <sub>OH</sub>	V <sub>PUP</sub>	oval	5.5	Volts	1,2
Input Resistance	I <sub>R</sub>		500K		Ohms	3
Operating Current	lop		bnuovo c	36	nC	5
Standby Current	I <sub>STBY</sub>	n supply:	0.2	15	nA	6

# DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V<sub>cc</sub>= 1.4V ± 10%, -40° to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V <sub>II</sub>	-0.5		0.2	Volts	1
Input Logic High	V <sub>IH</sub>	1.0 mg/l	BOARR	6.0	Volts	TITEOF
Sink Current	I,	1	2		mA	7
Output Logic Low	VoL		apV <u>A</u>	0.4	Volts	4
Output Logic High	V <sub>OH</sub>	V <sub>PUP</sub>		5.5	Volts	1,2
Input Resistance	I <sub>B</sub>		500K		Ohms	3
Operating Current	IOP			36	nC	5
Standby Current	ISTRY	-0	12	25	nA	6

# **ACELECTRICAL CHARACTERISTICS**

 $(V_{cc} = 1.4V \pm 10\%, -40^{\circ} to 85^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t <sub>slot</sub>	70		9	μS	gnested
Data Valid Read	t <sub>DVR</sub>	1		15	μS	
Data Valid Write 1	t <sub>Low1</sub>	1		15	μS	
Data Valid Write Ø	Lowe	60	ATING CC	15	μS	IRCOM
Data Setup Time	t <sub>su</sub>	1	LOSEN	14	μS	MARAR
Frame Sync Time	t <sub>syc</sub>	1			μS	MA ENG

# **ACELECTRICAL CHARACTERISTICS**

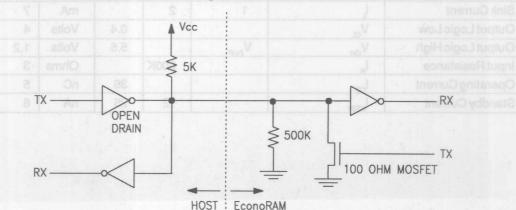
 $(V_{cc} = 5V \pm 10\%, -40^{\circ} to +85^{\circ}C)$ 

	, 60 –							
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES		
Time Slot	t <sub>slot</sub>	60	TORIN		μS	MARAG		
Data Valid Read	t <sub>DVR</sub>	a 0 1		15	μS	Input Logic		
Data Valid Write 1	Lowi 8.0-	/ 1	10	15	μS	Input Logic		
Data Valid Write Ø	t <sub>Lowø</sub>	60		15	μS	Sink Cum		
Data Setup Time	t <sub>su</sub>	1		14	μS	Output La		
Frame Sync Time	t <sub>syc</sub>	v / 1	180	V	μS	Output Lo		

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. V<sub>PUP</sub> = external pull-up voltage to system supply.
- 3. Input pull-down resistance to ground.
- 4. @  $V_{OI} = 0.4V$ .
- 5. 36 nanocoulombs per 264 time slots @ 1.5V (see Figure 6).
- 6. See Figure 7 for typical values over temperature.
- 7. @ V<sub>OL</sub>= 0.2 V.

# HOST TO EconoRAM INTERFACE Figure 8



### **APPLICATION EXAMPLES**

#### **Using Backup Capacitors**

EconoRAMs are extremely conservative with power. Data can be retained in these small memories for as long as a month using the energy stored in a capacitor. Data is retained as long as the voltage on the V<sub>CC</sub> pin of the EconoRAM (V<sub>CAP</sub>) is at least 1.2 volts. A typical circuit is shown in Figure 9.

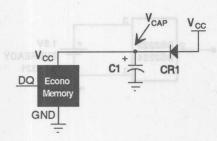
When  $V_{cc}$  is applied, capacitor C1 is charged and the EconoRAM receives power directly from  $V_{cc}$ . After power is removed, the diode CR1 prevents current from leaking back into the system, keeping the capacitor charged.

In the standby mode, the EconoRAM typically consumes only 12nA at 25°C. However, the power-down

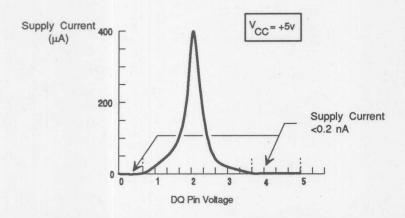
process of the system can cause a slightly higher current drain. This is due to the fact that as system power ramps down, the signal attached to the DQ pin of the EconoRAM transitions slowly through the linear region, while the V<sub>CAP</sub>voltage remains at its initial value. While in this region, the part draws more current as a function of the DQ pin voltage (see Figure 10).

The data retention time can be estimated with the aid of Figure 11. In this figure, the vertical axis represents the value of the capacitor C1; the horizontal axis is the data retention time in hours. The two curves represent initial  $V_{\text{CAP}}$  voltages of 3 and 5 volts. These curves are based on the assumption that the time the DQ pin is in the linear region is less than 100 mS.

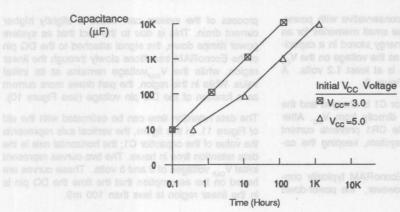
# SUGGESTED CIRCUIT Figure 9



# ICC VS. DQ VOLTAGE Figure 10

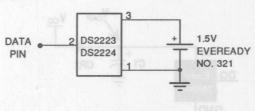


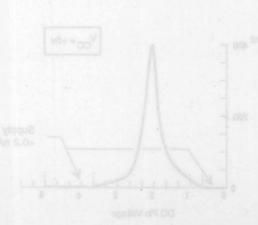
DATA RETENTION TIME VS. CAPACITANCE Figure 11



# **Using Battery Backup**

14mA-Hr => 144 million transactions







# DS2400 Silicon Serial Number

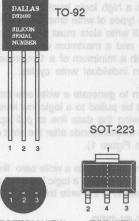
#### **FEATURES**

- Unique 48-bit silicon serial number gives 10<sup>14</sup> combinations
- · Factory lasered and tested, no two parts alike
- 8-bit cyclic redundancy check ensures error-free reading
- 8-bit model number references DS2400 communications requirements to system
- Presence detect indicates to the system when first contact is made
- Low-cost TO-92 package and optional surface mount option
- Reduces control, address, and data to a single pin
- Zero standby power required
- Directly connects to one port pin for microprocessor interface
- Pulse width measurement determines 1's or 0's
- Power derived from data line
- Applications
  - PCB Identification
- Local Area Network I.D.
- Software Protection
- Operates over industrial temperature range
   -40° to +85°C

#### DESCRIPTION

The DS2400 Silicon Serial Number contains an 8-bit family code, a unique 48-bit serial number, and an 8-bit cyclic redundancy check value embedded in silicon. Signaling necessary for reading or writing is reduced to just one interface lead. The familiar TO-92 package provides a small, low-cost enclosure. Power for reading and writing is derived from the data line itself with no need for an external power source.

# PIN DESCRIPTION



BOTTOM VIEW

TOP VIEW

See Mechanical Drawings Section 16, pgs. 18 & 19

# PIN NAMES

Pin 1 Ground

Pin 2 Data (DQ)

Pin 3 No Connect

Pin 4 Ground

#### ORDERING INFORMATION

DS2400 TO-92 Package

DS2400Z SOT-223 Surface Mount Package

DS2400T 1000 piece tape-and-reel of DS2400

DS2400Y 2500 piece tape-and-reel of DS2400Z

DS2400-XXX Portion of serial number has a

custom code-TO-92 Package

DS2400Z-XXX Portion of serial number has a custom code -SOT 223 Package

DS2400T-XXX 1000 piece tape-and-reel of

DS2400-XXX

DS2400Y-XXX 2500 piece tape-and-reel of DS2400Z-XXX

#### **OPERATION**

All communication to and from the DS2400 Silicon Serial Number is accomplished via a single interface lead. Data contained within the DS2400 is accessed through the use of time slots and a 1-Wire protocol. Power to the part is derived from the high going pulse at the beginning of a write or read time slot.

#### WRITE TIME SLOTS

A write time slot is initiated when the system pulls the data line from a high logic level to a low logic level. There are two types of write time slots: write one and write zero. All write slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond sync pulse between individual write cycles.

For the system to generate a write one time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (see Figure 1).

For the system to generate a write zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (see Figure 2).

#### **READ TIME SLOTS**

The system generates read time slots when data is to be read from the DS2400. A read time slot is initiated when the system pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of 1 microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the DS2400 data must be read by the system within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (see Figure 3). All read time slots must be a minimum of 60 microseconds in duration and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond sync pulse between individual read time slots.

# 1-WIRE PROTOCOL

To communicate with the DS2400 a specific protocol is utilized. The 1-Wire protocol consists of four separate states which are used to reset the device, issue a command word, read the type identifier number, and read the unique silicon serial number and CRC byte (see Figure 4).

To initially set the DS2400 into a known state, a reset pulse must be sent to it. The reset pulse is a logic low

generated by the system which must remain low for a minimum of 480 microseconds and then be followed by a 480 microsecond logic high level (see Figure 5). During this 480 microsecond high time the DS2400 will assert a presence detect signal. This signal is generated by the DS2400 and consists of a logic low level which is held for a maximum of 240 microseconds and minimum of 60 microseconds. This signal can be used to detect that a DS2400 is attached to the 1-wire interface after the issuance of a reset command.

Once the DS2400 has been set into a known state, the command word is transmitted to the DS2400 with eight write time slots. The command word for the DS2400 is a hexadecimal **0F**.

Upon recognition of the command word, the DS2400 is ready to respond to the next eight read time slots with the type identifier number. This number is a hexadecimal **01**.

After the system receives the type identifier number, the DS2400 is ready to output the unique 48-bit serial number contained within the device. The system must issue 48 read time slots to retrieve this number. Following the 48-bit serial number is an 8-bit cyclic redundancy check value. This CRC value has been calculated over the type identifier and serial number (56 bits) and is lasered into the part at the time of manufacture. To read the CRC value the system must issue eight read time slots. To stop reading at any time the system can issue a reset pulse.

## **CRC GENERATION**

To validate that the transmitted data from the DS2400 has been received correctly by the system, a comparison of the system-generated CRC and the received DS2400 CRC must be made. If the two CRC values match, the transmission was error-free. An example of how to generate the CRC using software is shown in Table 1. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO\_CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC variable. After all the data has been passed to DO CRC, the variable CRC will contain the result. For a detailed explanation of the CRC computation, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

# RECOMMENDED SYSTEM INTERFACE

The system must have an open drain driver with a pullup resistor of approximately 5K ohms to Vcc on the data signal line. The DS2400 has an internal open drain driver with a 500K ohm pulldown resistor to ground. The pulldown resistor holds the data input pin at ground potential when the DS2400 is not connected to a 1-Wire interface (see Figure 6).

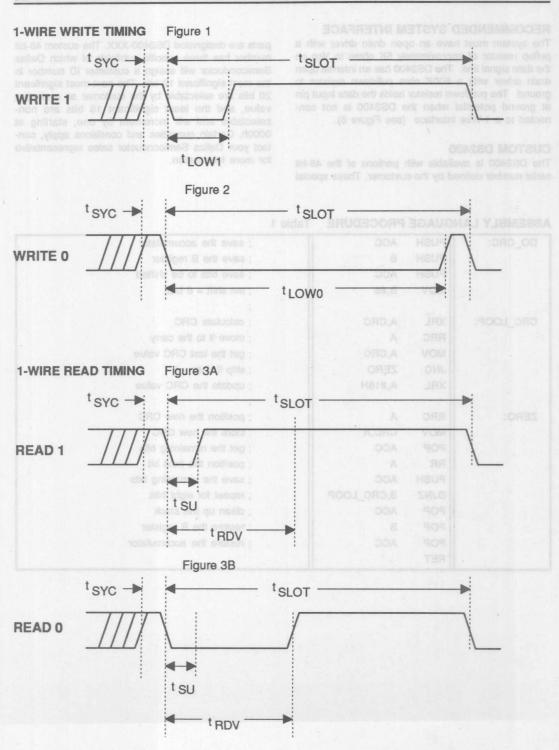
#### **CUSTOM DS2400**

The DS2400 is available with portions of the 48-bit serial number defined by the customer. These special

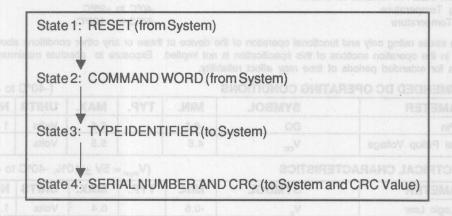
parts are designated DS2400-XXX. The custom 48-bit number has three specific subfields of which Dallas Semiconductor will assign a customer ID number in the most significant 12 bits. The next most significant 20 bits are selectable by the customer as a starting value, and the least significant 16 bits are non-selectable and will increment by one, starting at 0000h. Certain quantities and conditions apply, contact your Dallas Semiconductor sales representative for more information.

### ASSEMBLY LANGUAGE PROCEDURE Table 1

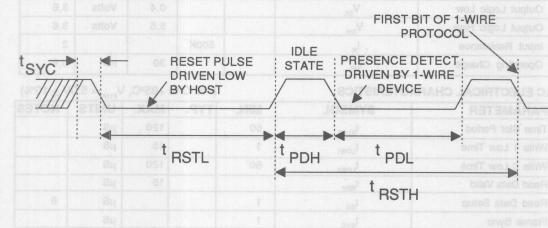
DO_CRC:	PUSH	ACC		; save the accumulator	
	PUSH	В		; save the B register	
	PUSH	ACC		; save bits to be shifted	
	MOV	B,#8	VOJI -	; set shift = 8 bits	
				i	
CRC_LOOP:	XRL	A,CRC		; calculate CRC	
	RRC	A		; move it to the carry	
	MOV	A,CRC		; get the last CRC value	
	JNC	ZERO		; skip if data = 0	
	XRL	A,#18H		; update the CRC value	
			tous! -	SYC - M - SYC	
ZERO:	RRC	A		; position the new CRC	
	MOV	CRC,A		; store the new CRC	
	POP	ACC		; get the remaining bits	
	RR	A		; position the next bit	
	PUSH	ACC		; save the remaining bits	
	DJNZ	B,CRC_LOOP		; repeat for eight bits	
	POP	ACC		; clean up the stack	
	POP	В		; restore the B register	
	POP	ACC		; restore the accumulator	
	RET			,	



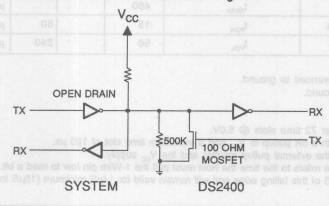
# 1-WIRE PROTOCOL Figure 4



# **RESET PULSE/PRESENCE DETECT** Figure 5



# RECOMMENDED SYSTEM TO DS2400 INTERFACE Figure 6



# **ABSOLUTE MAXIMUM RATINGS\***

Voltage On Data Pin Relative to Ground Operating Temperature Storage Temperature

-0.5 to +7V -40°C to +85°C -55°C to +125°C

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5	וחבעבוו	5.5	Volts	1
External Pullup Voltage	V <sub>cc</sub>	4.5		5.5	Volts	

### DC ELECTRICAL CHARACTERISTICS

 $(V_{PUP} = 5V \pm 10\%, -40^{\circ}C \text{ to } +85^{\circ}C)$ 

			101			
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V <sub>IL</sub>	-0.5		0.4	Volts	1,6
Input Logic High	V <sub>IH</sub>	3.0	5.0	5.5	Volts	1,6,7
Sink Current	l a	-1.0	ретвот	SENCE	mA	4,6
Output Logic Low	V <sub>oL</sub>			0.4	Volts	3,6
Output Logic High	V <sub>OH</sub>			5.5	Volts	3,6
Input Resistance	I <sub>R</sub>		500K		E-FH-	2
Operating Charge	I DP STATE	HSE .	ESET PI	30	nC	5,6

#### **AC ELECTRICAL CHARACTERISTICS**

(-40°C to +85°C, V<sub>evo</sub> = 5.0V + 10%)

		( To a to to a to a pup and in a to a				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t <sub>slot</sub>	60		120	μS	
Write 1 Low Time	t <sub>LOW1</sub>	1 1	- Properties	15	μS	
Write 0 Low Time	t <sub>LOW0</sub>	60	2101	120	μS	
Read Data Valid	t <sub>RDV</sub>			15	μS	
Read Data Setup	t <sub>su</sub>	1			μS	8
Frame Sync	t <sub>syc</sub>	1			μS	
Reset Low Time	t <sub>RSTL</sub>	480	Man no	ranov	μS	internaci
Reset High Time	t <sub>RSTH</sub>	480			μS	
Presence Detect High	t <sub>PDH</sub>	15		60	μS	
Presence Detect Low	t <sub>PDL</sub>	60		240	μS	

#### NOTES:

- 1. All voltages are referenced to ground.
- 2. Input is pulled to ground.
- 3. @1 mA.
- 4. @  $V_{OUT} = 0.4V$ .
- 5. 30 nanocoulombs per 72 time slots @ 5.0V.

- 6.  $@V_{cc} = 5.0$  volts with a 5K pullup to  $V_{cc}$  and a maximum time slot of 120  $\mu$ s.

  7.  $V_{IH}$  is a function of the external pullup resistor and the  $V_{cc}$  supply.

  8. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1µS of this falling edge and will remain valid for 14µS minimum (15µS total from falling edge on 1-Wire).

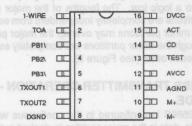


# DS2569S Touch/Proximtiy Memory Chip

#### **FEATURES**

- · Identification by touch contact or wireless link
- 512-bit read/write data memory
- 1-Wire touch pin for programming and reading all configuration and data memory
- Low-level input signal automatically trips a selfclocked output pin for modulating a wireless transmitting device (150-19,200 Hz)
- 3 pushbutton input pins manually trip the output pin to send different partitions of data memory
- Data transmissions are time-slotted to allow multiple devices to be read in the same field
- Laser-trimmed input receiver processes signals as small as 10 mVp-p
- Less than 2μA of standby current enables long battery life
- 64-bit ROM provides a unique, unalterable serial number via the 1-Wire pin
- Chip architecture is compatible with Dallas Semiconductor 1-Wire Touch Protocol

### PIN DESCRIPTION



16-PIN SOIC (300 MIL)

See Mechanical Drawings Section 16, pg. 6

#### PIN NAMES

PIN NAMES	
1-WIRE	1-Wire interface port
TOA	Time out adjust
PB1-3\	Pushbutton inputs; active low
TXOUT1	Transmit data output 1
TXOUT2	Transmit data output 2
M+, M-	Differential receiver input
ACT	Device activity output
CD	Carrier detect; active high
TEST	Test function; leave this pin open
DGND	Digital ground
DVCC	Digital supply
AVCC	Analog supply
AGND	Analog ground

# 12

#### DESCRIPTION

The DS2569S is a 512-bit serial memory intended for 1-Wire touch or wireless identification applications. Data transmissions are triggered either by a low-level input signal sensed by an on-chip receiver or by a logic low on any of the pushbutton inputs. The memory is organized as three128-bit minor partitions and one 512-bit major partition which can overlap the other three. The length of each partition may specified to be any value less than the

maximum. Data is clocked out of the major partition onto the TXOUT1 pin using either the input signal or an on-chip clock source. The three minor partitions clock data out with the internally generated clock onto the TXOUT1/TXOUT2 pins when the proper levels are presented to PB1\, PB2\or PB3\. The configuration options and data memory can be programmed and read using the 1-Wire interface pin.

#### **MEMORY ORGANIZATION**

The DS2569S contains a serial read/write memory that is organized into 4 sections: a major partition up to 512 bits and three separate minor partitions, each up to 128 bits long. The exact length of each memory is programmed by control bits in the configuration register which is accessed through the 1-WIRE pin. The major partition data is transmitted out the TXOUT1 pin when triggered by reception of a low-level signal at M+ and M-as described later. Data in a minor partition is transmitted when a corresponding pushbuttion input pin (PB1-3V) is pulled to a logic low. The lengths of the major and minor partitions are completely independent from each. Any or all minor partitions may overlap the major partition, although the minor partitions are completely separate from each other (see Figure 2).

# WIRELESS TRANSMITTER OPERATION CW MODE

If the DS2569S is configured in the continuous wave (CW) mode, data in the major partition is clocked out the TXOUT1 pin using the input signal present at M+ and M-. Data in all cases is transmitted in the NRZ data format (i.e., data in valid for the entire clock period) and LSB first. A clock edge occurs on every positive signal transition of M+ relative to M-. This clock signal is fed to a programmable divider (N=1-512) whose output is used to clock major partition data. The DS2569S will cycle through the major partition 1 time and then will pause for a pseudo-random number (4 to 11) of partition cycles before restarting the data output. This random timeout scheme allows multiple devices to be read even though

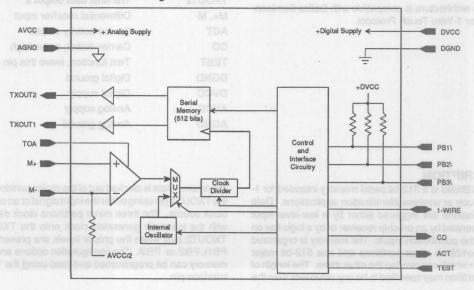
they are both in close proximity to each other. After 5 seconds from being triggered, the data output is disabled for a minimum of 30 seconds. When the 30 seconds have expired, the DS2569S can be retriggered for a new transaction only if the input signal at M+, M- has gone away for more than 250 usec, although this time can be increased by attaching an external capacitor on the TOA pin according to the following equation:

Time out period =  $C/(1.5 \times 10^{-7})$  where the period is in Seconds and C is in Farads

# WIRELESS TRANSMITTER OPERATION - SS MODE

When the DS2569S is configured in single-shot (SS) mode and at least one cycle is presented to M+ and M-, data is output onto the TXOUT1 pin using the internally generated clock. This clock is configurable over a range of frequencies from 150Hz to 19200Hz as shown in Table 3. The DS2569S will cycle through the major partition one time and then pause for a pseudorandom number (4 to 11) of partition cycles. If a signal is detected during the 4-11 pause time, the DS2569S will transmit another 1 on, 4-11 off pattern. This operation continues until the input signal disappears or the 5 second timeout expires as in the CW mode (with the resultant 30 second transmit disable). The input signal must also disappear for at least 250 usec to be retriggered, adjustable via the TOA pin.

# DS2569S BLOCK DIAGRAM Figure 1



#### **PUSHBUTTON OPERATION**

When any of the pushbutton inputs (PB1-3\) are pulled to a logic 0, data in a minor partition is output onto the TXOUT1 pin using the internally generated clock, irregardless of the CW/SS selection. The entire data of a minor partition is transmitted 4 times; the DS2569S then waits for that input to return high. When the pushbutton input is returned high, the minor partition data will be transmitted 4 more times, except that the data will be complemented. This positive-edge detection is buffered

and may occur during the initial 4 passes through the partition. Additionally, the next low/high sequence is buffered to allow for "double clicking" of the push button. The push button inputs are debounced which requires that successive negative edges be separated by at least 80 usec. Pushbutton operation takes precedence over any data transmission triggered by a signal at M+ and M-. Each pushbutton input activates a specific partition as shown in Table 1.

#### TXOUT1/2 CLOCK SOURCE Table 1

PB3\	PB2\	PB1\	PARTITION	MODE	TXOUT1/TXOUT2 CLOCK
1	1	881 1	MAJOR	CW	Derived from received signa
1	1	1	MAJOR	SS	Internal
X	X	0	MINOR 1	CW/SS	Internal
X	0	1	MINOR 2	CW/SS	Internal
0	1	BST MALLISE	MINOR 3	CW/SS	Internal

#### MAJOR PARTITION LASERABLE BITS

The first 96 bits (bits 0-95) of the major partition serial memory can be optionally programmed by the laser at the factory. Contact the marketing department for details about custom programming services. Otherwise, these bits will behave as normal read/write static memory.

#### **TXOUT2 OUTPUT**

The DS2569S offers a second data output called TXOUT2. The TXOUT2 transmits the same data as TXOUT1 at the start of a transmission; however TXOUT2 only cycles through the active partition for 4 times. TXOUT2 goes then to an inactive state (low) until retriggered by a new signal at M+, M- or any of the pushbutton inputs.

#### CARRIER DETECTION

When a valid signal is present at the M+ and M- receiver inputs, the CD (Carrier Detect) pin will transition high. The CD pin will remain high until the input signal disappears. Internal filtering integrates the input signal over several cycles before activating CD.

#### **ACTIVITY PIN**

The activity pin goes high whenever the any of the memory partitions are being cycled.

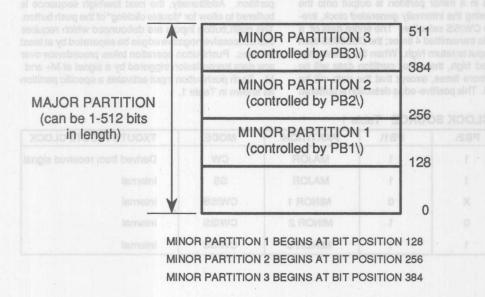
#### **FRESHNESS SEAL**

The DS2569 can be placed into a very-low power mode by using the freshness seal bit in the configuration register. If this bit is set to a 1, the internal power supply to the input receive opamp is disconnected, minimizing current consumption (all other circuitry remains powered). Clearing the freshness seal bit to a 0 reactivates the comparator. This feature is intended to conserve battery power when a part using the DS2569S is not in actual use (i.e., stored in inventory).

#### 1-WIRE INTERFACE

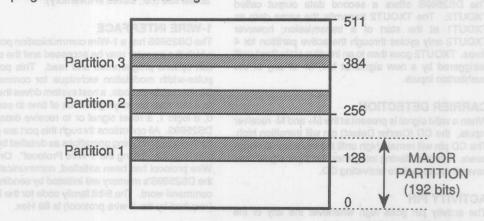
The DS2569S has a 1-Wire communication port through which the memory may be accessed and the configuration options programmed and read. This port uses a pulse-width modulation technique for communication. Similiar to Morse code, a host system drives the input pin to a low state for varying periods of time to send a logic 0, a logic 1, a reset signal or to receive data from the DS2569S. All operations through this port are preceded by the logic and timing operations as detailed by Application Note 23, "Using the 1-Wire Protocol". Once the 1-Wire protocol has been satisfied, communications with the DS2569S's memory are initiated by sending a 24-bit command word. The 8-bit family code for the DS2569S (required by the 1-wire protocol) is 69 Hex.

# **MEMORY ORGANIZATION** Figure 2



# **EXAMPLE:**

Minor partitions 1 and 2 have been programmed to be 64 bits long, minor partition 3 to be 32 bits long and the major partition programmed to be 192 bits long.



#### **COMMAND WORD**

The command word is a 24-bit sequence of logic 0's and 1's which specify the operation to be performed by the device. There are six possible operations: Read Data, Write Data, Lock Data, Set Configuration, Verify Configuration or Lock Configuration. The bit sequences are detailed in Table 2.

#### **READ DATA**

If the command word issued to the DS2569S specifies a Read Data operation then the device will output the entire 512-bit memory in a serial fashion. A single read cycle consists of the host driving the input pin from a high to low state, holding it there for a period of 1uS, and then releasing the pin so the DS2569S may drive data. If a logic zero is being driven the low state will be retained on the pin for 15-70 usec after the falling edge was input. A logic 1 will return the pin to high state in a period of time after release determined by the external pullup resistor (typically, about 2 usec).

#### WRITE DATA

The Write Data command allows the entire 512 bit data memory to be written in a serial fashion. The data is input after the command word using the same convention for sending logic 0's and 1's as the command word.

#### LOCK DATA

Once issued, the Lock Data command prevents any further Write Data operations to the memory. This command is a one time only command and its effect cannot be reversed unless the power supply is removed from the part and reattached.

#### SET CONFIGURATION

The Set Configuration allows those registers which determine the user defined options to be set. The data is written to all registers serially according to Table 3.

#### **VERIFY CONFIGURATION**

The Verify Configuration command allows the configuration registers to be read in serial fashion in the same manner as the Read Data operation. Refer to Table 3 for the specific bit locations.

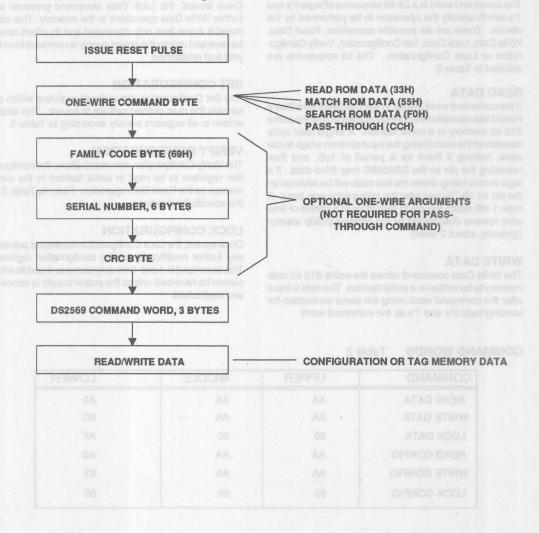
### LOCK CONFIGURATION

Once issued, the Lock Configuration command prevents any further modification of the configuration registers. This command is a one-time only command and its effect cannot be reversed unless the power supply is removed and reattached.

# COMMAND WORDS Table 2

COMMAND	UPPER	MIDDLE	LOWER
READ DATA	AA	AA	A3
WRITE DATA	AA	AA	5C
LOCK DATA	50	50	AF
READ CONFIG	AA	AA	AC
WRITE CONFIG	AA	AA	53
LOCK CONFIG	50	50	50

# 1-WIRE COMMAND SEQUENCE Figure 3



# **CONFIGURATION REGISTER** Table 3

BIT(DEC)	FUN	ICTION							
00 01-09		CW/SS Mode (1=CW; 0=SS) MAJOR PARTITION LENGTH (1 - 512 bits); BIT 01 = LSB							
		MSB	LSB	PAF	RTITION LENGTH	smem			
		00000	00000 = 00001 = 00010 =	2 bi	t long ts long ts long, etc.	0 00			
10-16	The	se bits shou	ld be progra	mmed	to 0000000.				
17-23	PAF	RTITION 1 L	ENGTH (1 -	128 bi	ts); BIT 17 = LSB				
24-30 31-37					ts); BIT 24 = LSB ts); BIT 31 = LSB				
				T					
		MSB 00000	LSB 0000 =		RTITION LENGTH tlong	V <sub>a</sub> V			
			0001 =	2 bi	ts long				
		00000	0010 =	3 bi	ts long, etc.	J.V			
38-40	PUS	SHBUTTON	/SINGLE SH	HOT M	DDE BAUD RATE				
	BIT	40 BIT39	BIT38	BAL	JD RATE (Hz)	CHAP			
	0	X AM 0	977 1	11110	150	18			
	0 0 1	1 1 0	0 1 0	0.7-	300 600 1,200	1			
	1	0	1	0.1-	2,400	10			
	1 1	1	0	-10.0	4,800 9,600	190			
	0	0	o		19,200				
41 VA.Q. 10 V	FRE	SHNESSS	EAL (1=on;	O-off)		an I			
V8.0 JoV									
42-50	DIF	FERENTIAL	CLOCK DI	VIDER	RATIO	_			
	-q m E	BIT50	BIT42	OID	IVIDER RATIO	0			
		00000000			= Divide by 1				
	302	00000000	)1	40	= Divide by 2	,D			
		:							
	mrldM(	•		1	•	0			
		11111111	1 .		= Divide by 512				
	79	1 6			The second second	P			

# **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground

Operating Temperature Storage Temperature Soldering Temperature -40°C to 70°C -55°C to +125°C 260°C for 10 seconds

-0.5V to 7.0V

\*This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

#### RECOMMENDED DC OPERATING CONDITIONS

(-40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply input	DVCC, AVCC	2.5	HENGLI I	6.5	Volts	17.18
Input Logic 1 DVCC> 3.4V	V <sub>IH1</sub> B3.1-18	2.2	S LENGTH	PARTITION	Volts	31-37
Input Logic 1 DVCC< 3.4V	V <sub>IH2</sub>	DVCC-1.2V	= 000000 = 000000	8666 00	Volts	
Input Logic 0	V <sub>IL</sub>	-0.3	= 010000	0.8	Volts	

# DC ELECTRICAL CHARACTERISTICS

(-40°C to 70°C, AVCC=DVCC= 2.5 to 6.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage Cur.	I <sub>IL</sub> 009	-1.0	i	+1.0	uA	
Output Current High	I <sub>OH1</sub> OON S	-1.0	. 0		mA	V <sub>OH</sub> = DVCC-0.5 V
Output Current High (TXOUT1/2 only)	I <sub>OH2</sub>	-10.0	7		mA	V <sub>OH</sub> = DVCC-0.5 V
Output Current Low	I <sub>OL1</sub>		EL LATER E	+4.0	mA	V <sub>OL</sub> = 0.4V
Output Current Low (TXOUT1/2 only)	I <sub>OL2</sub>	raadivio :	IOOTO TWI	+10.0	mA	V <sub>OL</sub> = 0.4V
Comparator Sensitivity (M+, M-)	C <sub>SEN</sub> OTAH REGIN	_10	FIE 6000	08718 00000	mVp-p	1
Comparator Frequency (M+, M-)	C <sub>FREO</sub>	40	198	250	Khz	
Comparator Input Resistance	C <sub>IR</sub> S18 vd abiviG a	1	1919	PETER .	Mohm	
Input Capacitance	C <sub>IO</sub>			5	pF	
Operating Current	I <sub>cc1</sub>		100	150	μΑ	2
Standby Current	I <sub>CC2</sub>			2.0	μА	3
Standby Current	I <sub>ccs</sub>			100	μА	Freshness bit = 1

# NOTES:

- 1. Measured with 133 KHz sine wave at M+, M-.
- 2. M+, M- fed with 250 KHz sine wave at 100 mV p-p (a-c coupled).
- 3. M+, M- both shorted together; 1-WIRE pin = GND.

#### 1-WIRE AC CHARACTERISTICS

(-40°C to 70°C, DVCC=2.5 TO 6.5 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	t <sub>SLOT</sub>	60		120	msec	
Write 1 Low Time	t <sub>LOW1</sub>	толя 1 ——		15	msec	
Write 0 Low Time	t <sub>LOW0</sub>	60	-1	120	msec	
Read Data Valid	t <sub>RDV</sub>	15	1	11111	µsес	
Read Data Setup	t <sub>su</sub>	1			μsec	1
Frame Sync	t <sub>syc</sub>	1	annest.		µsес	
Reset Low Time	t <sub>RSTL</sub>	480			μѕес	
Reset High Time	t <sub>RSTH</sub>	480			μѕес	3 7 7 7
Presence Detect High	t <sub>PDH</sub>	15		60	µsес	
Presence Detect Low	t <sub>PDL</sub>	60		240	µsес	

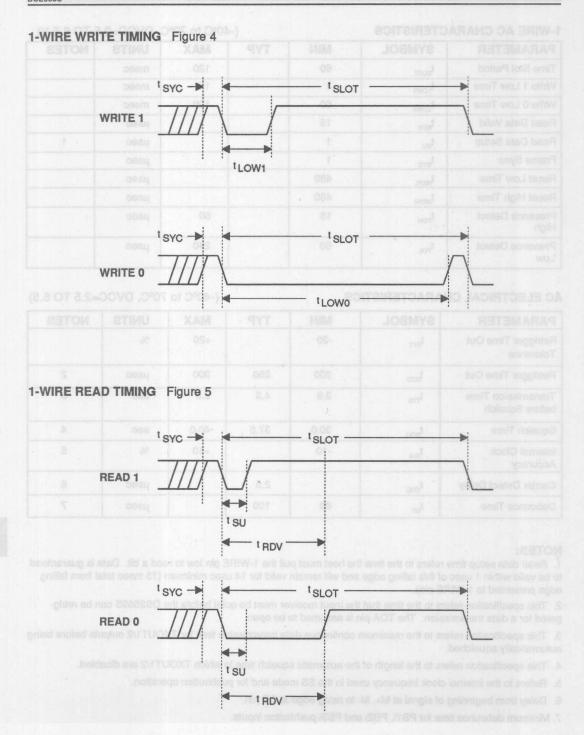
# AC ELECTRICAL CHARACTERISTICS

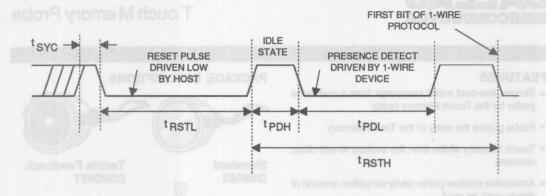
(-40°C to 70°C, DVCC=2.5 TO 6.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Retrigger Time Out Tolerance	t <sub>err</sub>	-20		+20	%	
Retrigger Time Out	t <sub>RTO</sub>	200	250	300	μsec	2
Transmission Time before Squelch	t <sub>TTS</sub>	3.8	4.3	5.0	sec	3
Squelch Time	t <sub>sou</sub>	30.0	37.5	40.0	sec	4
Internal Clock Accuracy	t <sub>ICA</sub>	-10		+10	%	5
Carrier Detect Delay	t <sub>CDD</sub>		2.5	VIII	μsec	6
Debounce Time	t <sub>DT</sub>	80	100		μsec	7

#### NOTES:

- 1. Read data setup time refers to the time the host must pull the 1-WIRE pin low to read a bit. Data is guaranteed to be valid within 1 usec of this falling edge and will remain valid for 14 usec minimum (15 msec total from falling edge presented to 1-WIRE pin).
- 2. This specification refers to the time that the input receiver must be quiet before the DS2569S can be retriggered for a data transmission. The TOA pin is assumed to be open.
- This specification refers to the maximum continuous data transmission time for TXOUT1/2 outputs before being automatically squelched.
- 4. This specification refers to the length of the automatic squelch time in which TXOUT1/2 are disabled.
- 5. Refers to the internal clock frequency used in the SS mode and for pushbutton operation.
- 6. Delay from beginning of signal at M+, M- to rising edge at CD pin.
- 7. Minimum debounce time for PB1\, PB2\ and PB3\ pushbutton inputs.





ESCRIPTION
ha DSB092 Touch Memory Probe provides the elecical contact nacessary for the transfer of data to and
con the DS199x family of Touch Memories. The
sund probe shape provides a self-aligning interface
at readily matches the circular rim of the Touch
emory MicroCan. Metal contacts resist wear and are
say to leep clean.

The DS9092 is available with a fist face plate (standard) or with optional technic feedback. The canter contract of the standard reader no moving parts, making this a more rugged interface for harsh environments. This type of rugged leaders to be be best suited for dosigna where the Touch Memory is brought into contact with the reader. The tactile fieldback back proba is ideal for situations where the Touch Memory is stationary and the movable reader is brought in contact with it.

Soft types of probes are evallable in a panel-mount version. The facilie feedback probe is also available in a grip-mount version. The panel-mount probes are settened with a rear-tocking clip ring.

Two 6-inch 22AIVG wires are provided for easy connection to the system microcontroller. The hand-grip mount mobe connectation to a 4-inch handle and one metal cable which is terminated with an R.111 tack.



# DS9092 Touch Memory Probe

#### **FEATURES**

- Simple, low-cost metal stampings form a read/write probe for the Touch Memory family
- Probe guides the entry of the Touch Memory
- Touch Memory slides over the surface to self-clean contacts
- Accessible shallow probe cavity simplifies removal of debris such as mud
- Flexible design supports panel mount or hand-grip mount with optional tactile feedback
- Bright tarnish-resistant metal surface provides millions of operations
- · Panel-mount probe, pre-wired for easy installation
- Hand-grip probe mates to RJ-11 jack for quick installation

# DESCRIPTION

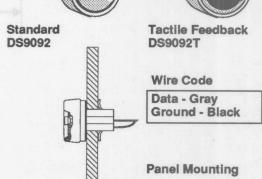
The DS9092 Touch Memory Probe provides the electrical contact necessary for the transfer of data to and from the DS199x family of Touch Memories. The round probe shape provides a self-aligning interface that readily matches the circular rim of the Touch Memory MicroCan. Metal contacts resist wear and are easy to keep clean.

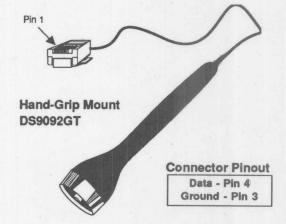
The DS9092 is available with a flat face plate (standard) or with optional tactile feedback. The center contact of the standard reader has no moving parts, making this a more rugged interface for harsh environments. This type of probe is best suited for designs where the Touch Memory is brought into contact with the reader. The tactile feedback probe is ideal for situations where the Touch Memory is stationary and the movable reader is brought in contact with it.

Both types of probes are available in a panel-mount version. The tactile feedback probe is also available in a grip-mount version. The panel-mount probes are fastened with a rear-locking clip ring.

Two 6-inch 22AWG wires are provided for easy connection to the system microcontroller. The hand-grip mount probe comes attached to a 4-inch handle and one-meter cable which is terminated with an RJ11 jack.

# PACKAGE DESCRIPTIONS





# ORDERING INFORMATION

DS9092 -

- Panel-mount probe, solid face

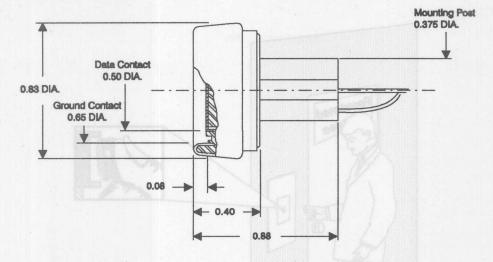
DS9092T - Panel-mount probe with tactile

feedback

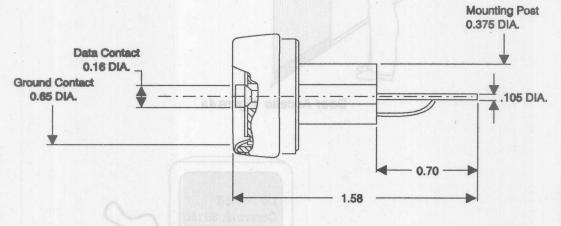
DS9092GT - Hand-grip mount with tactile feed-

back

# STANDARD TOUCH PROBE Figure 1

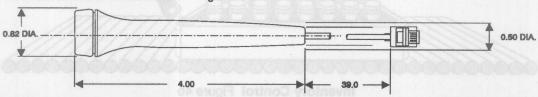


# **OPTIONAL TACTILE FEEDBACK** Figure 2



# 12

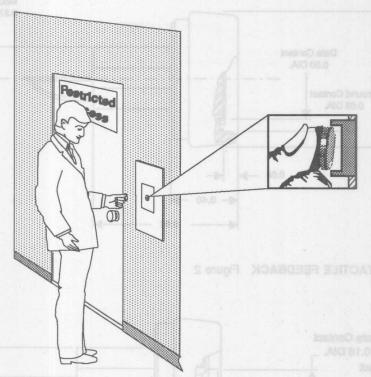
# **OPTIONAL HAND-HELD WAND** Figure 3



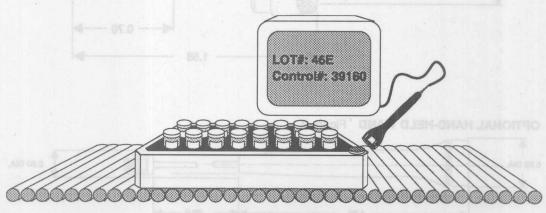
NOTE:

All dimensions are in inches.

# **TOUCH APPLICATIONS**



Door Access Figure 4a



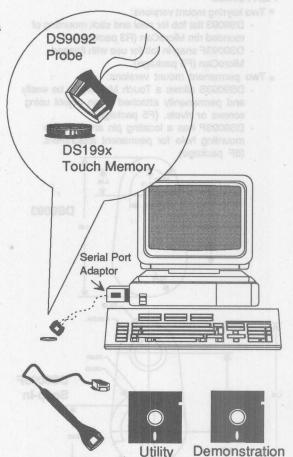
**Inventory Control** Figure 4b



# DS9092K Touch Memory Starter Kit

# **FEATURES**

- Evaluation kit for accessing DS 199x Touch Memories from an IBM PC-compatible computer
- Two DS1990 Touch Serial Numbers, one DS1991 Touch Multikey, one DS1993 4K-bit Touch Memory, one DS1994 4K-bit Touch Memory Plus Time
- DS9092 Touch Memory Probe
- DS9092GT Touch Memory Probe with Hand-grip
- Assortment of Touch Memory attachment accessories; DS9093, DS9093F, DS9093S, DS9094F, DS9096
- DS9097 PC serial port adaptor
- PC demonstration software on 5 1/4" diskette
- 5 1/4" diskette of utility functions and source code
- Data sheets and application notes



12

# DESCRIPTION

The DS9092K Touch Memory Starter Kit provides hardware and software for quick evaluation of any of Dallas Semiconductor's Touch Memory family using a PC-compatible DOS computer. Included in the kit are 5 Touch Memory devices, a DS9092 and DS9092GT Touch Probe, a PC serial port adaptor, an assortment of Touch Memory attachment accessories, demonstration

software and utility programs. The demonstration programs can be executed to read or write a Touch Memory device through a serial port via a 25-pin adaptor which connects to the DS9092 probe. The utility disk allows the user to quickly develop his own Touch Memory programs from the code provided.

Diskette

Software

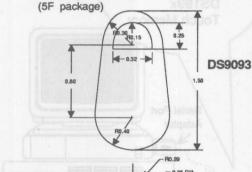
**DS9092GT** 

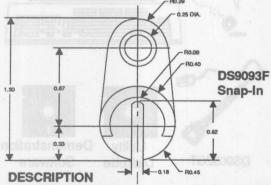


# DS9093 Touch Memory Mount

# **FEATURES**

- Two keyring mount versions:
  - DS9093 flat fob for peel and stick mounting of rounded rim MicroCan (R3 package)
  - DS9093F snap-in fob for use with flanged MicroCan (F5 package)
- Two permanent mount versions:
  - DS9093S allows a Touch Memory to be easily and permanently attached to an object using screws or rivets. (F5 package)
  - DS9093P has a locating pin and a single mounting hole for permanent attachment.

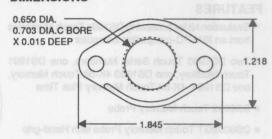


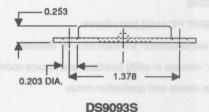


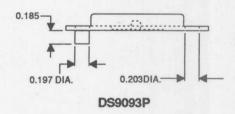
The DS9093 Touch Memory Mount offers the user a low-cost plastic fixture that holds a Touch Memory for thumbpad applications or permanent attachment to an object.

The DS9093 flat fob offers the simplest way to mount a Touch Memory for applications that require only momentary contact. The DS9093F snap-in fob is more versatile and works in captive reader applications where extended communication with the Touch

# DIMENSIONS







Memory is required. Both fobs can be attached to a keyring for carrying.

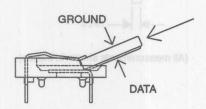
The DS9093S and DS9093P allows the user to permanently attach a Touch Memory to an object with one or two screws, rivets, etc. The plastic plate is designed with an inset that accommodates the flange on the F5 package and allows for flush mounting. A protective wall is provided along the sides of the plate to reduce incidental damage to the Touch Memory.



DS9094 MicroCan Clip

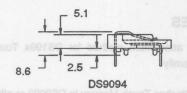
# **FEATURES**

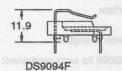
- Low cost holder for 16.3mm MicroCan
- Printed circuit board mount
- MicroCan contacts are 302 spring stainless steel
- Flammability rating: UL94V-O
- Three versions:
- DS9094 for R3 MicroCan (round rim, 3.2 mm high)
- DS9094F for F5 MicroCan (flanged rim, 5.8 mm high)
- DS9094FS for surface mounting F5 MicroCan (flanged rim, 5.8 mm high)
- Printed circuit contacts are selectively tin-lead plated for improved solderability

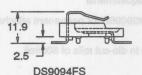


# DESCRIPTION

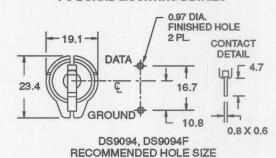
The DS9094 Clip holds a MicroCan and connects to a printed circuit board. By deflecting the spring clip in the molded housing, a MicroCan can be inserted and extracted without special tools. If reverse insertion is attempted, the beveled edge on the housing prevents contact. The DS9094's low profile minimizes the clearance height above the printed circuit board.

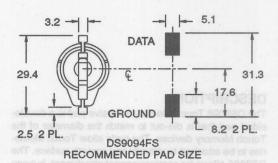






# PC BOARD MOUNTING DETAILS





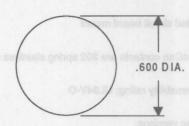


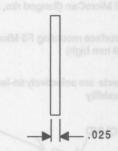
# Touch Memory Adhesive Pads

# **FEATURES**

- Low-cost attachment method for DS199x Touch Memory family
- Readily attaches Touch Memory to DS9093 or other smooth surface
- Two adhesion strengths
  - DS9096 for semi-permanent attachment requirements
  - DS9096P for permanent attachment
- Available in die-cut rolls of 500/roll

# PACKAGE DESCRIPTION





(All measurements shown in inches)

# DESCRIPTION

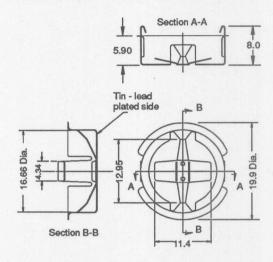
The DS9096 Touch Memory adhesive pad is a doublesided pad that is die-cut to match the diameter of the Touch Memory devices. The pads allow Touch Memories to be attached to virtually any smooth surface. The DS9096 allows for semipermanent attachment, but can be removed if necessary. The DS9096P offers a very permanent attachment method that is not intended to be removed. The pads are ideal for use in conjunction with the DS9093 keyring mount.



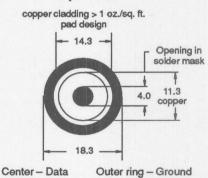
# DS9098 MicroCan Retainer

# **FEATURES**

- Compact single-piece, all-metal receptacle for MicroCan mounting
- Retainer withstands high temperatures required for surface mounting
- Center contact is permanently separated at first insertion of MicroCan
- Material is stainless steel with selective tin-lead plating for optimal solderability to printed circuit board
- Retainer to MicroCan connection is stainless steel to stainless steel
- Quadruple redundancy of contacts (4 plus 4)
- Contact force exceeds 200 grams for reliable connection
- At insertion, MicroCan is latched for retention
- Pops up for removal when latch is released
- >100 insertion/withdrawal cycles with no performance degradation
- Compatible with standard pick and place equipment; insensitive to angular orientation
- · Cleaning fluids drain freely for quick clean up
- Available in tube packaging (DS9098) or in 32mm wide tape and reel (DS9098T)



# Recommended Printed Circuit Layout Pads



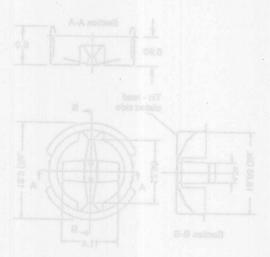
All dimensions are in millimeters

# 12

# DESCRIPTION

The DS9098 MicroCan Retainer is a low-cost, surface mount device that retains a 16.3mm x 5.8mm MicroCan on a printed circuit board. The slender design secures

the MicroCan for a compact printed circuit board mount. The retainer latches the flange of the MicroCan and prevents reversed insertion.





**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 





DS2250(T) Soft Micro Stik

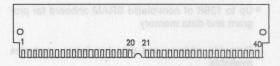
# **FEATURES**

- Compatible with industry standard 8051 instruction set
- Nonvolatile SRAM for program and/or data
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip, full-duplex serial port
- Adjustable partition between program and data memory
- Completely crashproof: program/data RAM and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power-up/ down
- Program and data memory secure, with a tamperproof, on-chip encryptor
- DS2250T: Permanently powered clock/calendar
- 40-position SIMM connection scheme

# DESCRIPTION

The DS2250 Soft Micro Stik and DS2250T Time Micro Stik are the functional equivalents of the DS5000 Soft Microcontroller and DS5000T Time Microcontroller, respectively, with the exception that both devices are available with 64 Kbytes of nonvolatile memory. The

# PACKAGE OUTLINE



40-Pin SIMM

# ORDERING INFORMATION

DS2250 XX—XX DS2250(T) XX—XX	Soft Micro	oft Micro Stik oft Micro Stik SPEED GRADE		
ro Chip	8 12 16	8MHz 12MHz 16MHz		
	PROG	PROGRAM/DATA RAM		
	8 32 64	8 Kbytes 32 Kbytes 64 Kbytes		

pinout and instruction set of both products match the industry standard 8051 microcontroller. The DS2250 and DS2250T each plug into a SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.



DS2251(T) 128K Micro Stik

# **FEATURES**

- 100% compatible with 8051 instruction set
- Up to 128K of nonvolatile SRAM onboard for program and data memory
- Bytewide address and data bus leaves port pins available
- Two peripheral chip enables access external devices via the bytewide bus
- Reprogrammable peripheral controller (RPC mode) emulates 8042 for PC bus applications
- Optional DS1283 Watchdog Timekeeper Chip allows wake-up from idle or stop mode (DS2251T)
- Flexible program loading from serial port or RPC mode peripheral bus
- Based on the DS5001FP Micro Chip
- 72-pin SIMM connection scheme

# DESCRIPTION

The DS2251 128K Micro Stik is a complete 8051-compatible microcontroller system based on the DS5001FP 128K Micro Chip. The DS2251 supports all of the improved features that the DS5001FP offers over its DS5000 predecessor. These include expanded onboard memory and additional I/O functions.

The DS2251 incorporates up to 128K of nonvolatile SRAM onboard, accessed by the DS5001FP's bytewide address and data bus. This bus is added to a standard 8051 architecture and is available at the connector for user applications. The four standard 8051-compatible ports are also available and can be used without interference from memory access. Additional I/O circuits can also be memory mapped onto the bytewide bus by using the two decoded peripheral enable signals.

# **PACKAGE OUTLINE**



72-Pin Stik

A Reprogrammable Peripheral Controller mode (RPC) brings the benefits of up to 128K nonvolatile RAM to the design of intelligent and flexible peripheral controllers through hardware emulation of the popular 8042 slave interface. This interface allows the DS2251 to reside as a peripheral on the bus of a more powerful processor.

Apermanently powered timekeeping function, the DS1283 Watchdog Timekeeper, is incorporated into the DS2251T. This real time clock is driven by an onboard quartz crystal and keeps time to a hundredth of a second. In addition, the date is automatically adjusted at the end of the month, including those months with fewer than 31 days. Leap year compensation is also performed automatically. Access to the timekeeping function is performed entirely using the DS5001FP's bytewide bus.

# **DALLAS**SEMICONDUCTOR

DS2252(T) Secure Micro Stik

# **FEATURES**

- Enhanced firmware security
   Stronger address/data encryptor
   64-bit internal encryption key
   Automatic random key generation
   SDI self-destruct input
   Top-coating on die defeats microprobe
   Customer-specific encryption available
- 100% compatible with 8051 instruction set
- Up to 128K of nonvolatile SRAM onboard for program and data memory
- Crashproof computer
   Power-fail reset
   Early-warning power-fail interrupt
   Watchdog timer
- Optional DS1283 Watchdog Timekeeper Chip DS2252T

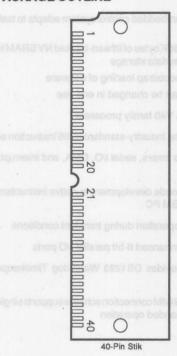
Permanently powered timekeeping Programmable time of day interrupt Programmable interval timer

- Hardware slave interface emulates 8042
- Flexible program loading from serial port or slave interface bus
- Based on the DS5002FP Secure Micro Chip
- 40-pin SIMM connection scheme

# DESCRIPTION

The DS2252 Secure Micro Stik is a complete 8051-compatible microcontroller system based on the DS5002FP Secure Micro Chip. It combines the Micro Chip with up to 128K bytes of nonvolatile SRAM memory for program and data, and an optional real-time clock. Onboard program and data memory are accessed by the DS5002FP's bytewide secure memory bus, which is encrypted using an internal security key. Thus, the memory is secure against observation. This leaves the four 8051-type ports for user I/O, while still using the full memory map of the 8051. All security provisions of the DS5002FP chip are available in the DS2252. This includes memory encryption, random 64-bit encryption-

# **PACKAGE OUTLINE**



key generation and self-destruct input for tamper protection. The details of these security functions are discussed in the DS5002FP data sheet, which is available under a nondisclosure agreement.

A permanently powered timekeeping function, the DS1283 Watchdog Timekeeper, is included in the DS2252T. This real-time clock is driven by an onboard 32 KHz crystal and keeps time to a hundredth of a second. Date is automatically adjusted at the end of the month, and leap year compensation is also performed. Access to the timekeeping function is performed entirely on the DS5002FP's memory bus.

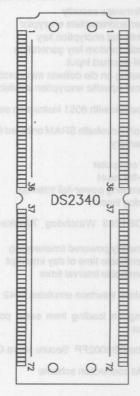


DS2340(T) Soft V40 Flip Stik

# **FEATURES**

- V40-based embedded control system adapts to taskat-hand:
  - Up to 256K bytes of lithium-backed NV SRAM for program/data storage
  - Serial bootstrap loading of software
  - Code can be changed in end use
- Incorporates V40 family processor:
  - Executes industry-standard 8086 instruction set
  - On-chip timers, serial I/O, DMA, and interrupt control
  - Allows code development in native instruction set of IBM PC
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports
- DS2340T provides DS1283 Watchdog Timekeeper Chip
- Dual 72-pin SIMM connection scheme supports singleboard or expanded operation

# **PACKAGE OUTLINE**



72-Pin SIMM Double-edge Connector

The DS2340(T) offers two SIMM card-edges to support single-board and expanded operations. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support the selected operation. Connector A supports single-board operation. This card edge provides a total of three 8-bit parallel I/O ports. One of these ports allows each pin to serve as an interrupt input. The other two ports can be configured as a high-speed interface to allow the DS2340(T) to act as a peripheral controller to a host microprocessor system.

# DESCRIPTION

The DS2340 and DS2340T Soft V40 Flip Stiks are complete, 8086-compatible microcontroller systems that provide the benefits of adaptability, crashproof operation, and powerful I/O capabilities for embedded control applications in an extremely small form factor. These unique features are made possible by the incorporation of the DS5340 V40 Softener Chip. In addition, the DS2340(T) executes the native instruction set of the IBM PC, so that the PC can serve as a development platform for the Soft V40 Flip Stiks. As a result, a wide variety of high-level language compilers, assemblers, and debugging tools are available to support system designs based on the DS2340.



# DS5000 Soft Microcontroller

# **FEATURES**

- · 8-bit uC adapts to task-at-hand:
  - 8 or 32 Kbytes of high performance nonvolatile RAM for program and/or data memory storage
  - Initial downloading of software in end system via onchip serial port
  - Capable of modifying its own program and/or data memory in end use
  - 128 internal nonvolatile registers for variable retention
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V<sub>cc</sub>
  - Orchestrates orderly shutdown and automatic restart on power up/down
  - Automatic restart on detection of errant software execution
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip, full-duplex serial I/O ports
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout

# DESCRIPTION

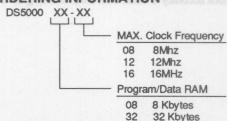
The DS5000 Soft Microcontroller is a high performance 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V<sub>cc</sub>. The entire program/data memory space is implemented using high speed, nonvolatile static CMOS RAM. Two memory size versions are available which offer either 8 Kbytes or 32 Kbytes of NV RAM for program/data stor-

# PIN CONNECTIONS

P1.0	Into riting sellorano	40	VCC
P1.1	2	39	P0.0 AD0
P1.2	3	38	P0.1 AD1
P1.3	4	37	PO.2 AD2
P1.4	<b>1</b> 5	36	P0.3 AD3
P1.5	6	35	PO.4 AD4
P1.6	17	34	P0.5 AD5
P1.7	8 8 100 100 100 100	33	P0.6 AD6
RST	9	32	PO.7 AD7
RXD P3.0	<b>1</b> 0	31	EA\ /Vpp
TXD P3.1	11 dirigino	30	ALE/PROG\
INTO\ P3.2	12	29	PSEM
INT1\ P3.3	13	28	P2.7 A15
T0 P3.4	14	27	P2.6 A14
T1 P3.5	15	26	P2.5 A13
WR\ P3.6	16	25	P2.4 A12
RD\ P3.7	17	24	P2.3 A11
XTAL2	18	23	P2.2 A10
XTAL1	<b>1</b> 9	22	P2.1 A9
VSS	20	21	P2.0 A8

40-Pin Encapsulated Package

# ORDERING INFORMATION



age. Furthermore, internal data registers and key configuration registers are also nonvolatile.

A major benefit resulting from its nonvolatility is that the Soft Microcontroller allows program memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the program and data memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution.

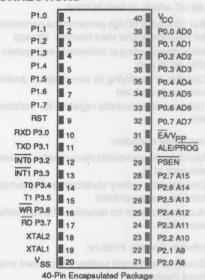


# DS5000T Time Microcontroller

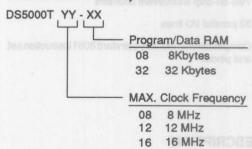
### **FEATURES**

- DS5000 Soft Microcontroller with embedded clock/ calendar
- Internal lithium cell preserves clock function in the absence of V<sub>cc</sub>
- · Permits logging of events with time and date stamp
- 8 or 32 Kbytes of embedded nonvolatile program/ data RAM
- Program loading via on-chip full-duplex serial port
- User-selectable program/data memory partition
- All 4 ports available for system control
- Resident encryptor protects program from piracy
- Power sequencer and watchdog timer help ensure crashproof operation
- Compatible with industry standard 8051 instruction set and pinout
- Clock accuracy is better than 2 min/month @25°C

# **PIN CONNECTIONS**



# **ORDERING INFORMATION**



# DESCRIPTION

The DS5000T Time Microcontroller offers all the features of the DS5000 Soft Microcontroller with the added benefit of an embedded real-time clock/calendar function. The clock function itself is accessed as though it were a part of the embedded data RAMso that the 32 I/O pins are free for the application use. With this feature, new and existing

microcontroller systems can now log events, schedule activities, and time operations. The combination of DS5000T's soft features together with a real-time clock/calendar provides a powerful controller that adapts to the needs of time-driven applications.

# **DALLAS**SEMICONDUCTOR



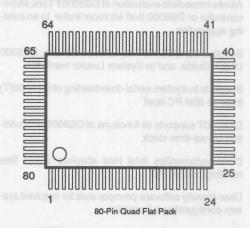
# **FEATURES**

- Offers the microcontroller die used in the DS5000 Soft Microcontroller DIP packaged in an 80-pin Quad Flat Pack (QFP)
- Provides access to bytewide address/data bus, not available on the DS5000 DIP
- Bytewide address/data bus frees up port pins for I/O use
- Direct interface to bytewide memories
- Supports up to 64 Kbytes of program/data memory
- Incorporates battery switching/monitoring circuitry for powering external memory devices in the absence of V<sub>cc</sub>
- Ultra-low standby current—less than 75 nA
- Watchdog timer ensures program control
- Fully compatible with 8051 instruction set

# **DESCRIPTION**

The DS5000FP Micro Chip is an 80-pin Quad Flat Pack (QFP) containing a standalone DS5000 Soft Microcontroller die which normally resides in a 40-pin DS5000 DIP package. It retains all the hardware features of a DS5000 DIP and can be used much like ROM-less versions of the 8051, except that all four ports of the DS5000FP are freed up for general-purpose I/O. An external lithium energy cell can be attached to this chip to power external SRAM(s) in the absence of  $\rm V_{\infty}$ . This gives the user the flexibility of using his own lithium cells and memories to implement a nonvolatile microcontroller solution with the

# **PACKAGE DESCRIPTION**



# **ORDERING INFORMATION**

DS5000FP-XX	-08	08 MHz
	-12	12 MHz
	-16	16MHz

soft features inherent in the DS5000 DIP. EPROM devices can be used for program memory in applications not requiring reloadable software.

Of the 80 pins on the package, only 68 are actually tied to pads on the die. The rest of the pins are no-connects. 40 pins of the 68 signal pins are identical in function to the 40 pins of a standard DS5000. The other 28 pins are normally used to interface to the embedded RAM and the lithium source on the standard DS5000 DIP products.

# **DALLAS**SEMICONDUCTOR

# DS5000TK Time Micro Evaluation Kit

# **FEATURES**

- Allows immediate evaluation of DS5000T Time Microcontroller or DS5000 Soft Microcontroller in an existing application
- Supplied with DS5000T32, software diskette, DS5000 User's Guide, and In-System Loader hardware
- Supports in-system serial downloading of DS5000(T) from an IBM PC host
- DS5000T supports all functions of DS5000 with addition of real-time clock
- Downloads/verifies Intel Hex absolute object files residing on IBM PC
- User-friendly software prompts user for required system configuration information
- Supports serial download rates up to 19200 bps
- Requires no support circuit overhead on target system

# Dallas Serviconductor

# DESCRIPTION

The DS5000TK Time Micro Evaluation Kit is a development support system which is designed to allow immediate evaluation of the DS5000T Time Microcontroller in a system application. Since the DS5000T performs all of the functions associated with the DS5000 Soft Microcontroller, it can also be used for evaluation of any of the versions of a DS5000 for a new or existing design.

Materials provided with the kit include a DS5000T with 32 Kbytes of RAM, full documentation on the DS5000(T), In-System Loader serial download hardware, and software for the IBM PC (KIT5K). Using the Evaluation Kit, the user can quickly configure the DS5000(T) for operation in the target system. This configuration can be performed without detailed knowledge of the operation of the DS5000's Serial Load Mode. The DS5000TK Evaluation Kit not only serves as a first-time evaluation system for the DS5000 or the DS5000T, but also performs the equivalent function of an EPROM programming system throughout the prototyping phase of the design cycle.

Adaptors are available for development with the DS2250 Soft Micro Stik and the DS2250T Time Micro Stik. For information on these see the DS907x data sheet.

The Evaluation Kit's in System Loader hardware allows application software to be loaded into the DS5000(T) while it is connected to the target system, eliminating the need for removal of the device when reprogramming is required. The In System Loader hardware consists of an RS232 cable that connects to the RS232 Fixture which houses the appropriate interface circuitry and provides a 40-pin Zero-Insertion-Force socket for the either the DS5000 or DS5000T. The fixture in turn attaches to the 40-pin target cable which connects to the microcontroller socket in the target system. The hardware provides the mechanism for the KIT5K software to take control of the DS5000(T) via the RS232 cable, place the device in its Serial Program Load Mode, and transmit new software to the device.

# DALLAS

# DS5001FP 128K Micro Chip

# **FEATURES**

- Enhanced CMOS microcontroller addresses up to 128K of NV SRAM for program/data
- Bytewide address/data bus leaves port pins for general-purpose I/O
- Multiple chip select outputs for memory mapping of peripheral devices
- Crashproof circuitry converts CMOS SRAM into nonvolatile storage
- Reprogrammable Peripheral Controller (RPC) mode emulates 8042 for PC bus applications
- Increased flexibility in program loading
- Optional CRC-16 check of NV program/data RAM area on power-up or watchdog reset
- Bandgap reference provides tight power supply monitoring
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface mount package

#### PIN CONNECTIONS BA11 P0.5/AD5 PE1\ P0.6/AD6 BA10 P0.7/AD7 CE1\ 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 P0.4/AD4 [ 7 P2 6/A14 CE3\ CE2\[ 63 CE4 PE2\ 62 □ BD3 BA9 [ 61 P0.3/AD3 ☐ P2.5/A13 BA8 BD2 P0.2/AD2 ☐ P2.4/A12 □ BD1 **BA13** ☐ P2.3/A11 P0.1/AD1 R/W BDO P0.0/AD0 UV C **DS5001FP** vcco 3 BA15 VCC GND MSEL P2.2/A10 P1.0 [ 15 P2 1/A9 P2.0/A8 RA14 16 XTAL1 P1.1 [ 17 BA12 [ 18 47 XTAL2 ☐ P3.7/RD\ P12 [ 19 P3.6/WR\ BAT [ P3.5/T1 P1.3 [ PE3\ 22 I PF 23 URST PE4 42 BA6 ☐ P3.4/T0 P3.1/TXD P3.2/INTO

80-Pin Quad Flat Pack

# DESCRIPTION

The DS5001FP 128K Micro Chip is an enhanced version of the DS5000FP Micro Chip. The DS5001FP is designed for systems with large nonvolatile SRAM and I/O requirements; its separate bytewide address/data bus accesses up to 128K bytes of nonvolatile SRAM for program/data storage. In addition, four peripheral enables allow additional I/O devices to be memory-mapped onto the bytewide bus without the need for external logic. Thus, even in the most complex systems, the 8051-compatible ports are free for general-purpose I/O. When combined with an appropriate external lithium energy cell, the DS5001FP's crashproof circuitry retains programs and data in external SRAM for 10 years in the absence of V<sub>CC</sub>.

Compared to its predecessor, the DS5000 Soft Microcontroller, the DS5001FP incorporates memory capacity and flexibility enhancements, additional I/O resources, and new software loading features. Memory improvements include the ability to address 128K bytes of NV SRAM on the bytewide bus, multiple memory architectures for optimum implementation, and a peripheral memory map. Substantial flexibility in memory selection is provided by the DS5001FP's unique architecture, which allows the most cost-effective memory selection to be used.

I/O flexibility is provided by the Reprogrammable Peripheral Controller (RPC). This is an 8042 hardware emulation mode that allows the DS5001FP to act as a slaved peripheral controller for PC bus applications. When the RPC is not in use, port I/O which is fully compatible with the 80C51 remains available. Additional I/O flexibility results from the ability to address external peripheral devices on the bytewide bus, which allows the ports to be used for other functions.

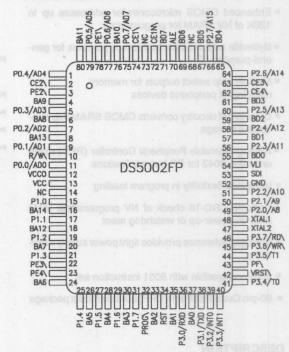


# DS5002FP Secure Micro Chip

# **FEATURES**

- Enhanced security features:
- Stronger address/data encryptor
- 64-bit encryption key word
- Automatic true random key generation
- SDI (Self-Destruct Input)
- Top coating defeats microprobe attack
- Customer-specific encryption versions available
- Incorporates enhanced memory and I/O features of DS5001FP 128K Micro Chip.
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface-mount package

# **PACKAGE OUTLINE**



# DESCRIPTION

The DS5002FP Secure Micro Chip is a secure version of the DS5001FP 128K Micro Chip. In addition to the memory and I/O enhancements of the DS5001FP, the Secure Micro Chip incorporates the most sophisticated security features available in any microcontroller. The security features of the DS5002FP include an array of mechanisms which are designed to resist all levels of threat, including observation, analysis, and physical attack. As a result, a massive effort would be required to obtain any information about memory contents. Furthermore, the soft nature of the DS5002FP allows frequent modification of the secure information, thereby minimizing the value of any secure information obtained at any given time by such a massive effort.

The DS5002FP implements a security system that is an improved version of its predecessor, the DS5000 Soft

Microcontroller. Like the DS5000, the DS5002FP loads and executes application software in encrypted form in up to 128K x 8 bytes of standard SRAM on its bytewide bus. This RAM is converted by the DS5002FP into lithium-backed nonvolatile storage for programs and data. As a result, the contents of the RAM and the execution of the software appear unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected key. Any attempt to discover the key value results in its erasure, rendering the encrypted contents of the RAM useless.

The Secure Micro Chip offers a number of major enhancements to the software security implemented in the previous generation of the DS5000 Soft Microcontroller. A full data sheet is available under non-disclosure agreement. Contact the factory for details.

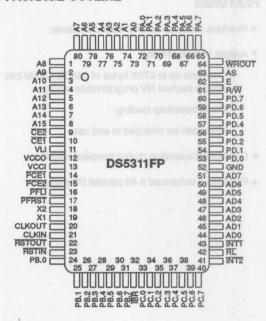


# DS5311FP 68HC11 Softener Chip

# **FEATURES**

- Softens 68HC11-based systems
  - Converts up to 64K bytes of CMOS RAM into lithium-backed NV program/data storage
  - Serial bootstrap loading
  - In-system program changes adapt HC11 to task at hand
- Crashproof operation during transient conditions
  - NV storage for 10 years with no V<sub>CC</sub>
  - Orderly shutdown/restart on power-up/down
  - Watchdog timer
  - CRC of memory on power-up
  - Call for Help via Modem
- Enhanced I/O
  - Provides four 8-bit parallel I/O ports to HC11
  - Dual port register file for Host bus interface
  - 4 decoded chip enables with write protection
  - Mates to HC11 Address/Data Bus

# PACKAGE OUTLINE



### DESCRIPTION

The DS5311FP 68HC11 Softener Chip is a member of the Softener family that is designed to provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Softener Family User's Guide, for systems based on the popular Motorola MC68HC11 microprocessor. The DS5311FP interfaces directly to the HC11's address/data bus and control signals, and converts up to 64K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the 68HC11, DS5311FP Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered DS1283 Watchdog Timekeeper Chip, can be added to the system without the need for additional glue logic.

Also available from Dallas Semiconductor is the DS2311 Soft HC11 Stik, a complete implementation of the embedded control system described above. The Stik is implemented on a SIMM module that plugs into the industry-standard 72-pin SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2311 can be used as a high-level building block in a system design, resulting in a quick time to market for a Softener-based HC11 system. Alternatively, it can be used for fast prototyping of a system that will ultimately incorporate the DS5311FP HC11 Softener Chip. The designer should consult the DS2311 data sheet for information on this application of the DS5311.

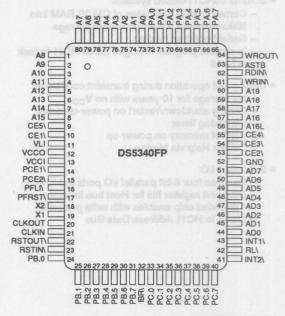


DS5340FP V40 Softener Chip

# **FEATURES**

- Provides softness for V40-based systems:
- · Adapts to task-at-hand:
  - Converts up to 672K bytes of CMOS SRAM into lithium-backed NV program/data storage
  - Serial bootstrap loading
  - Code can be changed in end use
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports

# PIN DESCRIPTION



80-Pin Quad Flat Pack

### DESCRIPTION

The DS5340 V40 Softener, a member of the Softener family, provides the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities as discussed in the DS53XX User's Guide for systems based on the popular 8088-compatible NEC V40 microprocessor. The DS5340 interfaces directly to the V40's address/data bus and control signals and converts up to 672K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the V40, DS5340 V40
Static RAM, and a lithium cell. Additional static RAM, and a lithium cell. Additional per Chip) can be added to the system without the lor additional glue logic. Because the V40 is codecompatible with the 8086, application code can be developed on a PC in its native instruction set. As a result, a

multitude of high-level language compilers, assemblers, and debugging packages are available to support development for a V40/DS5340-based embedded control system.

Also available from Dallas Semiconductor is the DS2340 V40 Soft Stik, which is a complete implementation of the embedded control system described above. The DS2340 is implemented as a small daughterboard that plugs into the industry-standard 72-pin SIMM connector scheme, which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2340 can be used as a high-level building block in a system design resulting in a quick time to market for a Softener-based V40 system. Alternatively, it can be used for fast prototyping of a system which will ultimately incorporate the DS5340 V40 Softener itself. The designer should consult the DS2340 product preview for information on this application of the DS5340.

**General Information** 

**Silicon Timed Circuits** 

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

Teleservicing

**Packages** 

Pi

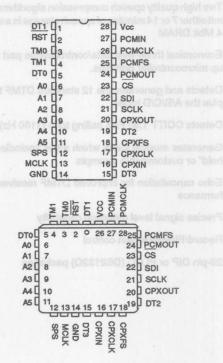


# Voice Messaging Processor

# **FEATURES**

- Per-channel voice messaging processor for digitized voice storage and retrieval
- High fidelity speech recording and playback at 8, 12, 16, 24 and 32 Kbits/sec
- Integral DTMF transceiver for remote touch-tone control and dialing
- Connects to popular PCM codec/filters for analog interfacing
- Direct PCM serial data bus interfaces to any of 32 possible TDM time slots
- Monitors and reports audio energy levels for call progress and voice detection
- Selectable beep generator for sound prompts
- 3-wire synchronous serial control port
- 28-pin DIP or PLCC (DS2130Q) packages

# PIN CONNECTIONS



# DESCRIPTION

The DS2130 Voice Messaging Processor is a CMOS DSP processor that serves as a voice messaging engine for digitized voice storage and retrieval applications. It offers half-duplex speech compression or expansion at either 8, 12, 16, 24 or 32 Kbits/sec. The advanced speech compression algorithm maintains excellent audio clarity even at low bit rates. The algorithm also incorporates a DTMF transceiver for decoding or generating touch-tone signals for remote control and automatic dialing. The tone generator can be used to create single-tone beeps used in popular answering machines. Voice and call progress detection can be easily implemented using the energy threshold detect outputs.

The DS2130 can be used together with a low-cost codec/filter device for analog interfacing in standalone applications such as answering machines or feature phones. It can also interface directly to a serial PCM bus on any of up to 32 possible time slots using an internal software-selectable time slot assigner circuit (TSAC). This configuration can be used in digital switching systems for adding voice messaging services to existing backplane designs.

Applications include digital answering machines, embedded voice response, speech annunciators, voice mail, key telephone systems and automatic operator services.

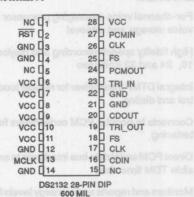


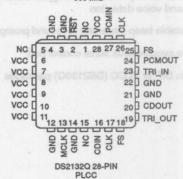
# DS2132/Q Digital Answering Machine Processor

#### **FEATURES**

- Two high quality speech compression algorithms permit either 7 or 14 minutes of speech storage in a single 4 Mbit DRAM
- Economical three-wire data/control/status port frees up microcontroller port pins.
- Detects and generates the 12 standard DTMF tones plus the A/B/C/D tones.
- Detects CCITT T.30 FAX calling tone (1100 Hz)
- Generates musical tones which allow "melodies-onhold" or customizable prompts
- Echo cancellation for improved DTMF receiver performance
- Precise signal level detection capability
- Record/Playback gain control
- 28-pin DIP or PLCC (DS2132Q) packages

# **PIN ASSIGNMENT**





# DESCRIPTION

The DS2132 Digital Answering Machine Processor is a Digital Signal Processor (DSP) optimized for the compression/expansion of PCM coded voice to/from an extremely low bit rate. The DS2132 contains two advanced speech compression algorithms that offer outstanding fidelity. The Standard Record/Playback algorithm compresses speech to 9.8Kbps and the Extended Record/Playback algorithm compresses speech to 4.9Kbps.

The DS2132 is ideal for embedded applications such as digital answering machines, voice mail, voice annunciators, and any other device that needs to maximize

speech storage in a limited memory space. A simple three wire interface to the embedded microcontroller frees up valuable controller port pins for other uses and simplifies the software needed to transfer speech data, issue commands, and receive DTMF/energy level/status information. The DS2132 detects and generates all 16 DTMF tones and can also generate a wide variety of call progress tones. In addition, the DS2132 provides CCITT Rec. T.30 FAX calling tone detection which enables the answering machine to determine if the incoming call is a voice or FAX transmission. The energy level detector allows the microcontroller to perform call progress detection and automatic gain control functions.



DS2141 T1 Controller

# **FEATURES**

- DS1 transceiver
- Parallel Control Port
- Frames to D4, ESF, and SLC-96R formats
- · Onboard two frame elastic store slip buffer
- · Extracts and inserts robbed bit signaling
- Programmable output clocks
- Supports both FDL standards, ANSI T1.403–1989 and AT&T TR54016
- 5V supply; low power CMOS
- Available in 40 pin DIP and 44 pin PLCC

# **PIN ASSIGNMENT**



40 PIN DIP

# DESCRIPTION

The DS2141 is a comprehensive, software-driven T1 framer. It is meant to act as a slave or co-processor to a microcontroller or microprocessor. Quick access via the parallel control port allows a single micro to handle many T1 lines. The DS2141 is very flexible and can be configured into numerous orientations via software. The software orientation of the device allows the user to modify

their design to conform to future T1 specification changes. The controller contains a set of 62 eight-bit internal registers which the user can access. These internal registers are used to configure the device and obtain information from the T1 link. The device fully meets all of the latest T1 specifications including ANSI T1.403-1989, AT&T TR 62411 (12-90), and CCITT G.704 and G.706.

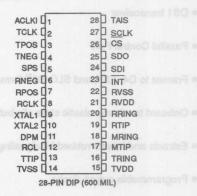


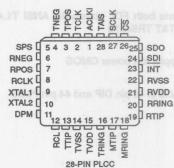
# DS2145/DS2146 T1/CEPT Medium Haul PCM Line Interface

#### **FEATURES**

- T1 (1.544 Mbps) and CEPT (2.048 Mbps) PCM line interface transceiver
- Pin compatible with the CS61574(A)/75/35(A) and LXT300/304A/305(A)
- Receiver sensitivity of -18 dB will recover data off of lines up to 3300 feet (1 km) in length
- Onboard 128 bit jitter attenuator which can be disabled
- DS2145 contains a receive side jitter attenuator DS2146 contains a transmit side jitter attenuator
- Compatible with Dallas Semiconductor's complete line of framers including the DS2180A, DS2181A, and DS2141
- Available in 28 pin DIP and PLCC
- Single +5V supply

# PIN ASSIGNMENT





#### DESCRIPTION

The DS2145 and DS2146 are monolithic CMOS T1 (1.544 Mbps) and CEPT (2.048 Mbps) line interface transceivers. They couple directly to the T1 or CEPT lines via a transformer and will recover both clock and data from lines as long as 3300 feet (1 km). These devices contain a digital clock recovery system which is very tolerant to incoming jitter and its on-board 128 bit jitter attenuator allows it to smooth wide excursions that can appear in T1 and CEPT data streams. The DS2145

and DS2146 contain a receive only monitor mode in which the transmitter can be disabled to lower the power consumption and the receive side reconstruction filter can also be disabled and replaced with straight resistive gains of 12 dB, 18 dB, or 24 dB. These devices met or exceed the applicable sections of AT&T TR62411 (Dec. 90), ANSI T1.403–1989, and the CCITT Blue book Recommendations G.703, G.823, and G.735.

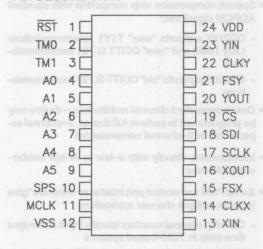


DS2165 16/24/32Kbps ADPCM Processor Chip

# **FEATURES**

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps
- Dual fully independent channel architecture; device can be programmed to perform either:
  - two expansions
  - two compressions
  - one expansion and one compression
- Interconnects directly to combocodec devices
- Input to output delay is less than 375 us
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports channel associated signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2167 ADPCM Processor Chip
- Single +3 to +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

# PIN DESCRIPTION



DS2165 24-Pin DIP

# DESCRIPTION

The DS2165 ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression to 32Kbps follows the algorithm specified by CCITT Recommendation G.721 (July 1986) and ANSI document

T1.301 (April 1987). The compression to 24Kbps follows ANSI document T1.303. The compression to 16Kbps follows a proprietary algorithm developed by Dallas Semiconductor. The DS2165 can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

# **FULL DATA SHEET AVAILABLE - CALL 214-450-3836**



# DS2167/DS2168 ADPCM Processor

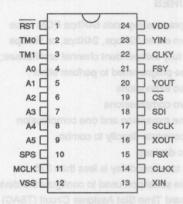
# **FEATURES**

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture device may be programmed to perform full duplex, 2-channel expansions, or 2-channel compressions
- Interconnects directly with u-law or A-law combocodec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On-chip channel counters identify input and output time slots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- · Hardware mode intended for standalone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface mount package available, designated DS2167Q/DS2168Q

### DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the

# **PIN ASSIGNMENT**



24 PIN DIP (600 mil)

transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

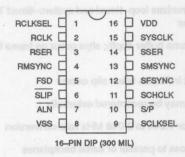


# DS2175 T1/CEPT Elastic Store

# **FEATURES**

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- · Comprehensive on-chip "slip" control logic
  - Slip occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A, DS2181 CEPT Transceivers
- Industrial temperature range of –40°C to +85°C available, designated DS2175N

# **PIN ASSIGNMENT**



# DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1-1.544 MHz) and European (CEPT-2.048 MHz) rate networks. The chip has several flexible operating

modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross—connects (DACS), private network equipment and PABX—to—computer interfaces such as DMI and CPI.

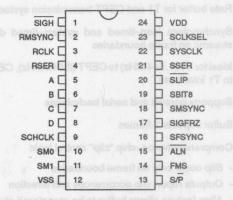


# DS2176 T1 Receive Buffer

# **FEATURES**

- Synchronizes loop–timed and system–timed T1 data streams
- Two frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of –40°C to +85°C available, designated DS2176N

# **PIN ASSIGNMENT**



24 PIN DIP (600 mil)

#### DESCRIPTION

The DS2176 is a low–power CMOS device specifically designed for synchronizing receive side loop–timed T–carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited dur-

ing alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

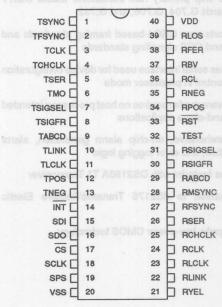
# **DALLAS**SEMICONDUCTOR

# DS2180A T1 Transceiver

# **FEATURES**

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for standalone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of -40°C to +85°C available, designated DS2180AN or DS2180AQN

# PIN ASSIGNMENT



40 PIN DIP

# DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

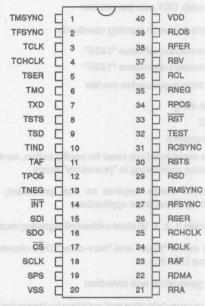


# DS2181 CEPT Primary Rate Transceiver

# **FEATURES**

- Single chip primary rate transceiver meets CCITT standards G.704, G.706, and G.732
- Supports new CRC4-based framing standards and CAS and CCS signalling standards
- Simples serial interface used for device configuration and control in processor mode
- Hardware mode requires no host processor; intended for stand-alone applications
- Comprehensive, on-chip alarm generation, alarm detection, and error logging logic
- Shares footprint with DS2180A T1 Transceiver
- Companion to dS2175 Transmit/Receive Elastic Store
- 5V supply; low-power CMOS technology

# PIN ASSIGNMENT



40 PIN DIP

# DESCRIPTION

The DS2181A is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704, G.706, and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signalling data, and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features such as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.



### DS2182 T1 Line Monitor Chip

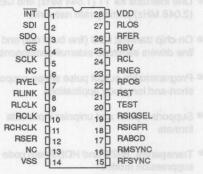
#### **FEATURES**

- · Performs framing and monitoring functions
- Supports Superframe and Extended Superframe formats
- Designed to fulfill the requirements outlined in TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit) and TR-TSY-000194 (ESF Interface Specification)
- Four onboard error counters
  - 16-bit bipolar violation
  - 8-bit CRC
  - 8-bit OOF
  - 8-bit frame bit error
- Indication of the following
  - yellow and blue alarms
  - incoming B8ZS code words
  - 8 and 16 zero strings
  - change of frame alignment
  - loss of sync
  - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allows quick access to counters for status updates
- Automatic counter reset feature
- Single 5V supply; low-power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC

#### DESCRIPTION

The DS2182 T1 Line Monitor Chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182 frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large onboard

#### **PIN ASSIGNMENT**



28-PIN DIP

counters allow the accumulation of errors for extended periods, which permit a single CPU to monitor a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signalling bits, and channel data.

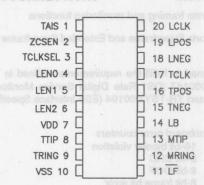


T1/CEPT Transmit Line Interface Chip

#### **FEATURES**

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip transmit LBO (line build out) and line drivers eliminate external components
- Programmable output pulse shape supports short-and long-loop applications
- Supports bipolar and unipolar input data formats
- Transparent B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply; low-power CMOS technology

#### **PIN CONNECTIONS**



DS2186 20-Pin DIP

#### **DESCRIPTION**

The DS2186 T1/CEPT Transmit Line Interface Chip interfaces user equipment to North American (T1-1.544MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback, and zero suppression logic. A line-coupling transformer is the only external component required. Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI. The DS2186 supports ISDN -PRI (Primary Rate Interface) specifications.

#### FULL DATA SHEET AVAILABLE - CALL 214-450-3836



T1/CEPT Receive Line Interface Chip

#### **FEATURES**

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411, and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank -- no tuning required
- Decodes AMI, B8ZS, and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1/ISDN Primary Rate and DS2181 CEPT Transceivers
- Companion to the DS2186 T1/CEPT Transmit Line Interface Chip
- Single 5V supply; low-power CMOS technology

#### PIN CONNECTIONS

AVDD CIL	1	20 DVDD
RAIS ZCSEN Z	3	19 RCL 18 AlS
N.C. III	CONT. YOUR SERVICE	17 BPV 16 N.C.
RCLKSEL CIT	6	15 N.C. 14 D RPOS
RRING 🗆	8	13 III RNEG
LOCK CIL		12 RCLK 11 DVSS

DS2187 20-Plin SOIC

AVDD [	1	18	DVDD
RAIS	2	DOB 17	RCL
ZCSEN [	3	16	AIS
LCAP [	4	15	BPV
RCLKSEL [	5	14	NC
RTIP [	6	13	RPOS
RRING	7	12	RNEG
LOCK [	8	11	RCLK
AVSS [	9	. 10	DVSS

DS2187 18-Pin DIP

#### DESCRIPTION

The DS2187 T1/CEPT Receive Line Interface Chip interfaces user equipment to North American (T1 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and

eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI.

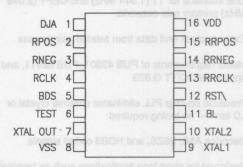


## T1/CEPT Jitter Attenuator Chip

#### **FEATURES**

- Attenuates clock and data jitter present in T1 or CEPT lines
- Meets the jitter attenuation templates outlined in TR62411, TR-TSY-000170, G.735, and G.742
- Only one external component required; either a 6.176MHz (T1) or 8.192MHz (CEPT) crystal
- Selectable buffer size of 128 or 32 bits
- Jitter attenuation is easily disabled
- Single +5V supply; low-power CMOS technology
- Available in 16-pin DIP and 16-pin SOIC

#### PIN DESCRIPTION



DS2188 16-Pin DIP

#### DESCRIPTION

The DS2188 T1/CEPT Jitter Attenuator Chip contains a 128 X 2-bit buffer which, in conjuction with an external 4X crystal, is used to attenuate the incoming jitter present in clock and data. The device meets all of the latest applicable specifications including those outlined in TR 62411(ACCUNET\* T1.5 Service Description and Interface Specifications, December 1988), TR-TSY-000170 (Digital Cross-Connect System Requirements and Ob-

jectives, November 1985), and the CCITT Recommendations G.735 and G.742. The DS2188 is compatible with the DS2180A T1/ISDN Primary Rate Transceiver and DS2181 CEPT Transceiver and it is the companion to the DS2187 T1/CEPT Receive Line Interface and DS2186 T1/CEPT Transmit Line Interface. It can also be used in conjunction with the DS2190 T1 Network Interface Unit.



T1 Network Interface
Unit (NIU)

#### **FEATURES**

- Modularized network interface for 1.544 Mbps T1 services
- Network side connects directly to T1 line
- Compatible with DS2180A T1/ISDN Primary
  Rate Transceiver
- Small size--approximately six square inchespermits integration onto line cards
- Compatible with AT&T publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data with no external components or tuning
- Detects and generates in-band loopback codes
- Assures proper ones density to network
- Powered by a local +5 volt supply

#### **PIN CONNECTIONS**

CLKSEL 014 29 TRCOD LB01 015 28 0 LOCLB LB02 016 27 0 DELSEL	LB01 LB02 LB03 LB04 LB05 LB06	01 02 03 04 05 06 08 09 010 012 013 014 015 016 017 018 019 020			42 d 41 d 39 d 38 d 37 d 36 d 35 d 34 d 33 d 31 d 30 d 29 d 28 d 27 d 26 d 25 d 25 d	RXTIP RXRING NC NC NC RSCOD RRCOD INHDEN REMLB TDENS TZERO TSCOD TRCOD LOCLB DELSEL FRSYNC TNEG TOLK
--	--	--	--	--	--	---

#### DESCRIPTION

The DS2190 T1 Network Interface Unit is a small sealed module designed to meet the recommendations of AT&T Publication 62411 for interfacing to T1 1.544 Mbps services (such as Accunet\* T1.5, Skynet\* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing

cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

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#### FULL DATA SHEET AVAILABLE - CALL 214-450-3836



DS2264 DS2268 ADPCM Stik

#### **FEATURES**

- Provides four channels (DS2264) or eight channels (DS2268) of parallel full-duplex ADPCM processing in a pre-fabricated, snap-in module
- Based on the DS2167Q or DS2165Q ADPCM Processor Chip which implements the T1.301 and CCITT G.721 recommendations
- Occupies only 2 square inches of board space
- Conforms to popular JEDEC standard 35 position single in-line connector
- Easily cascadable up to 64 full-duplex channels in multiples of four or eight
- Both A-law and U-law compatible
- Utilizes serial interface port for microprocessor control of timeslot assignments
- Includes onboard buffers for all critical signals

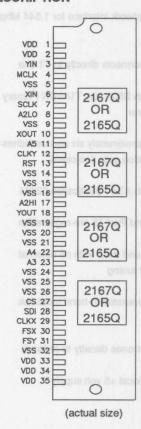
#### **ORDERING INFORMATION**

4 channels with DS2167Q	DS2264
8 channels with DS2167Q	DS2268
4 channels with DS2165Q	DS2264 - EXP
8 channels with DS2165Q	DS2268 - EXP

#### DESCRIPTION

The DS2264 and DS2268 ADPCM Stiks are complete, pre-fabricated cards that perform either four or eight channels of full-duplex ADPCM processing. The ADPCM algorithm compresses 64Kbps voice data to either 32Kbps, 24Kbps, or 16Kbps. The DS2264 is only populated on one side and offers four channels while the DS2268 is populated on both sides of the Stik and offers

#### PIN DESCRIPTION



eight channels. Control of the Stiks is handled by an external microcontroller via a serial port. Both Stiks are based on the DS2167Q or DS2165Q ADPCM Processor Chips. Specific details on the DS2167Q and DS2165Q can be found in their respective data sheets.

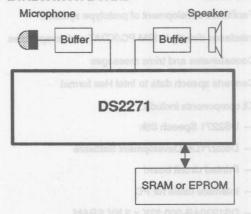
## **DALLAS**SEMICONDUCTOR

DS2271 Speech Stik

#### **FEATURES**

- Adds speech recording and playback to any system without any moving parts
- Any sound can be recorded and recreated
- Words can easily be concatenated to form sentences, which lowers the cost of storing the recorded speech
- Telephone-grade speech can be recorded at rates as low as 8Kbps
  - recording capacity of over 8 minutes with external memory
  - 14 seconds of capacity with on-Stik memory
- Can be controlled via switch closures (hardware mode) or via an external controller (software mode)
- New words can be downloaded into the Stik via software
- A kit designed to aid in speech development is available (DS2271DK)

#### **EVALUATION BOARD**



#### DESCRIPTION

The DS2271 Speech Stik is a complete solid-state audio recording/reproducing subsystem that replaces mechanical tape-based recording for embedded applications. With the Speech Stik, equipment can coach novice users on its operation or it can inform nontechnical users of malfunctions. The DS2271 Speech Stik digitizes speech and automatically stores the speech in external memory. With external EPROM, the DS2271 becomes a voice annunciator. With external SRAM, the DS2271 becomes a voice recorder with the ability to both record and play back speech. The DS2271 has been designed to allow the user to easily integrate it into

existing systems. The Stik has the unique ability to allow the user to customize each unit with different words and phrases. With the separate speech development kit (DS2271DK), the user has the ability to "edit" the recorded speech to create smooth sounding sentences out of discrete words.

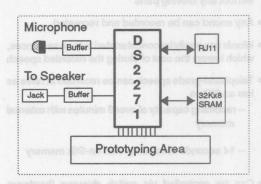


### DS2271DK Speech Stik Design Kit

#### **FEATURES**

- Facilitates development of prototype systems
- Interfaces directly to IBM PC/XT/AT and compatibles
- Concatenates and trims messages
- Converts speech data to Intel Hex format
- Kit components include:
  - DS2271 Speech Stik
  - DS2271 DK Development Software
  - Printed circuit board
  - Interface cable for PC
  - DS1230AB-200 32K x 8 NV SRAM
  - Microphone, speaker jack, and interface circuitry
  - RS-232C Port

#### **EVALUATION BOARD**



#### DESCRIPTION DESCRIPTION

The DS2271 DK Design Kit provides a convenient and flexible platform for prototyping the wide array of possible DS2271 applications. The evaluation board comes with a DS2271 and the interface circuitry necessary for common applications including a microphone, a speaker jack, and an RS-232 port. By connecting the provided cable between a PC and the evaluation board's RS-232

port, the design kit control software can be used to issue DS2271 commands and build compound messages from smaller recorded messages. Prospective compound messages can be previewed by using the MPLAY command and, if desired, converted to Intel Hex format for mask programming.

### DS2280/DS2281 T1 Line Card Stik **CEPT Line Card Stik**

#### **FEATURES**

- · Pretested, Snap-In T1 or CEPT line card
- DS2280 DS2281-075

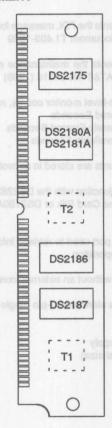
T1 Line Card

DS2281-120

75 ohm CEPT Line Card 120 ohm CEPT Line Card

- Consumes only 2 square inches of board space
- Performs four functions:
  - line interface
  - framing
  - monitoring
  - buffering
- DS2280 and DS2281 share the same pinout
- Includes line interface transformers and termination resistors
- Connects to both 1.544 MHz and 2.048 MHz backplanes
- Operates off a single +5V supply

#### **PIN ASSIGNMENT**



#### DESCRIPTION

The DS2280 and DS2281 are T1 and CEPT line cards that consume only two square inches of printed circuit board space. The cards are designed to plug into standard 68-pin Single In-line connectors. They have been arranged for maximum flexibility and contain all the necessary hardware to connect directly to either T1 or CEPT 75 ohm lines, or CEPT 120 ohm lines. The line interface function is performed by the DS2187 and

DS2186. The monitoring and framing functions are performed by the DS2180A on the DS2280 and by the DS2181 on the DS2281. The buffering function is handled by the DS2175. The DS2280 and DS2281 provide all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). They also provide indication of frame errors, CRC-6 or CRC-4 errors, and bipolar violations.

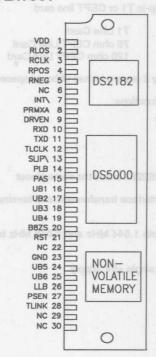


T1 FDL Controller/ Monitor Stik

#### **FEATURES**

- Fully implements the FDL message format as described in the ANSI document T1.403-1989
- Fully implements the maintenance message protocol described in AT&T TR 54016 (1989)
- · Provides high-level monitor counts, namely:
  - Errored Seconds
  - Severely Errored Seconds
  - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2283 T1 Enhanced Line Card Stik or DS2180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin Single In-Line connector
- Single +5V supply (actual size)

#### Stik LAYOUT



#### DESCRIPTION DE LA COMPANIE DE LA COM

The DS2282 T1 FDL Controller/Monitor Stik completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000194 (Extended Superframe Format Interface Specification, December 1987) and the ANSI document T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). It also implements

the protocol that is described in the AT&T publication TR 54016 (Requirements for Interfacing DTE to Services Employing ESF - September 1989). In addition, it provides a number of important performance parameters involved in monitoring T1 lines such as Errored Seconds, Severly Errored Second, and Unavailable Seconds.

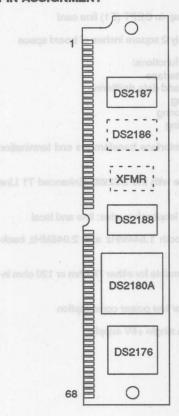


## DS2283 Enhanced T1 Line Card Stik

#### **FEATURES**

- Pre-tested, snap-in T1 line card
- · Consumes only 2 square inches of board space
- Performs six functions:
  - line interface
  - clock recovery/dejittering
  - framing
  - monitoring
  - buffering
  - robbed-bit signaling extraction
- Includes line interface transformers and termination resistors
- Three separate loopback modes: payload, line, and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- Fully CMOS for low power consumption
- Operates off a single +5V supply

#### PIN ASSIGNMENT



#### DESCRIPTION

The DS2283 is a T1 line card that consumes only two square inches of printed circuit board space. The card is designed to plug into standard 68-pin, single in-line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to T1 DSX-1 twisted pair lines. The line interface function is performed by the DS2187 Receive Line Interface and DS2186 Transmit Line Interface. The dejittering of the clock and data is performed by the DS2188

T1/CEPT Jitter Attenuator. The monitoring and framing functions are performed by the DS2180A T1/ISDN Primary Rate Transceiver. The buffering and robbed-bit signaling extraction functions are handled by the DS2176 Elastic Store with Signalling Buffer. The DS2283 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC-6 errors, and bipolar violations.

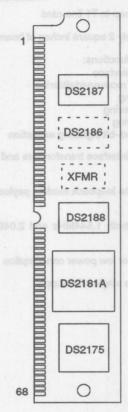


## DS2284 Enhanced CEPT Line Card Stik

#### **FEATURES**

- Pretested, Snap-In CEPT (E1) line card
- · Consumes only 2 square inches of board space
- Performs five functions:
  - line interface
  - clock and data dejittering
  - framing
  - monitoring
  - buffering
- Includes line interface transformers and termination resistors
- Pin compatible with the DS2283 Enhanced T1 Line Card Stik
- Two separate loopback modes: line and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- User programmable for either 75 ohm or 120 ohm interfaces
- Fully CMOS for low power consumption
- Operates off a single +5V supply

#### **PIN ASSIGNMENT**



#### DESCRIPTION

The DS2284 is a CEPT (E1) line card that consumes only 2 square inches of printed circuit board space. The card is designed to plug into standard 68-pin Single In-Line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to either CEPT 2.048Mbps 75 or 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The dejittering of the clock

and data is performed by the DS2188. The monitoring and framing functions are performed by the DS2181A. The buffering function is handled by the DS2175. The DS2284 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC errors, and bipolar violations.

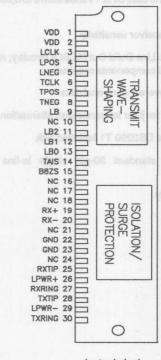


DS2290 T1 Isolation Stik

#### **FEATURES**

- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403-1989 for transmit pulse characteristics
- . Line build outs of 0dB, -7.5dB, and -15dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

#### Stik LAYOUT



(actual size)

#### DESCRIPTION

The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre-registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping circuitry that creates transmit pulses meeting the latest T1 specifica-

tions including TR 62411 (Accunet\* T1.5 Service Description and Interface Specifications, - December 1988) and T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

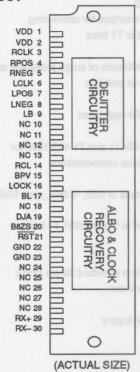


DS2291 T1 Long Loop Stik

#### **FEATURES**

- Recovers clock and data off of T1 lines from 0 to 6,000 feet in length
- +0 to -30dBSX receiver sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- · Dejitters the recovered clock and data
- Meets TR 62411 for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

#### STIK LAYOUT



#### DESCRIPTION TO THE PROPERTY OF THE PARTY OF

The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data off a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6,000 feet. It also will dejitter the recovered clock and data according the jitter attenuation curves

outlined in AT&T Communications Document TR 52411 (Accunet\* T1.5 Service Description and Interface specification — December 1988). Applications area include Channel Service Units (CSU), T1 monitoring equipment, and T1 test equipment.

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

**Automatic Identification** 

Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 

General Information

Silicon Timed Circuits

Multiport Memory

Nonvolatile RAM

Intelligent Sockets

Timekeeping

User-Insertable Memory

User-Insertable Memory (Secured)

**Battery Backup and Battery Chargers** 

System Extension

Sin Stilk Prefabs

Automatic identification

Microcontrollers

Telecommunications

Teleservicing

Packages

# **DALLAS**SEMICONDUCTOR

### DS0065 TeleMicro Interface System Software

#### **FEATURES**

- Modem control software for the DS2244T TeleMicro Stik
- Multi-tasking between application code and modem control code
- Frees the user from understanding complex modem protocols
- Speeds system development
- Compact assembly language uses minimal memory
- Entire library requires 7K bytes of program memory
- Optional routines may be omitted from memory
- · Simplified user interface-one system call
- · Easily modifiable source code allows customization
- Allows DS2244T to be reloaded by phone
- C-callable routines
- · Library of functions includes:

Multitasking system executive routine
Software UART routine
Originate only routine
Answer only routine
Remote reloader routine
Hang-up routine
DTMF decode routine
Phantom DAA operations

- Supports numerous user-selectable parameters
- Provides complete status reporting
- Phantom DAA (DS2249PH) support

Test modes routine



#### DESCRIPTION

The DS0065 TeleMicro Interface System is a library of software subroutines and parameter structures that can be combined with user application software in the DS2244T TeleMicro Stik. The DS2244T is an 8-bit microcontroller that incorporates 32K of nonvolatile RAM, a real-time clock, DTMF decoding and modem features. This device allows the user to execute specialized application software and to incorporate data communications by telephone. Embedded systems using the DS2244T can benefit from its integral modem when performing a variety of tasks such as data logging (including time stamp and date) with telephone reporting, remote control by telephone, and embedded control with telephone status reporting. Interaction of the user's application software with the outside world is conducted via the onboard modem. The DS0065 package is designed to simplify this interface, freeing the user from learning the intricacies of modem communication and minimizing the time required to incorporate modem communication into the embedded control realm. The DS0065 allows system designers to concentrate on the application design. A simple software interface is provided with one entry point. However, the library is designed to handle the majority of tasks concerning data communication from intitialization of modem parameters to terminating the telephone call. The multitasking system included as part of the DS0065 provides an orderly means of switching between modem control tasks and application code with minimal disruption.





### DS1360 Phantom DAA Chip

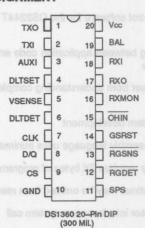
#### **FEATURES**

- Single-chip DAA controller for:
  - Modems
  - Speech interfaces
- Phantom operation reports loop current changes back to host
- Allows the DAA to use an existing phone line unobtrusively
- Transmit/receive interface connects directly to 600 ohm phone-line coupling transformers
- On-chip electronic 2- to 4-wire converter
- Integrates FCC Part-68 DAA requirements:
  - Ring detection
  - 2-second billing delay
  - Transmit power limiter
- Onboard, low-pass filtering of transmit and receive signals
- Replaces up to 20 discrete components
- Voice/data switching
- Software-controlled receive gain
- · 3-wire serial control port
- +5 Volt single-supply operation
- DS1360S surface mount version available

#### DESCRIPTION

The DS1360 Phantom DAA Chip is a CMOS device that integrates FCC requirements for interfacing data and voice to the telephone network. The DS1360 meets FCC Part-68 specifications such as 2-second billing delay, transmit signal power limiting, and ringing detection. It also offers programmable transmit and receive gains and an on-chip 2- to 4-wire converter (hybrid). By adding a coupling transformer, a relay, and an optocoupler, a complete DAA circuit can be quickly designed.

#### PIN ASSIGNMENT



A unique feature of the DS1360 is its ability to sense loop current using an on-chip, 8-bit A/D converter. By using an external optocoupler (for proper isolation), the phone loop current can be digitized and monitored through the serial port by a host processor. The DS1360 can also be programmed by external resistors to report when the current has changed by a certain percentage. Loop current sensing is important for monitoring the activity of extension phones or for determining loop length for cable compensation.



### DS2244T TeleMicro Stik

#### **FEATURES**

- · 8-bit microcontroller system with integral modem
  - Fully user-programmable
  - 32K x 8 NV RAM for program/data memory
  - 24 general-purpose port pins for user I/O
  - 10 year data retention without V<sub>CC</sub>
  - Based on standard 8051 instruction set
- Integral modem provides outside data access
  - Supports Bell 212A/103 & CCITT V.22bis/V.22/V.21
  - 1200 or 2400 bps modem versions available
  - Transfers data from connector or uC memory
- DS0065 software support library available
- Permanently powered real-time clock/calendar
  - Time of day interrupt alarm
  - Periodic interrupt alarm
- DTMF generation and detection
- Low-power +5V only operation
- Standard 30-pin SIMM connection scheme

#### DESCRIPTION

The DS2244T TeleMicro Stik is an 8-bit, 8051-compatible microcontroller system that is based on nonvolatile RAM and that incorporates an integral modem and DTMF decoder. 32K x 8 of nonvolatile SRAM is available for program and data memory storage. The DS2244T also includes a permanently powered real-time clock/calendar (RTC). Twenty-four port pins are available for user-defined I/O. The nonvolatile memory and permanently powered clock/calendar allow data to be recorded, logged to nonvolatile memory with time stamp and date, and reported via the phone line at a later time. Using the alarm capabilities of the integral timekeeper, the DS2244T can originate a telephone call report at a predetermined time and date.

#### **PIN NAMES**

-			
1	P3.5 (T1)	16	P3.6 (WR)
2	P3.1 (TXD)	17	ALE
3	P1.4 ( <del>OH</del> )	18	P3.0 (RXD)
4	P1.5 (RI)	. 19	P3.2
5	P2.0	20	P0.0
6	P2.1	21	AIN
7	P2.2	22	P0.1
8	P2.3	23	P0.2
9	P2.4	24	P0.3
10	P2.5	25	P0.4
11	P2.6	26	P0.5
12	vcc	27	P0.6
13	P2.7 (RXCLK)	28	AOUT
14	GND	29	P0.7
15	P3.7 (RD)	30	PROG

Date and time of day will be retained by lithium-backed circuitry in the absence of power for at least 10 years at 25° C. The DS2244T can serve a wide range of functions from a diagnostic processor with automatic reporting to a specialized modem by providing a full-function, user-programmable microcontroller coupled to an integral modem. The user's application software can access any feature of the DS2244T with few restrictions. However, interaction with the on board modem can be greatly simplified using the DS0065 TeleMicro Interface System software. This package provides a multi-tasking environment that controls the modem and performs other user-requested tasks. More detail is available in the DS0065 TeleMicro Interface System data sheet.



DS2245 Soft Modem Stik

#### **FEATURES**

- Bell 212A/103 and CCITT V.22bis/V.22/V.21
- Full-duplex operation at 2400, 1200 and 300 bps
- Familiar AT command set
- FCC Part-68 pre-certified when used w/DS2249 DAA
- Teleservicing mode allows reloading/monitoring of DS2250 Soft microcontroller Stik
- Provides remote software updates without host cooperation
- Generates and interprets DTMF tones
- Auto-answer and Originate modes
- Parallel interface connects to PC or other bus
- Reprogrammable with firmware upgrades
- +5V operation
- Low power operation consumes under 400 mW
- Extremely small form factor
- 30-pin SIMM connection scheme

#### ORDERING INFORMATION

PIN ASSIGNMENT

DS2245-12U 1200 BPS U.S. ONLY DS2245-24 2400 BPS INT'L.

#### PIN NAMES

1	CP.2	16	D7
2	CP.1	17	D6
3	OH	18	WR
4	RI	19	D5
5	SPEN	20	RD
6	CP.3	21	AIN
7	CP.0	22	NC
8	D4	23	A2
9	D3	24	A1
10	D2	25	A0
11	D1	26	OUT1
12	VCC	27	UR
13	D0	28	AOUT
14	GND	29	INT.
15	CS	30	PROG

#### DESCRIPTION

The DS2245 Soft Modern Stik is a data communication subsystem which forms a complete 2400/1200/300 bps modern when combined with the DS2249 DAA. The DS2245-24 supports V.22bis, V.22, V.21 as well as Bell 212A and 103. The DS2245-12U supports the latter Bell standards only. In addition to industry-standard, AT-type commands, the DS2245 provides decoding of incoming DTMF tones. This allows a host system to accept com-

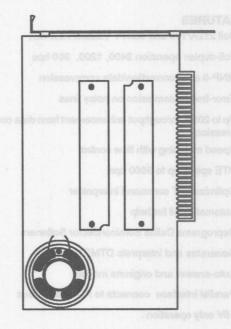
mands from a remote site where a modem is not available. A unique Teleservicing mode allows a central location to dial up a remote system and examine, edit, or reload the program/data memory contents of that system. The DS2245 is designed for embedded applications that benefit from communication with the outside world, and for which a familiar AT command set is desired.



### DS2245K Soft Modem PC Evaluation Kit

#### **FEATURES**

- PC evaluation kit for DS2249 DAA and DS2245 Soft Modem
- For use in PC XT/AT-compatible computers
- Terminal emulation software included
- Provides reprogramming fixture for DS2245 family
- Selectable COM1 or COM2
- AT command set-compatible
- DTMF detection
- Call progress detection
- Speaker for audio monitoring
- FCC Part 68 approved



#### DESCRIPTION

The DS2245K is an evaluation kit and programming fixture for the DS2245 family of modem Stiks. It includes a DS2245-24 modem and DS2249 DAA. The evaluation kit slides into a normal XT/AT 8-bit expansion slot and acts as either a COM1 or COM2 serial port. Software that is included with the kit provides communication control and allows reprogramming of DS2245 series

Stiks. The PC card also incorporates a high quality speaker for monitoring of a call connection. The DS2245K provides a convenient platform for evaluation of the DS2245 and DS2249 family, as well as providing a convenient fixture for loading program upgrades into the modems. New modem control programs can be loaded directly into the DS2245 from a diskette.



### DS2245M Soft Modem w/MNP

#### **FEATURES**

- Bell 212A/103 and CCITT V.22bis/V.22/V.21
- Full-duplex operation 2400, 1200, 300 bps
- MNP-5 error correction/data compression
- Error-free transmission on noisy lines
- Up to 200% throughput enhancement from data compression
- Speed matching with flow control
- DTE speed up to 9600 bps
- Optimized AT command interpreter
- Automatic call for help
- Reprograms Dallas Semiconductor Softeners
- Generates and interprets DTMF tones
- Auto-answer and originate modes
- Parallel interface connects to PC or other bus
- +5V only operation
- Low-power operation consumes under 400 mW
- Extremely small form-factor
- Pin-compatible with DS2245
- 30-pin SIMM connection scheme

#### DESCRIPTION

The DS2245M Soft Modem with MNP is a data communications subsystem which forms a complete 2400/1200/300 bps modem when combined with the DS2249 DAA. Embedded software in the DS2245M is capable of sophisticated error correction and data compression using MNP level 5. This software allows the DS2245M to negotiate with the remote modem in order to determine the highest level of protocol that is mutually supported. The DS2245M supports V.22bis, V.22/V.21 and Bell 212A/103 standards. In addition to industry-standard commands and MNP-5, the Soft Modem pro-

#### **PIN ASSIGNMENTS**

#### **ORDERING INFORMATION**

DS2245ML-24 2400 bps MNP modem DS2245ML-24 2400 bps MNP modem, w/no DTMF detection

#### PIN NAMES

1	CP.2	16	D7
2	CP.1	17	D6
3	OH	18	WR
4	RI	19	D5
5	SPEN	20	RD
6	CP.3	21	AIN
7	CP.0	22	NC
8	D4	23	A2
9	D3	24	A1
10	D2	25	A0
11	D1	26	OUT1
12	VCC	27	UR
13	D0	28	AOUT
14	GND	. 29	INT
15	CS	30	PROG

vides decoding of incoming DTMF tones. This allows a host system to accept commands from a remote site where a modem is not available. The DS2245M is optimized for embedded applications that require reliable communication and for which an AT command set is desired. A unique Teleservicing mode allows a central location to dial up the remote system and examine, edit, or reload the program/data memory contents of that system. The DS2245M is also capable of initiating a call for help when using a Dallas Semiconductor Softener and reloading the soft processor by phone.



## Data Access Arrangement (DAA) Stik

#### **FEATURES**

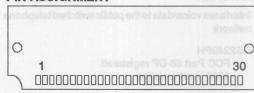
- Direct connection to the public switched telephone network
- FCC Part-68 compatible with 1000 volts isolation
- User-transferable FCC registration when used with DS2245 Soft Modem Stik
- Single +5 volt supply
- Ring detection
- 2- to 4-wire converter
- Audio monitor output
- 30-pin SIMM connection scheme

#### DESCRIPTION

The DS2249 Data Access Arrangement (DAA) Stik is designed to provide direct connection to the public switched telephone network through an appropriate connector such as an RJ-11. The DS2249 DAA carries a user-transferable, FCC Part-68 registration when used with the DS2245 modem. It is easily registrable with any other data/voice communication circuitry, provided that this circuitry performs output power limiting and billing delay. Included in the DS2249 is a ring detection output, a 2- to 4- wire converter for use with modems such as the DS2245, and an audio output for connection to speaker circuitry. It operates from a single +5 volt source.

Applications include laptop computers, remote data collection, or any application which can benefit from data or voice communication by telephone.

#### **PIN ASSIGNMENT**



30-PIN SIMM

#### PIN NAMES

	SAME AND INSTRUMENTS
PIN#	PIN NAME
1	OH
2	AUDIO
3	TXA
4	RXA
5-9	NC
10	VCC
11	GND
12	RI ooV nedw
13-26	NC
27	RINGO
28	TIPO
29	RING
30	TIP

#### FULL DATA SHEET AVAILABLE - CALL 214-450-3836



## DS2249PH/EU

#### **FEATURES**

- Interfaces voice/data to the public switched telephone network
- DS2249PH
   FCC Part 68-DP registered
   1000 Vrms isolation
- DS2249EU
   3750 Vrms isolation
   Meets most European requirements
- Single +5 volt supply operation
- Phantom feature monitors DC loop current Reports changes to host Allows unobtrusive access to existing phone lines
- Ring detection
- 2- to 4-wire converter
- Audio output monitor
- System monitoring and control
   power up equipment on ring detect
   Early warning NMI to uP
   uP reset when V<sub>CC</sub> is out of tolerance
   Watchdog timer
   Wink detection (DS2249PH only)
- 30-pin SIMM connection scheme

#### **PIN ASSIGNMENT**

	Acres 1	
600		
0		0
5	1 0000000000000000000000000000000000000	30

#### PIN NAMES

1	OH	16	ST
2	AUDIO	17	PSI
3	TXA	18	PSO
4	RXA	19	V <sub>BAT</sub>
5	AUXI	20	RINGDIS
6	SCLK	21	RST
7	D/Q	22	IN
8	cs	23	NMI
9	SPS memory	24	WINK (DS2249PH ONLY)
10	Vcc	25	NC
11	GND	26	NC
12	RI da de gan (	27	RINGO
13	BAL	28	TIPO
14	GSRST	29	RING
15	DLTDET	30	TIP

#### DESCRIPTION

The DS2249PH Data Access Arrangement (DAA) Stik provides data communication equipment (modem) with direct connection to the public switched phone network and has been registered by the FCC under Part 68-DP. This user-transferable registration includes isolation and protection, billing delay, and power limiting so that

no further certification is required under Part-68. The DS2249PH also features extensive system monitoring and control capability which had been previously unavailable in a DAA. The DS2249PH has been tailored to embedded systems by providing these additional capabilities while saving power and space.

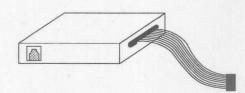


## DS6071A TeleMemory System DS6071K TeleMemory Evaluation Kit

#### **FEATURES**

- Teleservicing retrofit system
- Connects to a standard 28-pin, bytewide RAM socket through a ribbon cable
- Uploads memory contents from any remote system
- Allows remote examination/editing of data memory
- Distributes new embedded application software by telephone
- MNP Level 5 error correction guarantees accurate data transmission
- Data compression minimizes phone line charges
- FCC Part-68 registered for immediate connection to phone line
- Multiple connecting options via modem
  - Modem connects at 2400 or 1200 bps
  - V.22bis, V.22, & Bell212
  - Answers on a programmable number of rings
  - Varies the number of rings with time of day
- Holds host processor in reset allowing program code updates
- No additional engineering required
- Eurocard box includes three Teleservicing Stiks:
  - DS2249 DAA
  - DS2244T Modem (with TeleMemory software)
  - DS2230T Dual Port NVRAM
- Evaluation kit (DS6071K) includes DS0020 Service Coordinator software for the PC
- Direct RJ11 connection to phone line
- +5V operation, powered from ribbon cable

#### PACKAGE OUTLINE



#### **ORDERING INFORMATION**

DS6071A

TeleMemory System

DS6071K

TeleMemory Evaluation Kit (includes DS0020 software)

#### PIN NAMES

1	A14 (or V <sub>PP</sub> )	15	DQ3
2	A12	16	DQ4
3	A7	17	DQ5
4	A6	18	DQ6
6	A4	20	CE
7	A3	21	A10
8	A2	22	ŌĒ
9	A1	23	A11
10	A0	24	A9
11	DQ0	25	A8
12	DQ1	26	A13
13	DQ2	27	WE (or A14)
14	GND	28	Vcc

<sup>\*</sup>Alternate functions shown in parentheses () are used in retrofitting EPROM applications.



## DS6071A TeleMemory System DS6071K TeleMemory Evaluation Kit

#### PEATURES

- metava filodor politivosolo? •
- Connects to a standard 28-pin, bytewide RAM socket through a ribbon cable.
- · Upicade memory contents from any remote system
- Allows remote examination/editing of data memory
- Distributes new embedded application software by telephone
- MNP Layel 5 error correction guarantees accurate
   data transmission.
  - e Data compression minimizes phone line charges
- FCC Part-68 registered for immediate connection to phone line
  - e Multiple competing options via modern
  - Modern connects at 2400 or 1290 box
    - V 225is, V 22, & Beli212
- Answers on a programmable number of rings
  - Varios the number of rings with time of day
- Holds host processor in reset allowing program code updates
  - beriuper princenipre lancitibhs old a
  - Eurocard box includes three Teleservicing Stike:
    - DEPRING DAA
- DS2244T Modern (with TeleMemory software)
  - ... DSSSSOT Book NVRAM
- Evaluation kit (DS6071f) includes DS0020 Service
  Coordinator software for the PC
  - Finest RJ11 connection to phone line
  - e u.SV nagration, gowered from ribbon cable

#### PACKAGE OUTLINE



#### опревис ингорматиом

SE071A TeleMentory System
ISS071K TeleMentory Evaluation KB

#### PRIMARIE LOS

"Alternate functions shown in parentheses () are used in retrolithing EPROM applications.

ar

**General Information** 

Silicon Timed Circuits

**Multiport Memory** 

Nonvolatile RAM

**Intelligent Sockets** 

**Timekeeping** 

**User-Insertable Memory** 

**User-Insertable Memory (Secured)** 

**Battery Backup and Battery Chargers** 

**System Extension** 

Sip Stik Prefabs

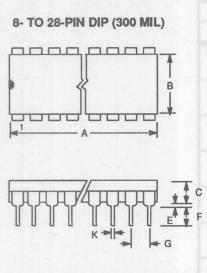
**Automatic Identification** 

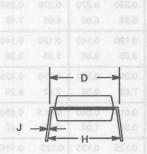
Microcontrollers

**Telecommunications** 

**Teleservicing** 

**Packages** 



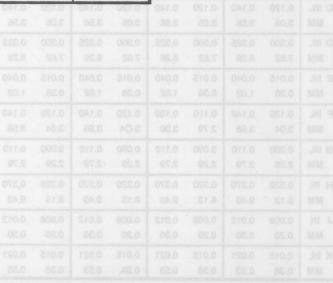


Includes:		
DS1000	DS1215	DS1291
DS1000M	DS1218	DS1293
DS1003	DS1221	DS1336
DS1003M	DS1222	DS1385
DS1005	DS1228	DS1602
DS1005M	DS1229	DS1610
DS1007	DS1231	DS1632
DS1010	DS1232	DS1640
DS1012M	DS1232LP	DS1651
DS1013	DS1234	DS1652B
DS1013M	DS1236	DS1653
DS1020	DS1237	DS1669
DS1040M	DS1238	DS2009D
DS1200	DS1239	DS2010D
DS1206	DS1259	DS2011D
DS1210	DS1267	DS2013D
DS1211	DS1275	o I have

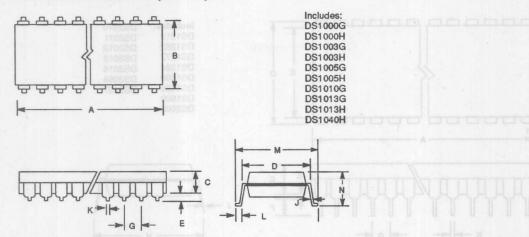
PKG	8-1	PIN	10-	PIN	14-	PIN	16-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
	3.04	3.56	2.79	3.30	3.O4	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN MM	0.008	0.012 0.30	0.008 0.20	0.012	0.008 0.20	0.012	0.008 0.20	0.012 0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

PKG	18-	PIN	20-	PIN	24-	PIN	28-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	1.020	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	25.91	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.260	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.10	6.60	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
ММ	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
ММ	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
ММ	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56



#### 8- TO 20-PIN GULLWING (300 MIL)

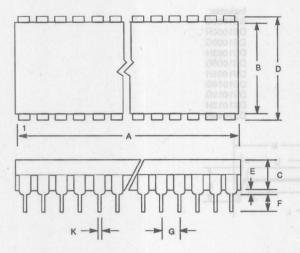


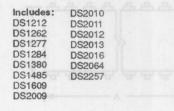
PKG	8-1	PIN	14-	PIN	16-	PIN	20-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.345	0.400	0.740	0.780	0.740	0.780	0.960	1.040
MM	8.76	10.16	12.19	13.20	18.79	9.81	24.38	26.41
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53
L IN.	0.030	0.050	0.030	0.050	0.030	0.050	0.030	0.050
MM	0.76	1.27	0.76	1.27	0.76	1.27	0.76	1.27
M IN.	0.370	0.420	0.370	0.420	0.370	0.420	0.370	0.420
MM	9.40	10.67	9.40	10.67	9.40	10.67	9.40	10.67
N IN.	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
MM	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57

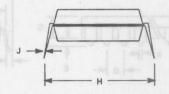
#### MECHANICAL DRAWINGS

#### 24- TO 40-PIN DIP (600 MIL)



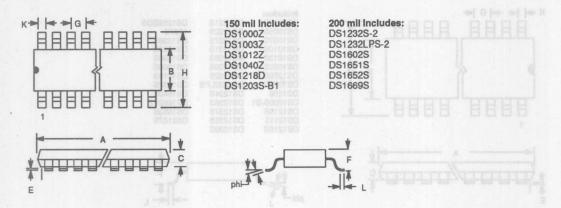






PKG	24-	PIN	28-	PIN	40-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	1.245	1.270	1.445	1.470	2.050	2.075
	31.62	32.25	36.70	37.34	52.07	52.71
B IN.	0.530 13.46	0.550 13.97	0.530 13.46	0.550 13.97	0.530 13.46	
C IN.	0.140	0.160	0.140	0.160	0.140	0.160
	3.56	4.06	3.56	4.06	3.56	4.06
D IN.	0.600	0.625	0.600	0.625	0.600	0.625
	15.24	15.88	15.24	15.88	15.24	15.88
E IN.	0.015 0.380	0.050 1.27	0.015 0.380	0.040 1.02	0.015 0.380	0.040
F IN.	0.120	0.145	0.120	0.145	0.120	0.145
	3.05	3.68	3.05	3.68	3.05	3.68
G IN.	0.090	0.110	0.090	0.110	0.090	0.110
	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.625	0.675	0.625	0.675	0.625	0.675
	15.88	17.15	15.88	17.15	15.88	17.15
J IN MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008	0.012
K IN.	0.015 0.38	0.022 0.56	0.015 0.38	0.022 0.56	0.015 0.38	0.022

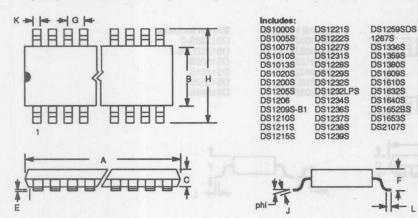
### 8-PIN SOIC (150 MIL AND 200 MIL)



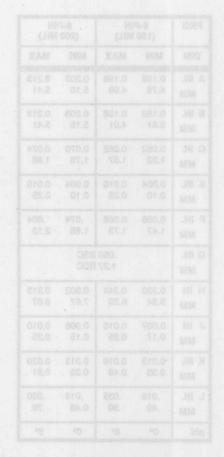
PKG	8-P (150		8-P (200	IN MIL)
DIM	MIN	MAX	MIN	MAX
A IN.	0.188	0.196	0.203	0.213
	4.78	4.98	5.16	5.41
B IN.	0.150	0.158	0.203	0.213
	3.81	4.01	5.16	5.41
C IN.	0.052	0.062	0.070	0.074
	1.32	1.57	1.78	1.88
E IN.	0.004	0.010	0.004	0.010
	0.10	0.25	0.10	0.25
F IN.	0.058	0.068	.074	.084
	1.47	1.73	1.88	2.13
G IN.		.050 1.27		
H IN	0.230	0.244	0.302	0.318
	5.84	6.20	7.67	8.07
J IN	0.007	0.010	0.006	0.010
	0.17	0.25	0.15	0.25
K IN.	0.013	0.019	0.013	0.020
	0.33	0.49	0.33	0.51
L IN.	.016	.035	.019	.030
	.40	.89	0.48	.76
phi	0°	8°	0°	8°

#### MECHANICAL DRAWINGS

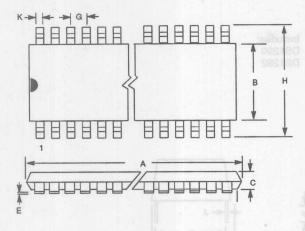
#### 16-, 20-, AND 24-PIN SOIC (300 MIL)



PKG	16-	PIN	20-	PIN	24-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.402	0.412	0.500	0.511	0.602	0.612
MM	10.21	10.46	12.70	12.99	15.29	15.54
B IN.	0.290	0.300	0.290	0.300	0.290	0.300
	7.37	7.65	7.37	7.65	7.37	7.65
C IN.	0.089	0.095	0.089	0.095	0.089	0.095
	2.26	2.41	2.26	2.41	2.26	2.41
E IN.	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012
F IN.	0.094	0.105	0.094	0.105	0.094	0.105
	2.38	2.68	2.38	2.68	2.38	2.68
G IN.				BSC BSC		
H IN	0.398	0.416	0.398	0.416	0.398	0.416
	10.11	10.57	10.11	10.57	10.11	10.57
J IN	0.009	0.013	0.009	0.013	0.009	0.013
MM	0.229	0.33	0.229	0.33	0.229	0.33
K IN.	0.013 0.33	0.019 0.48	0.013 0.33	0.019 0.48	0.013 0.33	0.019
L IN	.016	.040	.016	.040	.016	.040
	.40	1.02	.406	1.20	.40	1.02
phi	00	8°	0°	8°	0°	8°

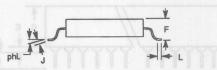


#### 24- AND 28-PIN 330 MIL SOIC



330 Mil Package
Includes:
DS2016S
DS2064S
DS2257S

350 Mil Package Includes: DS1385S DS1485S DS1262S

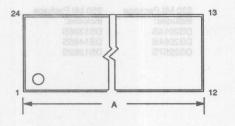


PKG	i mali	330	MIL BO	DY	350 MII	BODY
	24-	PIN	28-	PIN	28-	PIN
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	.594 15.10	.602 15.30	0.697 17.7	0.705 17.9	0.706 17.93	0.728 18.49
B IN. MM		.335 8.50	0.327 8.3	0.335 8.5	0.338 8.58	0.350 8.89
C IN.	.0925 2.35	.104 2.65	0.093 2.35	0.104 2.65	0.086 2.18	0.110 2.79
E IN.	.007 .19	.008	0.007 0.19	0.008 0.21	0.002 0.051	0.014 0.356
F IN.			<b>TYP.</b> .7		0.090 2.29	0.124 3.15
G IN.			BSC 27		0.050 I 1.27	3SC
H IN	0.452 11.5	.477 12.1	0.452 11.5	0.477 12.1	0.460 11.68	0.480 12.19
J IN	.004	.008 0.20	0.004 0.10	0.008 0.20	0.006 0.152	0.013 0.32
K IN.	.012 .30	0.20 0.50	0.012 0.30	0.020 0.50	0.014 0.36	0.020 0.51
L IN.	0.039	ГҮР	0.039	ГҮР	0.020 0.51	0.050 1.27
phl	0°	8°	0°	8°	0°	8°

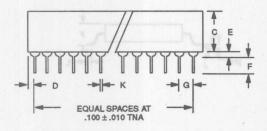
0.215		
		3633

#### **MECHANICAL DRAWINGS**

## 16- AND 24- PIN ENCAPSULATED PACKAGE (FLUSH BOTTOM – 450 MIL.)





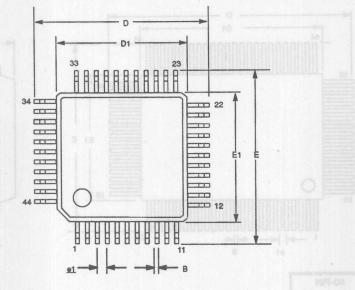


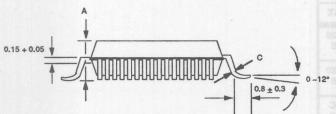
1			1
1			T
	- J		
1		Н	H

PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.820	0.840	1.310	1.330
	20.83	21.34	33.27	33.78
B IN.	0.440	0.460	0.440	0.460
MM	11.18	11.68	11.18	11.68
C IN.	0.330	0.370	0.330	0.370
	8.38	9.40	8.38	9.40
D IN.	0.180	0.210	0.215	0.245
	4.57	5.33	5.46	6.22
E IN.	0.020	0.040	0.020	0.040
	0.51	1.02	0.51	1.02
F IN.	0.110	0.140	0.110	0.140
	2.79	3.56	2.79	3.56
G IN.	0.090	0.110	0.090	0.110
	2.29	2.79	2.29	2.79
H IN	0.330	0.380	0.330	0.380
	8.38	9.65	8.38	9.65
J IN MM	0.008	0.012	0.008	0.012
	0.20	0.31	0.20	0.31
K IN.	0.015	0.021	0.015	0.021
	0.38	0.53	0.38	0.53

NOTE: On 16-pin package, pins 1 and 16 are missing by design. On 24-pin package, pins 1 and 24 are missing by design.

# 44-PIN QUAD FLAT PACK (PRELIMINARY) (MAN 0.00 X MAN 0.84) MOASTALF CAUG MISI-08

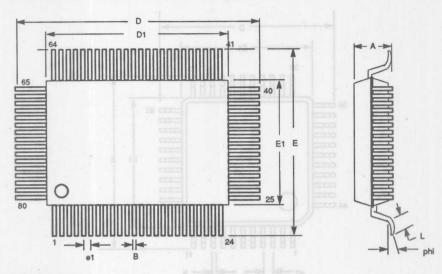




PKG	10 X 10	10 X 10 BODY		4 BODY
DIM	MIN	MAX	MIN	MAX
A MM	-	2.45	-	3.4
ВММ	0.30	0.45	0.20	0.50
C MM	0.13	0.23	0.10	0.20
D MM	13.65	14.35	16.95	18.00
E MM	13.65	14.35	16.95	18.00
D1MM	9.90	10.10	13.80	14.20
E1MM	9.90	10.10	13.80	14.20
L MM	0.65	0.95	0.50	1.10
e1 IN MM	0.315 0.80 B	sc	0.039 1.00 B	sc

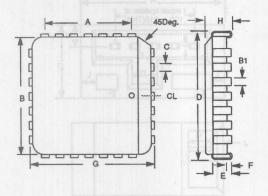
# MECHANICAL DRAWINGS

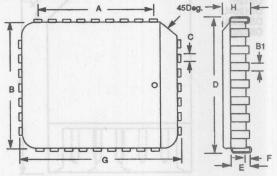
# 80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)



PKG	80-	PIN
DIM	MIN	MAX
A IN.	0.11 2.80	0.128 3.25
B IN. MM	0.010 0.25	0.020 0.45
e1 IN. MM	0.031 0.80	BSC
D1IN. MM	0.781 19.85	0.793 20.15
E1IN. MM		0.557 14.15
E IN. MM	0.688 17.50	0.720 18.30
D IN.	0.921 23.40	0.953 24.20
L IN	0.025 0.65	0.038 0.95
phl	0°	8°

#### 28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)

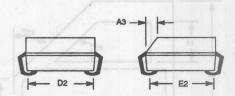




28- Pin Includes:

DS1212Q	
DS1284Q	
DS1285Q	
DS12885Q	

PKG	28-	PIN	32-	PIN
DIM	MIN	MAX	MIN	MAX
A IN.	0.300 E 7.62	BSC	0.400 E 10.16	ssc
B IN.	0.445	0.460	0.442	0.460
	11.30	11.68	11.30	11.68
B1 IN	0.013	0.021	0.013	0.021
MM	0.33	0.53	0.33	0.53
C IN	0.027	0.33	0.027	0.33
	0.68	0.84	0.68	0.84
D IN.	0.480	0.500	0.480	0.500
	12.19	12.70	12.19	12.70
D2IN.	0.390	0.430	0.390	0.430
	9.91	10.92	9.91	10.92
E IN.	0.090	0.120	0.060	0.095
	2.29	3.05	1.52	2.41
E2IN.	0.390	0.430	0.490	0.530
	9.91	10.92	12.45	13.46
F IN.	0.020 0.51		0.015 0.38	1.7 M
G IN	0.480	0.500	0.580	0.600
	12.19	12.70	14.7	15.24
H IN	0.165	0.180	0.100	0.140
	4.19	4.57	2.54	3.56

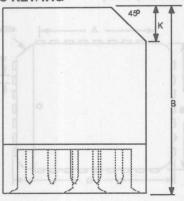


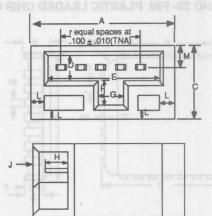
32-Pin includes: DS2009Q DS2010Q DS2011Q DS2012Q

## MECHANICAL DRAWINGS

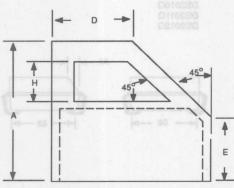
#### **ELECTRONIC KEY/TAG**

Includes: DS1201 DS1204U DS1205U DS1207





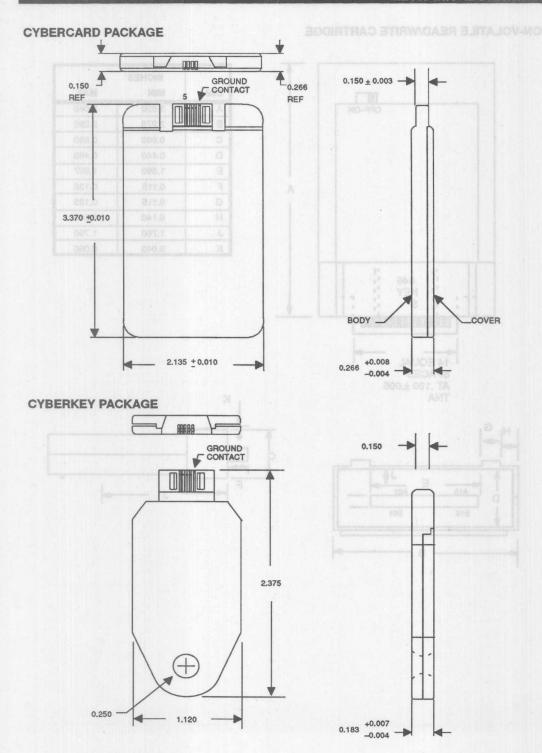
#### **KEY/TAG CAP**



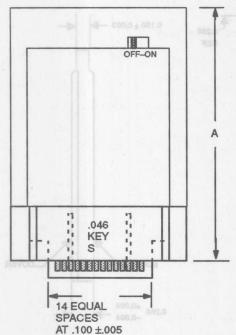
1		0 0 0	-
c	984. 58.	0,642 0	0,480
1 L	100	ممنعاله	100.0

PKG	ELECTRONIC KEY/TAG			/TAG AP
DIM	MIN	MAX	MIN	MAX
A IN.	0.610 15.50	0.650 16.51	0.790 20.07	0.810 20.57
B IN. MM	0.740 18.80	0.760 19.30	0.680 17.27	0.700 17.78
C IN.	0.310 7.87	0.355 9.02	0.405 10.29	0.425
D IN.	0.100 2.54	0.110 2.79	0.290 7.37	0.310 7.87
E IN.	0.505 12.83	0.515 13.08	0.410 10.41	0.430
F IN.	0.100 2.54	0.110 2.79		

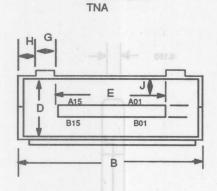
PKG	ELECTRONIC KEY/TAG		10.1	/TAG AP
DIM	MIN	MAX	MIN	MAX
G IN.	0.100 2.54	0.110 2.79		1.51 181
H IN	0.100 2.54	0.130 3.30	-	N. O.O.
J IN	0.030 0.76	0.060 1.52	A.0 0.4	14. 0.25
K IN.	0.045 1.14	0.055	-05	10.0 .30
L IN.	0.045	0.055 1.40	5.0 08	14:0 1.14
M IN.	0.100 2.54	0.110 3.30	7.0 88	10 35

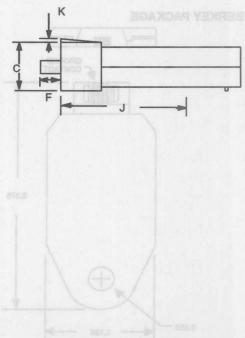


#### NON-VOLATILE READ/WRITE CARTRIDGE

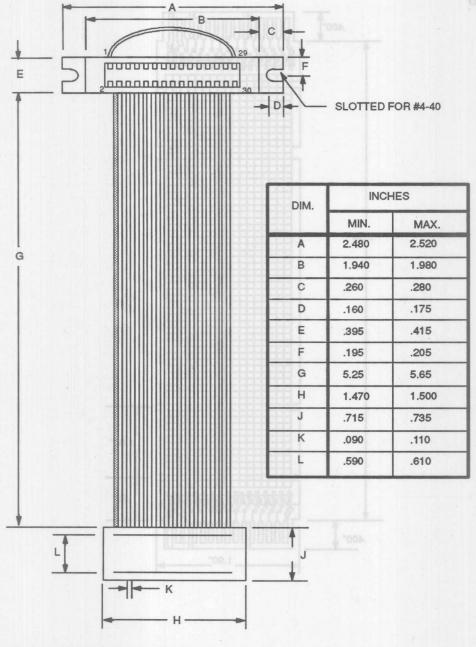


OAO -	INCHES	A 081.0
DIM	MIN	MAX
A	3.020	3.040
В	2.275	2.295
С	0.600	0.630
D	0.440	0.460
E	1.590	1.607
F	0.115	0.135
G	0.115	0.135
Н	0.140	0.160
J	1.760	1.790
K	0.040	0.060

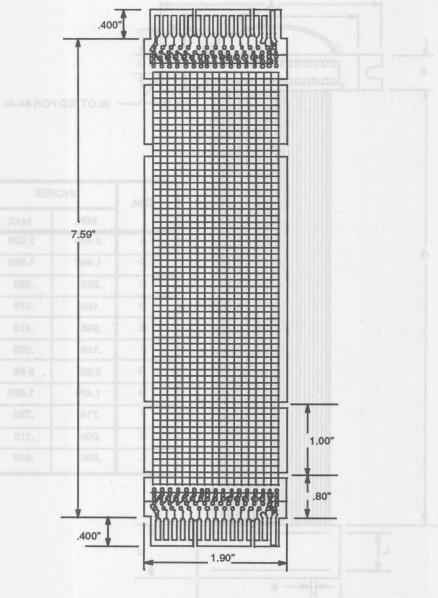




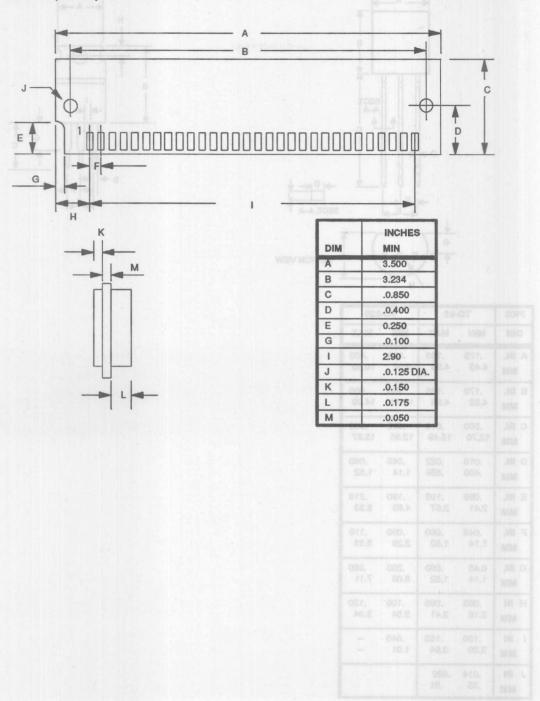
#### **BYTEWIDE CABLE HARNESS**

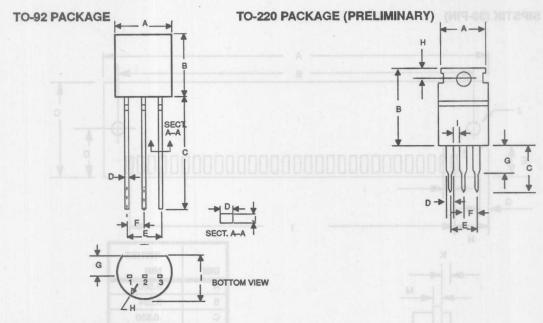


NOTES: COLOR STRIPE INDICATES PIN 1 END ON 28-PIN PULG. DIMENSION L IS CENTER TO CENTER DS9003 CARTRIDGE PROTO BOARD



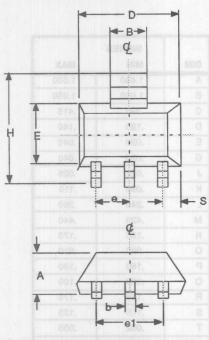
#### SIPSTIK (30-PIN)



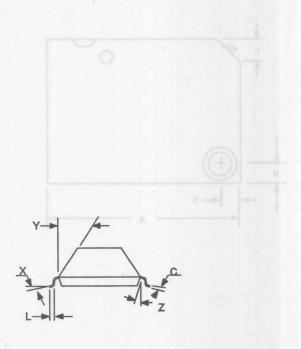


PKG	TO	-92	TO	-220
DIM	MIN	MAX	MIN	MAX
A IN.	.175	.195	.380	.420
	4.45	4.96	9.66	10.66
B IN.	.170	.195	.560	.600
	4.32	4.96	14.23	14.99
C IN.		.610 15.49	.510 12.95	.550 13.97
D IN.	.016	.022	.045	.060
	.406	.559	1.14	1.52
E IN.	.095	.105	.190	.210
	2.41	2.67	4.83	5.33
F IN.	.045	.060	.090	.110
	1.14	1.52	2.29	5.33
G IN.	0.45	.060	.200	.280
	1.14	1.52	5.08	7.11
H IN	.085	.095	.100	.120
	2.16	2.41	2.54	3.04
I IN	.130 3.30	.155 3.94	.040 1.01	=
J IN	.014 .35	.020 .51		

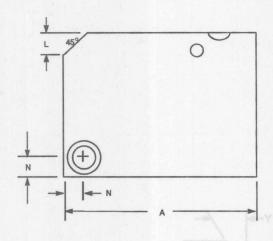
### SOT-223 PACKAGE



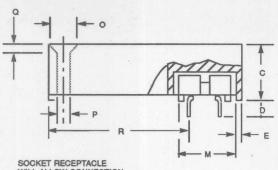
DIM	INC	HES	
1000	MIN	MAX	
A	-	.067	
b	.025	.033	
В	.116	.124	
С	.009	.013	
D	.248	.263	
0	.0905 typ.		
e1	.181 typ.		
E	.130	.145	
Н	.264	.287	
L	.016	.036	
S	.033	.041	
Х	10° MAX		
Υ	10°	20°	
Z	10° 20°		



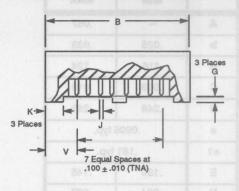
#### **DS1260 SMART BATTERY**



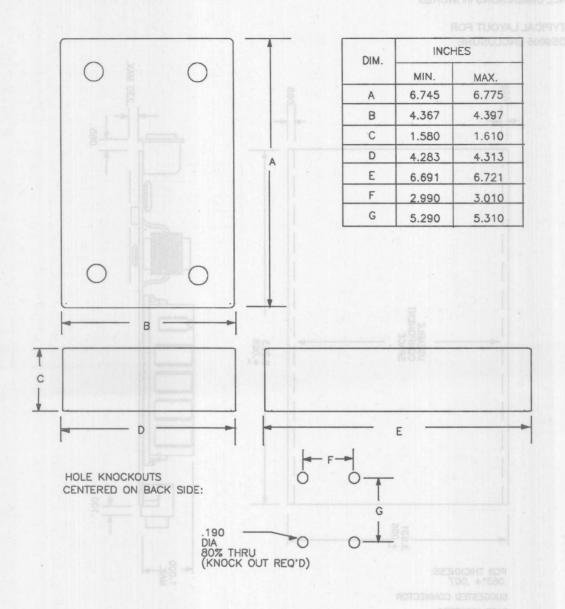
DIM	INCHES	MAX
A	1.480	1.500
В	1.030	1.050
C	.390	.415
D	.120	.140
E	.020	.040
G	.020	.040
J	.022	.026
K	.090	.110
L	.240	.260
M	.420	.440
N	.165	.175
0	.800	.810
P /	.160	.180
Q	.098	.109
R	.165	.175
S	.115	.125
Т	.052	.058
U	.980	1.000
٧	.055	.075



SOCKET RECEPTACLE
WILL ALLOW CONNECTION
WITH A STANDARD
16-DIP SOCKET.
BURDY DILB16R-11T
SUPPLIED WITH EACH ORDER.

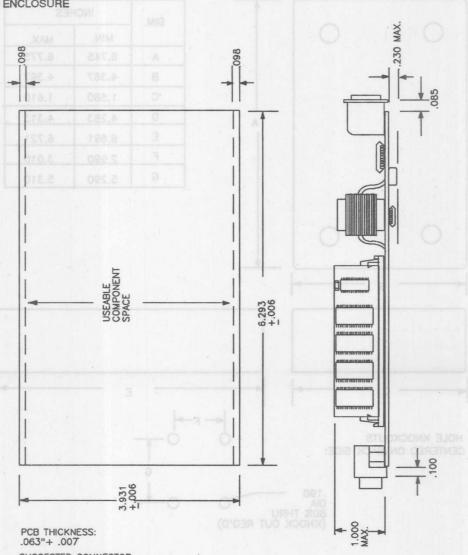


#### **DS9005 EUROCARD ENCLOSURE**



#### DS9006 SIP STIKTM MOTHERBOARD ALL DIMENSIONS IN INCHES

TYPICAL LAYOUT FOR **DS9005 ENCLOSURE** 



SUGGESTED CONNECTOR

PART NUMBERS:

RJ45- AMP #520252-4 9-PIN D-SUB FEMALE- AMP #745781-1 DIN-64 POS. FEMALE AMP# 531796-2